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0.7 V, 5.745 GHz CMOS RF low noise amplifier for IEEE 802.11a wireless LAN

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Abstract

In this paper, a 0.7 V, 5.745 GHz CMOS three stages low noise amplifier (LNA) intended for use in the IEEE 802.11 wireless local area networks (WLAN) or C-band front-end receiver. The circuit is simulated in standard 0.25 μm CMOS MOSIS. From the simulation results, the LNA exhibits a gain of 24.6 dB, noise figure (NF) of 5.48 dB, output return loss (S22) of −5.3 dB, input return loss (S11) of −17.3 dB, reverse isolation (S12) of −140.5 dB, and a power consumption is 8.75 mA from a single 0.7 V power supply.

One of the features of the proposed design is using transformer-coupled technique to enhance high gain.

Keywords: Low noise amplifier; RF front-end; Wireless local area network (WLAN); C-band receiver; Wireless personal area networks (WPAN)

1. Introduction

The market demand for low cost and high-performance wireless communication systems, including cellular phones, wireless local area networks (WLANs) and wireless personal area networks (WPAN), has attracted heavy investment and intensive research in the area of integrated RF transceiver design. The WLAN market has grown at a very rapid pace for the past several years. The 802.11 WLAN standards have evolved from 2.4 to 5 GHz bands to increase the rate of data transmission. The new generations of 802.11a WLAN and HiperLAN2 standards operating in the 5 GHz spectrum using orthogonal frequency division multiplexing (OFDM) are becoming popular due to high speed greater system capacity, low interference and less congestion. Typically, the required power level far the 802.11a standard in 5.15–5.25, 5.25–05.35 and 5.75–5.85 GHz bands is 50, 250 mW and 1 W, respectively [1–5]. WLAN is a fast growing market driven by the insatiable demand for high-speed wireless connectivity and increasing availability of cost-effective standards-based interoperable products. WLAN applications include: (1) the extension of the wired Ethernet to wireless mobile devices in the enterprise; (2) the seamless connectivity of networks inside the home for broadband Internet sharing; and (3) the increasing deployment of wireless accesses in the public areas such as airports and hotels. Furthermore, the core technology also has applications in the fixed wireless space enabling cost-effective wireless broadband network between buildings and into the homes. With the Federal Communications Commission (FCC) allocation of 300-MHz bandwidth in the 5-GHz frequency band for the Unlicensed National Information Infrastructure (UNII), high-data-rate (up to 54 Mb/s) WLANs become increasingly popular and important for mobile connectivity [6].

With the increasing demand for user capacity at higher data rates, WLAN chips must be able to cover WLAN standards in both the ISM and UNII bands for smooth migration

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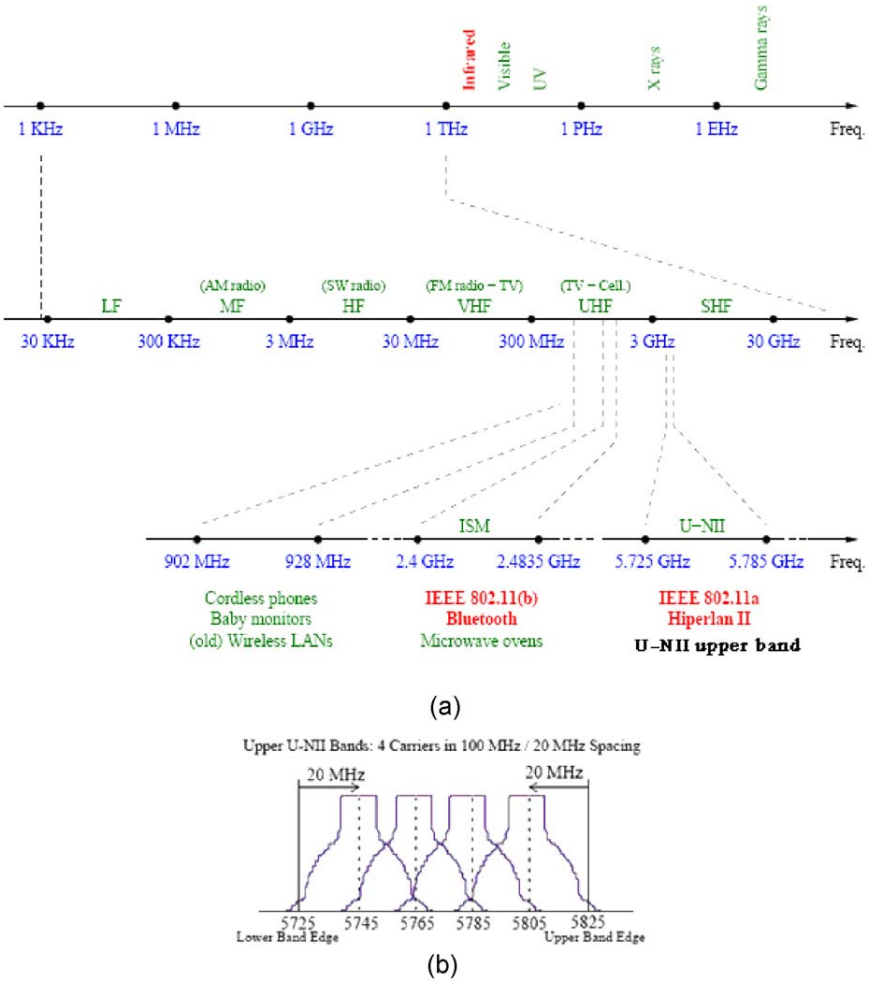

Fig. 1. (a) The EM spectrum allocation. (b) OFDM Phy frequency channel plan for the US [2,8–11].

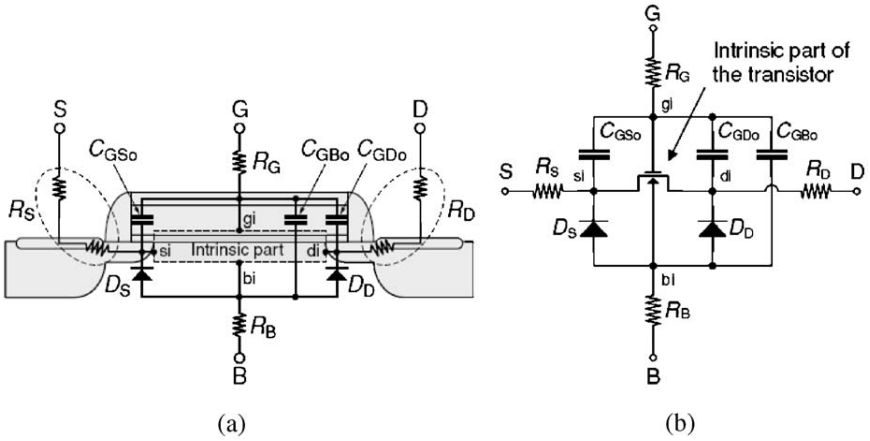

Fig. 2. (a) Definition of the extrinsic part of the MOS transistor and the extrinsic components including the series access resistances, the overlap parasitic capacitances, and the junction parasitic capacitances. (b) Simple equivalent circuit of the extrinsic part corresponding to (a) [13,14].

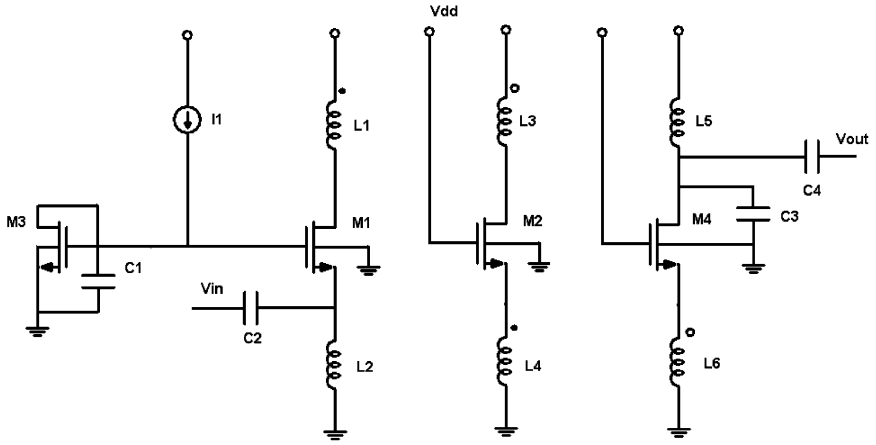

Fig. 3. Three stages low noise amplifier.

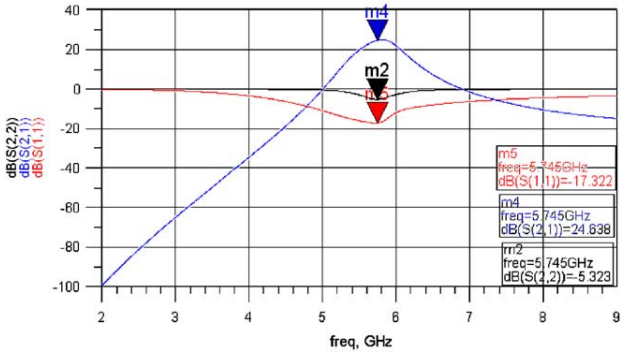

Fig. 4. Simulated input return loss, LNA gain, and output return loss of the LNA.

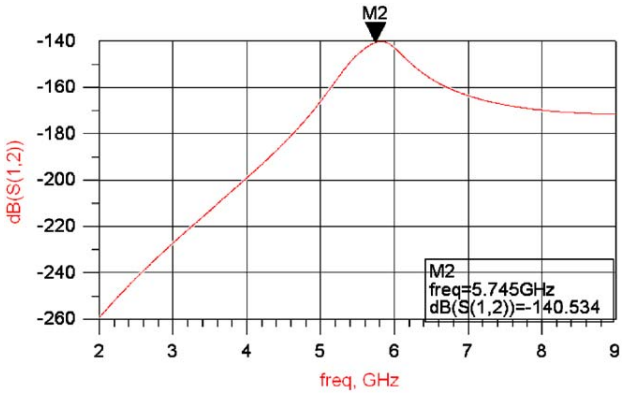

Fig. 5. Simulated reverse isolation of the LNA.

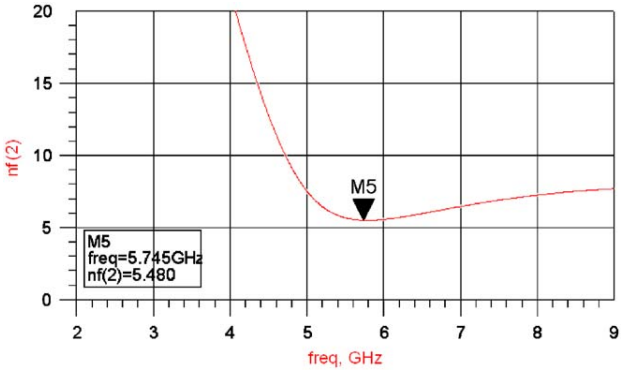

Fig. 6. Noise figure.

to higher data rates and transition between different standards [7]. Using this newly released frequency band, WLAN systems can provide data rates of several tens of megabits per second. The allocated frequencies overlap the European and US standard for the high-performance radio LAN (HiperLAN) frequency band as shown in Fig. 1 [2,8–11].

This paper describes a CMOS low noise amplifier (LNA) designed for IEEE 802.11a standard for the UNII band from 5.72 to 5.85 GHz, Sometimes referred to as *U-NII/ISM* due to overlap with the Instrumentation, Scientific and Medical (ISM) band. Simulated in a 0.25 μm CMOS process and operating from a single power supply of 0.7 V, the design consumes low power in addition to the presented LNA is ready for use in C-band communication.

2. LNA design

Being the first block of the receiver, the LNA plays a crucial role in amplifying the received signal while adding little noise to it [12].

Accurate MOSFET model at RF will enable better prediction of the simulation. Since the conventional RF MOSFET model, BSIM3v3 is not accurate at high frequencies; the model is improved by adding additional elements such as a gate resistance, substrate resistance, and diode to model

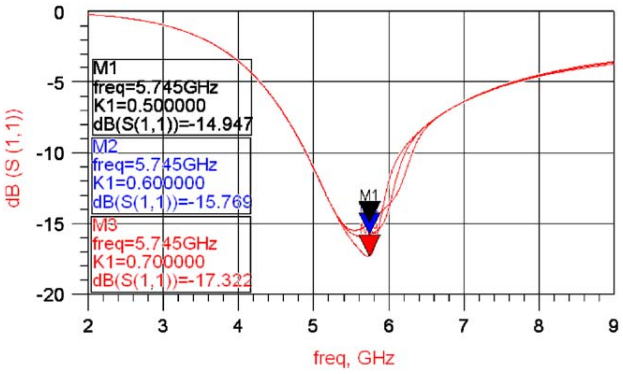

Fig. 7. Simulated input return loss of the LNA.

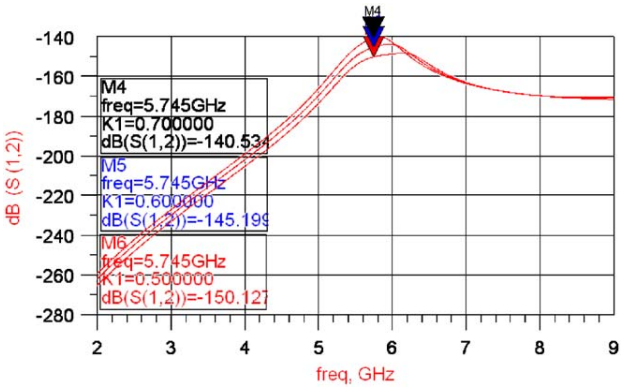

Fig. 8. Reverse isolation of the LNA.

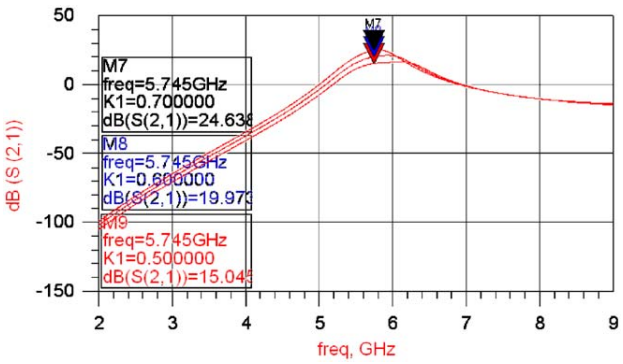

Fig. 9. LNA gain.

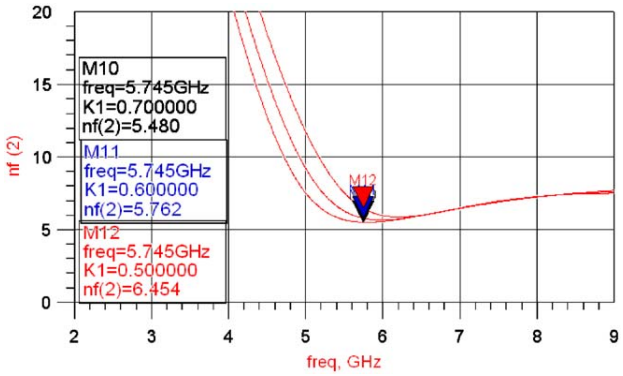

Fig. 10. Noise figure.

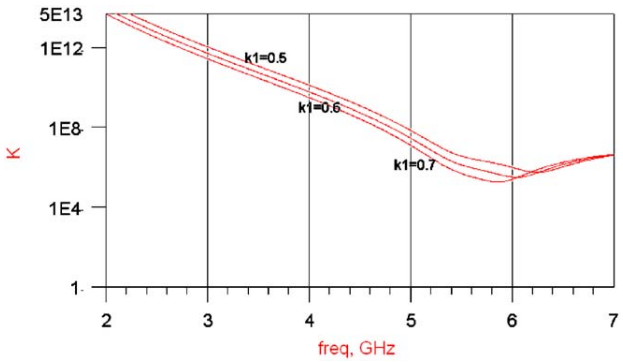

Fig. 11. Stability factor.

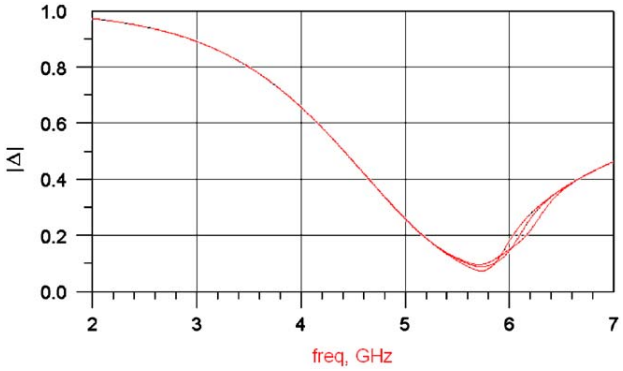

Fig. 12. Stability condition (1).

finger-type junction capacitances from drain and source as shown in Fig. 2 [13,14].

Many types of coupling such as transistor resistor-coupled amplifier, choke-coupled amplifier, and transformer-coupled transistor are used in the amplifier design in general. The high gain of transformer-coupled amplifier stage is the advantage of this type of coupling [15]. The transformer-coupled coupling type is used in the proposed LNA design.

Fig. 3 shows the LNA topology. It consists of three stages: the first stage is a common-gate amplifier with a shunt inductor, L2; common-gate amplifiers can be more easily matched and usually exhibit better linearity than common-source amplifiers. The second and the third stage are both common-gate also. Another interesting idea of using a common-gate amplifier, since a high reverse isolation in that case can be achieved from just one transistor, which is very good for

Table 1

Ref.	S_{11} (dB)	S_{22} (dB)	S_{12} (dB)	Gain (dB)	Vdd (V)	NF (dB)	Freq. (GHz)	Tech. C-MOS (μm)
[19]	−10.3	−19	−28	12.3	1.2	2.7	5.5	0.09
[20]	−11.7	−14	−30	13	1.9	2.7	5.5	0.09
[21]	−28	−14	−33	11.2	0.6	3.6	5.5	0.09
[22]	−20	−20	−30	20	1.5	3.5	5	0.18
[23]	−5.3	−10.3	–	13.2	1	2.5	5.8	0.18
	−7.1	−12.3	–	12.5	0.7	2.68	5.8	0.18
[24]	−30	–	−35	10	2	3	5.2	0.25
	−45	–	−36	11	2	2.17	5.2	0.25
[25]	−11.5	−12.3	−25.5	14.4	3	2.8	5.25	0.25
	−12.3	−11.9	−26.4	16	3	2.5	5.25	0.25
[26]	−23.5	−10.3	−30	8	2	4.8	5.5	0.25
[27]	−22.67	–	−75.8	16.45	1.8	2.66	5	0.18
[28]	−14	−17	–	11.45	1.8	3.4	5.7	0.18
[29]	–	–	–	16	1	1.8	5.8	0.18
	–	–	–	16	1	2.3	5.8	0.18
	–	–	–	16	1	2.5	5.8	0.18
[12]	−14	−17	–	11.6	1.8	3.4	5.7	0.18
	−10	−22	–	13.1	1.8	4.1	5.7	0.18
[30]	−12	−21	–	9.2	0.6	4.5	5	0.18
This design for $k = 0.5$, $k = 0.6$, $k = 0.7$	−14.9	−5.3	−150	15	0.7	6.45	5.745	0.25
	−15.7	−5.3	−145	19.9	0.7	5.76	5.745	0.25
	−17.3	−5.3	−140	24.6	0.7	5.48	5.745	0.25

low supply voltage by reducing the cascode element used in one stage.

The coupling technique between the three stages is depending on the mutual induction with magnetic coupling coefficient, $k1$; between L1 and L4 for the coupling between the first and second stage; in addition to the mutual induction with magnetic coupling coefficient, $k2$; between L3 and L6 for the coupling between the second stage and third stage. The mutual induction is used for enhancing the overall gain and as a matching technique between the stages also. C3 is used for tuning the output stage resonant frequency. The biasing circuit is consisting of the current source I1 and MOS transistor M3. C1 is selected such as reduce the variation of the biasing voltage.

3. Simulation results

The small-signal model of the transistor employed in the simulation is given in Fig. 2. The circuit simulation is performed using Cadence and are based on the BSIM 3.3 MOSFET model after the modification to match the RF model in Fig. 2 for accurate simulation results.

The circuit of Fig. 3 is simulated with ADS simulation tool. Fig. 4 shows the input return loss (−17.3 dB at the frequency of interest 5.745 GHz). In Fig. 5 simulated reverse isolation of the LNA (about −140.5 dB at 5.745 GHz). The plots of LNA gain and output return loss are shown in Fig. 4. The gain of the LNA at the operating frequency is 24.6 dB and the S22 is −5.3 dB.

From the simulation results the noise figure (NF) is 5.48 dB as presented in Fig. 6, NF is affected negatively by the loss resistor of the inductor on the source of M1 in addition to the gate resistance of M1.

All the above simulation assuming the magnetic coupling coefficients $k1$ and $k2$ are equal; $k1 = k2 = 0.7$.

4. Magnetic coupling coefficient

The magnetic coupling coefficient, k, of the transformer is depending on the fabrication process and limitations. Though the coupling-coefficient, k, variation is affecting on the simulation results as presented in Figs. 7–9. The presented LNA shown in Fig. 3 is simulated taking into account the magnetic coupling coefficient k variation from 0.5 to 0.7 assuming $k1 = k2$. The NF is presented also in Fig. 10.

5. Stability considerations

For the three stage LNA in Fig. 3; to be unconditionally stable at a given frequency, the following inequalities must

hold:

$$|\Delta| < 1 \quad (1)$$

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \quad (2)$$

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

If the S-parameters of an LNA satisfy conditions (1) and (2), it is stable for any passive load and generator impedance. In other words, this amplifier is *unconditionally stable.* On the other hand, it may be *conditionally stable* (stable for limited values of load or source impedance) if one or both of these conditions are violated [18].

The stability conditions for the LNA in Fig. 3 are presented in Figs. 11 and 12. The presented LNA is stable at the frequency of interest 5.745 GHz; also the presented LNA is unconditionally stable over a wide frequency range as shown in Figs. 11 and 12; magnetic coupling coefficient variation was considered. A wide frequency range (2–9 GHz) was considered to make sure that none of the out of the band frequencies can cause the LNA to oscillate [16–18].

6. Power consumption

Today the present goal is to reduce the power consumption, which lead to increase the battery used time and the cost as well. The power consumption reduction is one of the requirements today; one of the ways to achieve this is to reduce the supply voltage. In the presented design the three elements limitation including one transistor per stage is used for reducing the supply voltage to 0.7 V that leads to reduce the power consumption and using a battery for long time. The power consumption of the presented LNA is 8.75 mA from a 0.7 V single supply.

7. Conclusion

A low voltage CMOS three stage LNA is presented. The insertion of the capacitor C3 gives another degree of freedom to control the LNA gain. The LNA is simulated in standard 0.25 μm. The LNA presented here is useful in RF signal processing applications, in the front-end transceiver, C-band receivers, IEEE802.11a WLAN, and ISM.

The circuit presented here is compared with other circuits in terms of performance; and results are summarized in Table1.

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