INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS
Int. J. Circ. Theor. Appl. 2010; **38**:787–795
Published online 17 April 2009 in Wiley Online Library (wileyonlinelibrary.com). DOI: 10.1002/cta.596

The voltage mirror–current mirror pair as a universal element

Ahmed M. Soliman[1,*,†] and Ramy A. Saad[2]

[1]*Electronics and Communications Engineering Department, Cairo University, Giza 12613, Egypt*
[2]*Analog and Mixed-Signal Center (AMSC), Texas A&M University, College Station, TX 77843-3128, U.S.A.*

SUMMARY

The voltage mirror–current mirror (VM–CM) pair is shown to be a universal active element. It provides two alternative realizations for the nullor. The VM–CM pair is also capable of realizing the op amp and all the four types of the current conveyors namely CCII−, CCII+, ICCII− and ICCII+ as special cases. Copyright © 2009 John Wiley & Sons, Ltd.

Received 1 September 2008; Revised 1 March 2009; Accepted 1 March 2009

KEY WORDS: pathological voltage mirror; pathological current mirror; nullor; current conveyor

1. INTRODUCTION

The universal active element also known as the nullor was introduced in [1]. The nullor is a two-port network element comprising an input nullator and an output norator, as shown in Figure 1(a). The port voltage and current of a nullator are always zero, while the port voltage and current of a norator can independently take any value.

The admittance matrix stamp for the representation of the nullor can be considered as that for a voltage-controlled current source (VCCS) [2, 3] with a transconductance G_{mi} as described below, where G_{mi} is taken to a limit of infinity.

$$\begin{array}{c} \\ c \\ d \end{array} \begin{array}{c} \begin{array}{cc} a & \quad b \end{array} \\ \begin{pmatrix} G_{mi} & -G_{mi} \\ -G_{mi} & G_{mi} \end{pmatrix} \end{array} \tag{1a}$$

*Correspondence to: Ahmed M. Soliman, Electronics and Communications Engineering Department, Cairo University, Giza 12613, Egypt.
†E-mail: asoliman@ieee.org

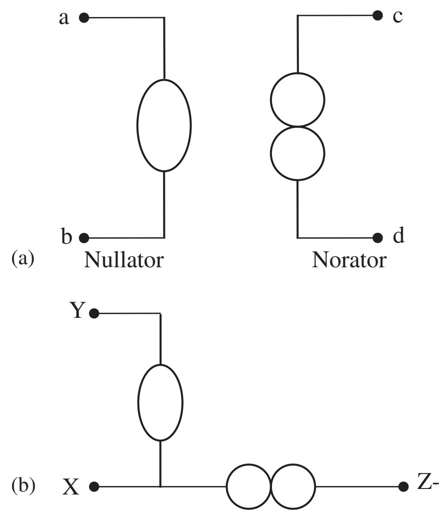

Figure 1. (a) Nullor element and (b) CCII- realized as a nullor with a common terminal.

Using the infinity variables the nullor description in Equation (1a) takes the form

$$\begin{array}{c} \\ c \\ d \end{array} \begin{array}{c} \begin{array}{cc} a & \quad b \end{array} \\ \begin{pmatrix} \infty_i & -\infty_i \\ -\infty_i & \infty_i \end{pmatrix} \end{array} \tag{1b}$$

The operational amplifier (op amp) is realized from a nullor with one of the norator terminals being grounded.

The nullor with a common terminal between nullator and norator realizes a CCII− as shown in Figure 1(b) [4–7]. The nullor however cannot realize the CCII+ or any of the two ICCIIs. The nullor has been used by several authors in important circuit applications [8–16] and was given the name the four terminal floating nullor (FTFN) in [13, 14].

2. VM–CM PAIR AS UNIVERSAL ELEMENT

Figure 2 represents the pathological voltage mirror (VM)–the pathological current mirror (CM) pair as a universal building block.

The VM [17–19] is a lossless two-port network element used to represent an ideal voltage reversing action and it is described by

$$V_{af} = -V_{bf} \tag{2a}$$

$$I_a = I_b = 0 \tag{2b}$$

Terminal f is the reference terminal for the VM.

DOI: 10.1002/cta

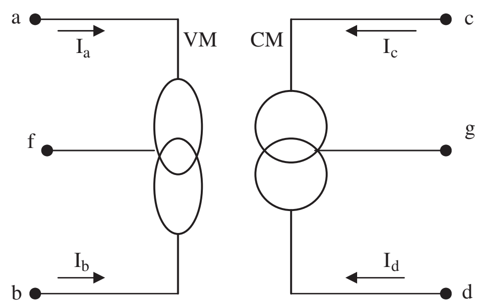

Figure 2. The VM–CM pair as a universal element.

The CM is a two-port network element used to represent an ideal current reversing action and it is described by

$$V_{cg} \quad \text{and} \quad V_{dg} \text{ are arbitrary} \tag{3a}$$

$$I_c = I_d \quad \text{and they are also arbitrary} \tag{3b}$$

Terminal g is the reference terminal for the pathological CM. Although the pathological CM element has the same symbol as the regular CM, it is a bi-directional element and has a theoretical existence [17–19]. Using the infinity variables the VM–CM pair is described in the nodal admittance matrix (NAM) [20, 21] by

$$\begin{matrix} & \begin{matrix} a & b & f \end{matrix} \\ \begin{matrix} c \\ d \\ g \end{matrix} & \begin{pmatrix} \infty_i & \infty_i & -2\infty_i \\ \infty_i & \infty_i & -2\infty_i \\ -2\infty_i & -2\infty_i & 4\infty_i \end{pmatrix} \end{matrix} \tag{4}$$

The summation of the three rows is zero indicating that the VM–CM pair is a floating element like the nullor.

3. GENERATION OF NULLOR FROM VM–CM PAIR

The VM–CM pair realizes the nullor by connecting the common terminal f of the VM to one of its terminals and connecting the common terminal g of the CM to one of its terminals as shown in Figure 3. To demonstrate this realization using the NAM description given in Equation (4), first connecting terminal f to b of the VM, hence adding the terms in their corresponding columns, the resulting NAM will be

$$\begin{matrix} & \begin{matrix} a & b,f \end{matrix} \\ \begin{matrix} c \\ d \\ g \end{matrix} & \begin{pmatrix} \infty_i & -\infty_i \\ \infty_i & -\infty_i \\ -2\infty_i & 2\infty_i \end{pmatrix} \end{matrix} \tag{5}$$

DOI: 10.1002/cta

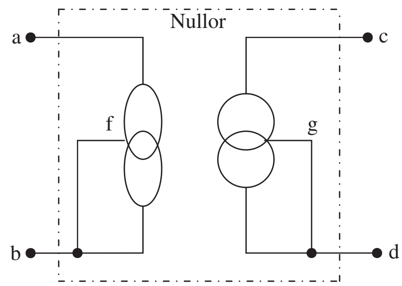

Figure 3. First nullor realization from VM–CM pair.

Next, connecting terminal g to d of the CM, hence adding the terms in their corresponding rows, the resulting NAM will be

$$\begin{array}{c} \\ c \\ d,g \end{array} \begin{array}{c} \begin{array}{cc} a & b,f \end{array} \\ \begin{pmatrix} \infty_i & -\infty_i \\ -\infty_i & \infty_i \end{pmatrix} \end{array} \tag{6}$$

The above equation represents the NAM of the nullor as given by Equation (1b).

If terminal d in Figure 3 is grounded then an op amp is obtained.

An alternative nullor realization using two VM to realize nullator and two CM to realize norator [18] is given in Figure 4(a).

Figure 4(b) represents the VCCS-based ideal model for the VM–CM pairs in Figure 4(a). Representing this ideal model using Y-matrix where the transconductance G_{mi} is taken to infinite limit, the following NAM is obtained:

$$\begin{array}{c} \\ c \\ n \\ d \end{array} \begin{array}{c} \begin{array}{ccc} a & m & b \end{array} \\ \begin{pmatrix} G_{mi} & -G_{mi}+G_{mi} & -G_{mi} \\ -G_{mi}+G_{mi} & G_{mi}-G_{mi} & -G_{mi}+G_{mi} \\ -G_{mi} & -G_{mi}+G_{mi} & G_{mi} \end{pmatrix} \end{array} \tag{7a}$$

Replacing G_{mi} by their infinity-variables representations, the result will be

$$\begin{array}{c} \\ c \\ n \\ d \end{array} \begin{array}{c} \begin{array}{ccc} a & m & b \end{array} \\ \begin{pmatrix} \infty_i & -\infty_i+\infty_i & -\infty_i \\ -\infty_i+\infty_i & \infty_i-\infty_i & -\infty_i+\infty_i \\ -\infty_i & -\infty_i+\infty_i & \infty_i \end{pmatrix} \end{array} \tag{7b}$$

The above NAM is equivalent to

$$\begin{array}{c} \\ c \\ d \end{array} \begin{array}{c} \begin{array}{cc} a & b \end{array} \\ \begin{pmatrix} \infty_i & -\infty_i \\ -\infty_i & \infty_i \end{pmatrix} \end{array} \tag{8}$$

The resulting NAM is the equivalent one for the nullor. This completes the proof that Figure 4(a) realizes a nullor.

DOI: 10.1002/cta

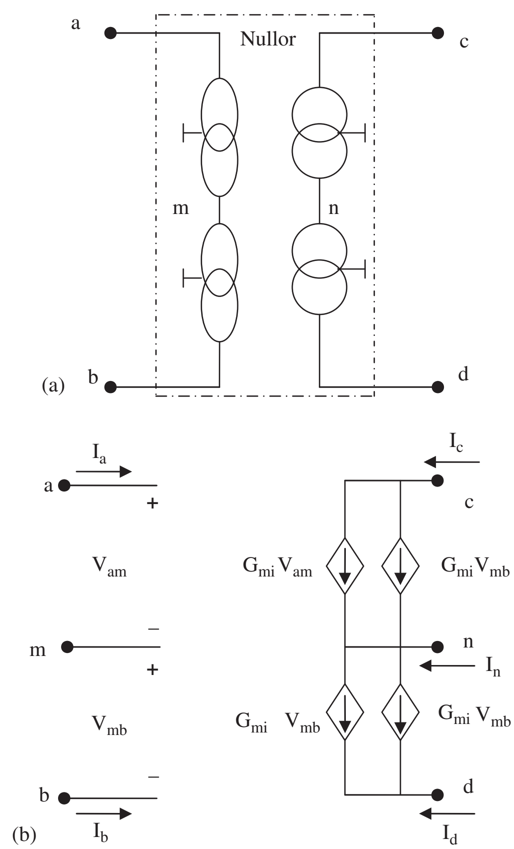

Figure 4. (a) Second nullor realization using two VM–CM pairs and (b) VCCS-based ideal model for the VM–CM pairs in Figure 4(a).

4. GENERATION OF CCII− AND CCII+

The CCII− is defined by the following equations:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{9}$$

The CCII− can be realized from the VM–CM pair as shown in Figure 5(a). This is a special case from Figure 3 obtained by connecting terminals a, c together to provide the X terminal of the CCII−. The terminals b, f provide the Y terminal and d, g the $Z-$ terminal. Applying this node

DOI: 10.1002/cta

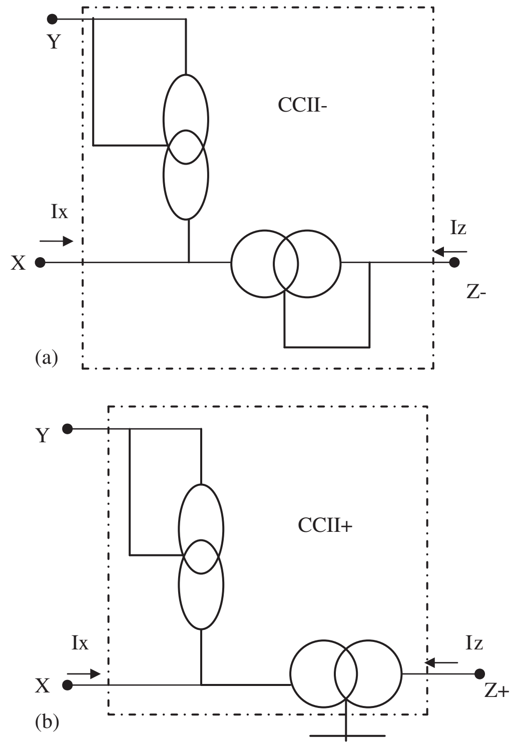

Figure 5. (a) Realization of CCII- from VM–CM pair and (b) realization of CCII+ from VM–CM pair.

equivalence to Equation (6) the CCII− in the NAM is represented by

$$\begin{array}{c} \\ X \\ Z \end{array} \begin{array}{c} \begin{array}{cc} X & Y \end{array} \\ \begin{pmatrix} \infty_i & -\infty_i \\ -\infty_i & \infty_i \end{pmatrix} \end{array} \tag{10}$$

The CCII+ is defined by the following equations:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{11}$$

Figure 5(b) is obtained from Figure 3 by grounding terminal g, the common terminal of the CM. Terminals a, c are connected together to provide the X terminal of the CCII+. The terminals b, f provide the Y terminal. The NAM of the CCII+ is obtained from Equation (5) by deleting the third row since g is grounded and is given by

$$\begin{array}{c} \\ X \\ Z+ \end{array} \begin{array}{c} \begin{array}{cc} X & Y \end{array} \\ \begin{pmatrix} \infty_i & -\infty_i \\ \infty_i & -\infty_i \end{pmatrix} \end{array} \tag{12}$$

From the NAM it is seen that the summation of the two rows is not zero indicating that the CCII+ is not a floating two-port element.

5. GENERATION OF ICCII− AND ICCII+

The ICCII− is defined by the following equations:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{13}$$

Figure 6(a) realizes the ICCII−, which is obtained from Figure 2 by grounding terminal f, the common terminal of the VM, and connecting terminals g to d to provide the $Z-$ terminal. The two terminals a and c are connected together to provide the Y terminal.

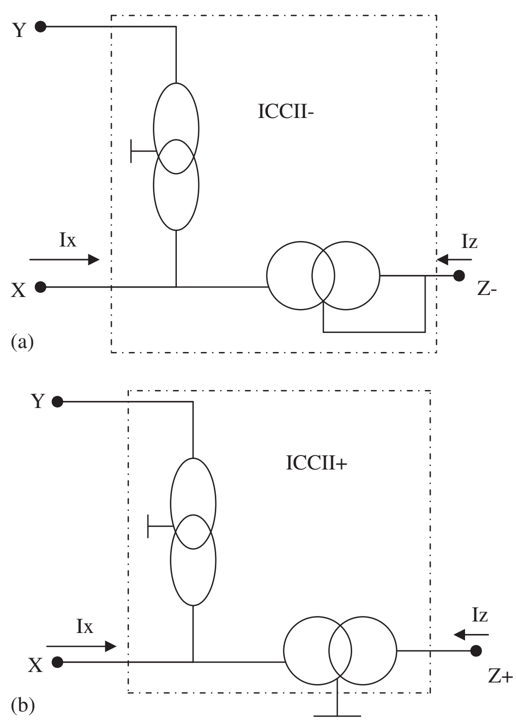

Figure 6. (a) Realization of ICCII− from VM–CM pair and (b) realization of ICCII+ from VM–CM pair.

DOI: 10.1002/cta

From Equation (4) by grounding terminal f thus deleting the third column, the NAM is simplified to

$$\begin{array}{c} \\ c \\ d \\ g \end{array}\begin{array}{c} \begin{array}{cc} a & b \end{array} \\ \begin{pmatrix} \infty_i & \infty_i \\ \infty_i & \infty_i \\ -2\infty_i & -2\infty_i \end{pmatrix} \end{array} \tag{14}$$

Connecting terminals d and g, thus adding the second and the third rows, the NAM of the ICCII− is given by

$$\begin{array}{c} \\ X \\ Z- \end{array}\begin{array}{c} \begin{array}{cc} X & Y \end{array} \\ \begin{pmatrix} \infty_i & \infty_i \\ -\infty_i & -\infty_i \end{pmatrix} \end{array} \tag{15}$$

The ICCII+ is defined by the following equations:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{16}$$

Figure 6(b) represents the ICCII+ realization from the VM–CM pair shown in Figure 2 by grounding terminals f and g that simplifies Equation (4) by deleting third row and third column. Therefore the NAM of the four terminal VM–CM pair with grounded common terminals is given by

$$\begin{array}{c} \\ c \\ d \end{array}\begin{array}{c} \begin{array}{cc} a & b \end{array} \\ \begin{pmatrix} \infty_i & \infty_i \\ \infty_i & \infty_i \end{pmatrix} \end{array} \tag{17}$$

Connecting terminals a, c in order to provide the X terminal of the ICCII+, the NAM is given by

$$\begin{array}{c} \\ X \\ Z+ \end{array}\begin{array}{c} \begin{array}{cc} X & Y \end{array} \\ \begin{pmatrix} \infty_i & \infty_i \\ \infty_i & \infty_i \end{pmatrix} \end{array} \tag{18}$$

Of course terminal b of the VM–CM pair is the Y terminal of the ICCII+ and terminal d of the VM–CM pair is the $Z+$ terminal of the ICCII+.

6. CONCLUSIONS

The VM–CM pair is shown to be a more universal active element than the nullor. It provides two alternative realizations for the nullor. On the other hand the nullor cannot realize the VM–CM pair. The two alternative nullor realizations based on the VM–CM pair are proved to have the NAM stamp of the nullor. The VM–CM pair is also capable of realizing the op amp and all the four types of the current conveyors namely CCII−, CCII+, ICCII− and ICCII+ as special cases. The NAM stamp of each of the four members of the current conveyors family is derived from the proper VM–CM pair realization.

DOI: 10.1002/cta

REFERENCES

1. Carlin HJ. Singular network elements. *IEEE Transactions on Circuit Theory* 1964; **11**:67–72.
2. Haigh DG, Clarke TJW, Radmore PM. Symbolic framework for linear active circuits based on port equivalence using limit variables. *IEEE Transactions on Circuits and Systems I* 2006; **53**(9):2011–2024.
3. Haigh DG, Radmore PM. Admittance matrix models for the nullor using limit variables and their application to circuit design. *IEEE Transactions on Circuits and Systems I* 2006; **53**(10):2214–2223.
4. De Jager W, Smit J. Design and symbolic analysis of current mode circuits. *Afdelingder Elektrotechneik* 1978.
5. Sedra AS, Smith KC. A second generation current conveyor and its applications. *IEEE Transactions on Circuit Theory* 1970; **17**:132–133.
6. Svoboda JA. Current conveyors, operational amplifiers and nullors. *IEE Proceedings Part G*: *Circuits*, *Devices and Systems* 1989; **136**:317–322.
7. Sedra AS, Roberts GW, Gohh F. The current conveyor: history, progress and new results. *IEE Proceedings Part G*: *Circuits*, *Devices and Systems* 1990; **137**:78–87.
8. Adams KM, Deprettere E. On the realization of gyrators by nullors and resistors. *International Journal of Circuit Theory and Applications* 1974; **2**:287–290.
9. Deprettere E. On the minimal realization of the gyrators by nullors and resistors I. *International Journal of Circuit Theory and Applications* 1974; **2**:383–390.
10. Deprettere E. On the minimal realization of the gyrators by nullors and resistors II. *International Journal of Circuit Theory and Applications* 1976; **4**:285–297.
11. Svoboda JA. Unique solvability of *RLC* nullor networks. *International Journal of Circuit Theory and Applications* 1983; **11**:1–6.
12. Svoboda JA. Using nullors to analyze linear networks. *International Journal of Circuit Theory and Applications* 1986; **14**:169–180.
13. Senani R. A novel application of four-terminal floating nullors. *Proceedings IEEE* 1987; **75**:1544–1546.
14. Senani R. Generation of new two-amplifier synthetic floating inductors. *Electronics Letters* 1987; **23**:1202–1203.
15. Carlosena A, Moschytz GS. Nullators and norators in voltage to current mode transformations. *International Journal of Circuit Theory and Applications* 1993; **21**:421–424.
16. Cel J. Adjoint nullator–norator networks. *International Journal of Circuit Theory and Applications* 1994; **22**: 409–418.
17. Awad IA, Soliman AM. Inverting second generation current conveyors: the missing building blocks, CMOS realizations and applications. *International Journal of Electronics* 1999; **86**:413–432.
18. Awad IA, Soliman AM. On the voltage mirrors and the current mirrors. *Analog Integrated Circuits and Signal Processing* 2002; **32**:79–81.
19. Awad IA, Soliman AM. A new approach to obtain alternative active building blocks realizations based on their ideal representations. *Frequenz* 2000; **54**:290–299.
20. Saad RA, Soliman AM. Use of mirror elements in the active device synthesis by admittance matrix expansion. *IEEE Transactions on Circuits and Systems I* 2008; **55**:2726–2735.
21. Saad RA, Soliman AM. A new approach for using the pathological mirror elements in the ideal representation of active devices. *International Journal of Circuit Theory and Applications* 2008. Online DOI: 10.1002/cta.534.