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Novel CMOS realizations of the inverting second-generation current conveyor and applications

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Abstract This paper presents two new CMOS realizations for the inverting current conveyor (ICCII). The proposed realizations offer enhanced features compared to previously reported ICCII. Also new oscillator circuits based on using the ICCII as an active element are presented. The presented oscillator circuits have the advantage that both the oscillation frequency and the oscillation condition can be adjusted independently. Also another application to the ICCII, which is a floating inductor, is proposed. A second order low pass filter using the proposed floating inductor is simulated and compared with the ideal result. The proposed ICCIIs and the presented applications are tested with SPICE simulations using CMOS 0.35 μm technology to verify the theoretical results.

Keywords Inverting current conveyor · Floating current source · Oscillator · Floating inductor

1 Introduction

The inverting second generation current conveyor (ICCII) was first introduced by Awad and Soliman [1] as a new block to the current conveyor family to obtain and design current-mode circuits from their voltage-mode counterparts [2, 3]. This active element can be easily implemented with CMOS technology. The ICCII can be considered a special case from the (Differential Voltage Conveyor) DVC [4], also known as Differential Difference Current Conveyor DDCC [5]. It is also related to other analog building block called (Differential Difference Amplifier) DDA [6, 7].

The symbolic representation of the inverting second-generation current conveyor is shown in Fig. 1. The relation between terminal voltages and currents can be given with following matrix equation [1].

$$\begin{pmatrix} I_y \\ V_x \\ I_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \begin{pmatrix} V_y \\ I_x \\ V_z \end{pmatrix} \quad (1)$$

The voltage at terminal X follows the voltage at terminal Y with negative sign. The current at terminal Z follows the current at terminal X in magnitude. In equation (1), the ±1 specifies the type of the current conveyor (ICCII+ or ICCII–). By convention, the positive sign is taken to mean that the current at the X and Z terminals are both flowing towards or away from the conveyor.

In the second section of this paper two new CMOS realizations of the ICCII– are presented. The principle of operation for each circuit will be described. In the third and fourth section of this paper, applications based on the ICCII– are introduced. These applications are two new oscillator circuits and a floating inductor.

2 New CMOS realizations for the ICCII–

In this section two new CMOS realizations for the ICCII– are proposed. The circuits' descriptions are introduced followed by SPICE simulations for the DC and AC characteristics between the terminal voltages and currents.

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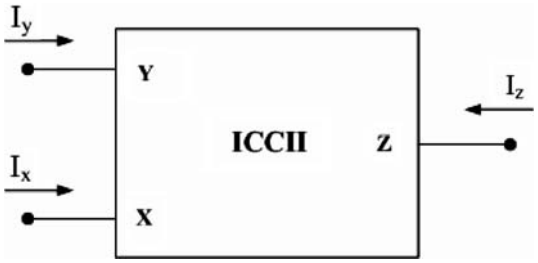

Fig. 1 Block diagram of ICCII

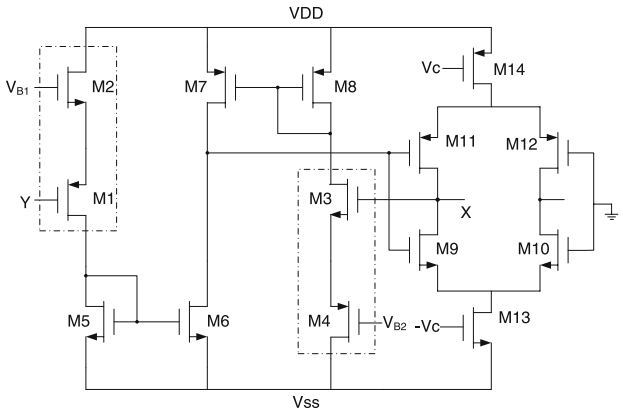

Fig. 3 The first proposed ICCII–

2.1 The first proposed ICCII–

Figure 2 shows the ICCII– reported by Awad and Soliman in [1]. The proposed ICCII–, shown in Fig. 3, is considered a modification for it. It uses a lower number of transistors. The mismatch limitations is reduced using a linear transconductor which depends on two matched CMOS pairs whose gain is controlled by two control voltages and are independent of the supply voltages. The input stage is formed from two matched CMOS pairs (M1-M2, M3-M4) and two current mirrors (M5-M6 and M7-M8).

$$I_{M1,2} = I_{M3,4} \tag{2}$$

$$\frac{K_{eff}}{2}\left(V_{B1} - V_Y - V_{Teff}\right)^2 = \frac{K_{eff}}{2}\left(V_X - V_{B2} - V_{Teff}\right)^2 \tag{3}$$

$$\text{where } K_{eff} = \frac{K_n K_p}{\sqrt{K_n} + \sqrt{K_p}}, V_{Teff} = V_{Tn} + \left|V_{Tp}\right| \tag{4}$$

The condition for $V_X = -V_Y$ is that $V_{B2} = -V_{B1}$.

The output stage formed from transistors M9 to M14 is the (Floating Current Source) FCS introduced in [8] for accurate current following action.

In the above analysis, the body of the transistors is connected to the source, which is necessary to make the threshold voltage constant for all transistors. This requires a twin well process so that the NMOS and PMOS transistors can be separated in different wells. Although twin-well CMOS process is available, it is not a standard VLSI technology.

Transistors aspect ratios are given in Table 1. The supply voltages are taken as ±1.5 V. The simulation results are shown in Fig. 4. A 0.13pF capacitor is connected between terminal X and the drain of M3 for compensation. The DC and AC characteristics between the Y and X terminals voltages are shown in Fig. 4(a) and Fig. 4(b,c) respectively. The DC and AC characteristics between the X

Table 1 Transistor aspect ratios of the first proposed ICCII– shown in Fig. 3

Transistor	W(μm)/L(μm)
M1,M2,M3,M4	35/1.05
M5,M6	8.75/1.05
M7,M8	26.25/1.05
M9,M10	17.5/0.35
M11,M12	35/0.35
M13	27.65/1.05
M14	57.75/1.05

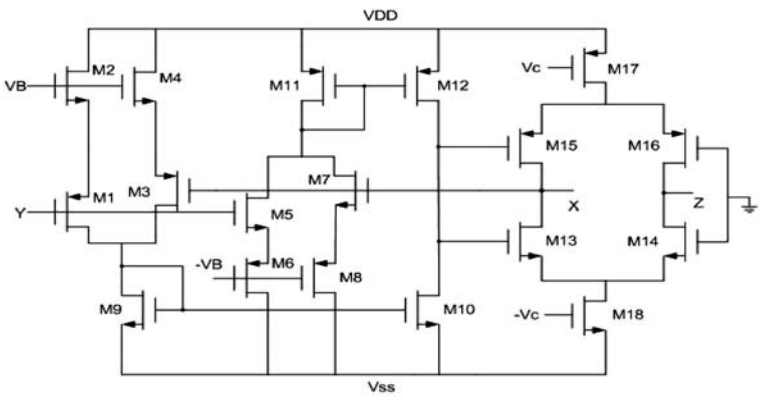

Fig. 2 The ICCII– CMOS realization reported in [1]

and Z terminals currents are shown in Fig. 4(d) and Fig. 4(e,f) respectively.

2.2 The Second proposed ICCII–

The floating current source (FCS) introduced by Arbel and Goldminz [8] was previously used as an output stage for the current conveyors [1]. The idea of using it as an input stage was first introduced by Bruun [9] and then used after that by Hassan [10]. The same idea is used here to build the second proposed ICCII–.

The circuit and a new proposed symbolic representation of the FCS are shown in Fig. 5(a) and Fig. 5(b) respectively. The relation between the terminals currents and voltages is given in equation (5) as in [10].

$$I_{Z1} = -I_{Z2} = -\frac{1}{2} v_d \left(\sqrt{K_n} \sqrt{2I_B - \frac{K_n v_d^2}{4}} + \sqrt{K_p} \sqrt{2I_B - \frac{K_p v_d^2}{4}} \right) \tag{5}$$

where

$$v_d = V_{Y1} - V_{Y2},\ K_n = \mu_n C_{OX} \frac{W_{1,2}}{L_{1.2}},\ \text{and}\ K_p = \mu_p C_{OX} \frac{W_{3,4}}{L_{3.4}} \tag{6}$$

Figure 6(a,b) shows both the block diagram and CMOS realization of the second proposed ICCII–. The input stage is formed from two FCSs for the voltage following action and the output stage is formed from a single FCS for the current following action.

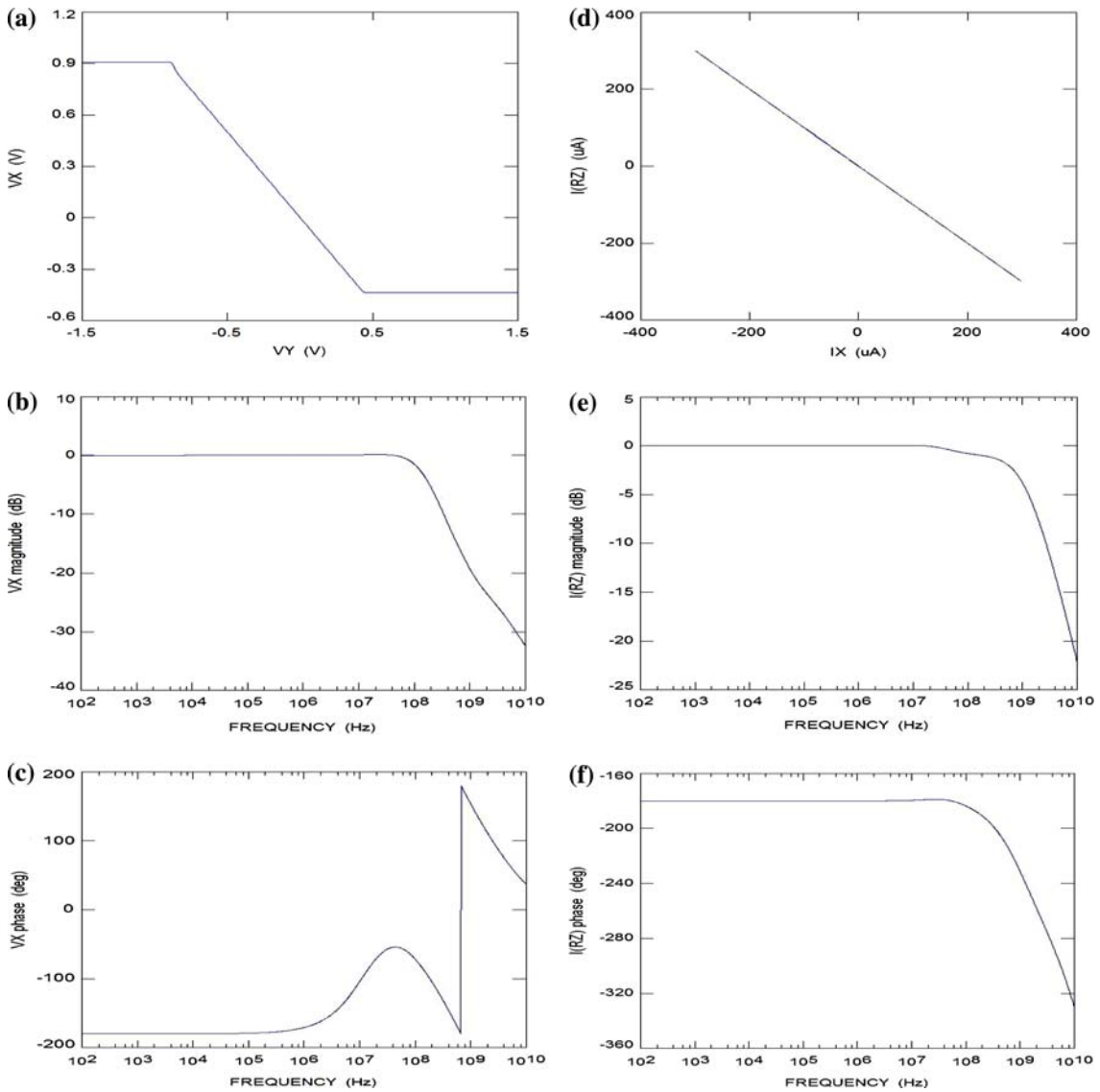

Fig. 4 Simulation results of the first proposed ICCII–

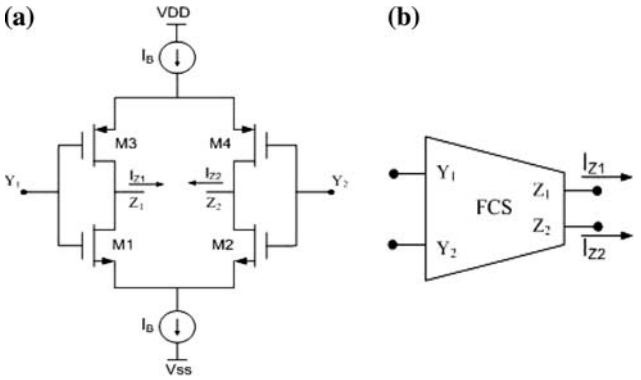

Fig. 5 (**a**) The CMOS FCS circuit [8] (**b**) A proposed symbolic representation of the FCS

For the voltage following action:

$$I_1 = -I_2 \tag{7}$$

By substitution in equation (5)

$$V_X = -V_Y \tag{8}$$

The operation of this circuit is insensitive to the threshold voltage variation caused by the body effect. Although the sources of transistors M1 and M2 are not connected to the body, their operation is still unaffected by the body effect because they form a differential pair, and, hence, have the same source voltage. This causes equal variation in the threshold voltage of M1 and M2, and, hence, the two threshold voltages cancel out. The same is true for all other differential pairs.

Transistors aspect ratios are given in Table 2. The supply voltages are taken as ±1.5 V. The simulation results are shown in Fig. 7. A 0.13pF capacitor is connected between terminal X and the drain of M3 for compensation. The DC and AC characteristics between the Y and X terminals voltages are shown in Fig. 7(a) and Fig. 7(b,c) respectively. The DC and AC characteristics between the X and Z terminals currents are shown in Fig. 7(d) and Fig. 7(e,f) respectively.

A fair comparison is done between the two proposed ICCII– circuits and Awad and Soliman second ICCII– [1]. From Table 3, one can easily notice that the first proposed ICCII– uses lower number of transistors which led to lower power consumption. The second proposed ICCII– achieves higher linearity voltage range as well as higher voltage and current bandwidths.

Table 2 Transistor aspect ratios of the second proposed ICCII– shown in Fig. 6(b)

Transistor	W(μm)/L(μm)
M1,M2,M7,M8	1.05/2.1
M3,M4,M9,M10	2.1/2.1
M13,M14	17.5/0.35
M15,M16	35/0.35
M5,M11,M17	27.65/1.05
M6,M12,M18	57.75/1.05

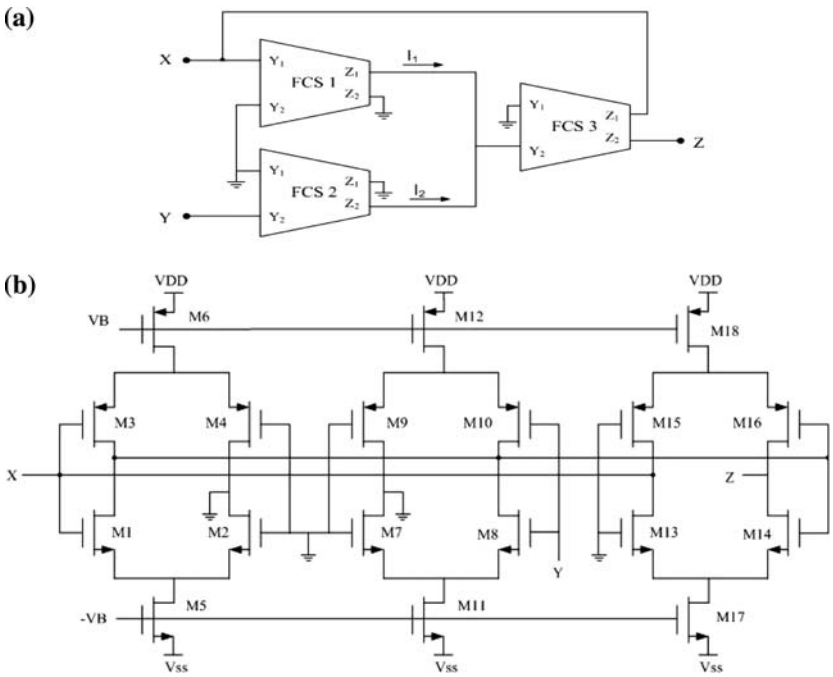

Fig. 6 (**a**) Second proposed ICCII– block diagram (**b**) Second proposed ICCII– CMOS realization

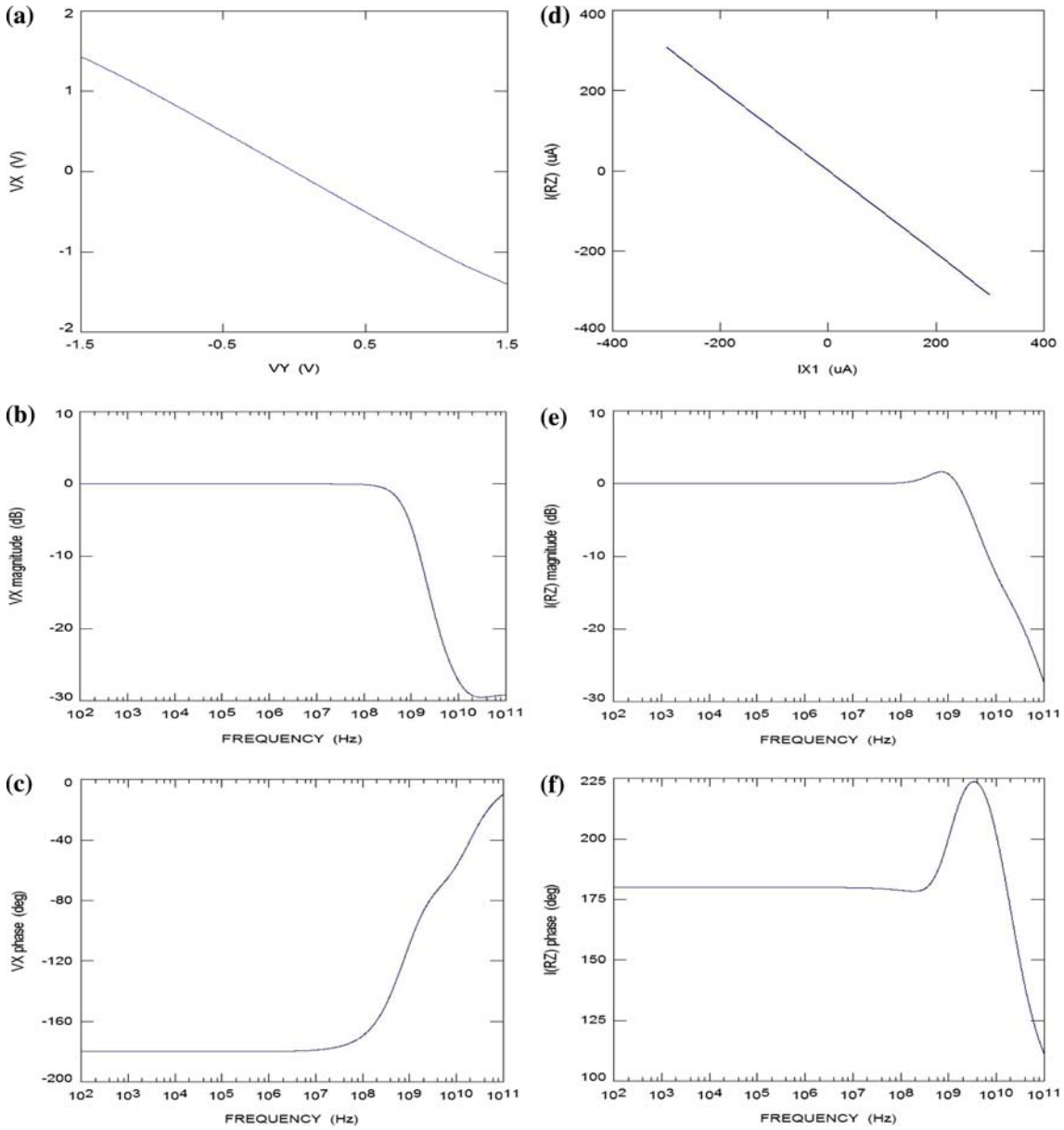

Fig. 7 Simulation results of the second proposed ICCII–

Table 3 Parameters of the ICCII– shown in Figs. 2 and 3 and 6

Parameters	Units	The ICCII– [1]	The first proposed ICCII–	The second proposed ICCII–
Input voltage range	V	–0.8 to 0.56	–0.9 to 0.44	–1.5 to 1.5
Voltage offset	mV	0.907	2.08	–2.97
3dB Bandwidth of open circuit voltage transfer gain	MHz	116	94	653
Input Current range	μA	–300 to 300	–300 to 300	–300 to 300
Current offset	μA	0.3	0.3	0.67
3dB Bandwidth of current transfer gain	GHz	0.86	1.49	2.6
R_x	Ω	7.6	8.4	25
Power consumption	mW	1	0.9	5
Number of transistors		18	14	18

3 New proposed ICCII– based oscillators

Different oscillators circuits based on using the CCII as an active element have been introduced in literature [11–13]. Two new proposed oscillator circuits employing three ICCII– and six grounded passive elements is shown in Fig. 8(a,b). The oscillator circuit shown in Fig. 8(b) is obtained from the previously reported CCII based oscillator shown in Fig. 4(b) in [11] by modifying it using ICCII–. The state equations of the two proposed oscillator are given as follows

$$\begin{pmatrix} \frac{dv_1}{dt} \\ \frac{dv_2}{dt} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{C_1 R_1} \\ \frac{1}{C_2 R_3} & \frac{1}{C_2}\left(\frac{1}{R_4} - \frac{1}{R_2}\right) \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \end{pmatrix} \tag{9}$$

From equation (9), the condition of oscillation, and the radian frequency of oscillation are given, respectively, by

$$R_4 = R_2 \tag{10}$$

$$\omega_o = \frac{1}{\sqrt{C_1 C_2 R_1 R_3}} \tag{11}$$

The advantage of the proposed oscillator circuits is that both the oscillation frequency and the oscillation condition can be adjusted independently. Furthermore, a single grounded resistor can be used to adjust the oscillation frequency so these oscillators are called single resistor controlled oscillators (SRCOs). It worth noting that the proposed oscillator circuit shown in Fig. 8(a) is also valid, with the same state equations, using ICCII+.

As a design example, the first oscillator circuit is tested with SPICE simulations. The elements are chosen as $R_1 = R_2 = R_3 = R_4 = 1\ k\Omega$ and $C_1 = C_2 = 40pF$, which results in an oscillation frequency of 3.98 MHz. The ICCII– used in simulations is the one proposed in Fig. 2 with supply voltage of ±1.5 V and Transistors aspect ratios are reported in Table 1. The waveform of the simulated filter and the corresponding Fourier transform is shown in Fig. 9(a) and Fig. 9(b) respectively.

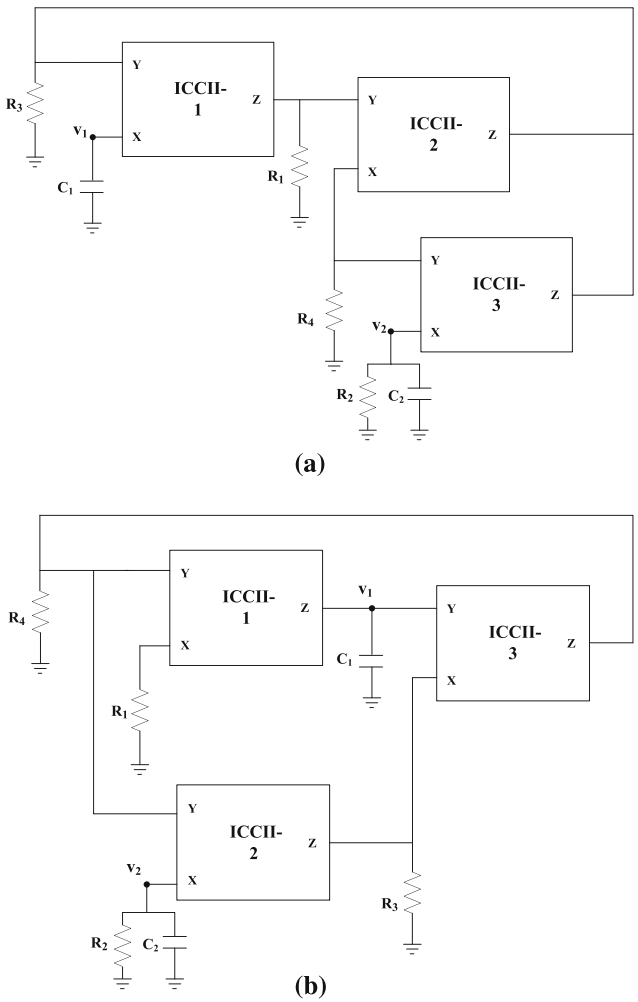

Fig. 8 (**a**) The first proposed oscillator topology (**b**) The second oscillator topology

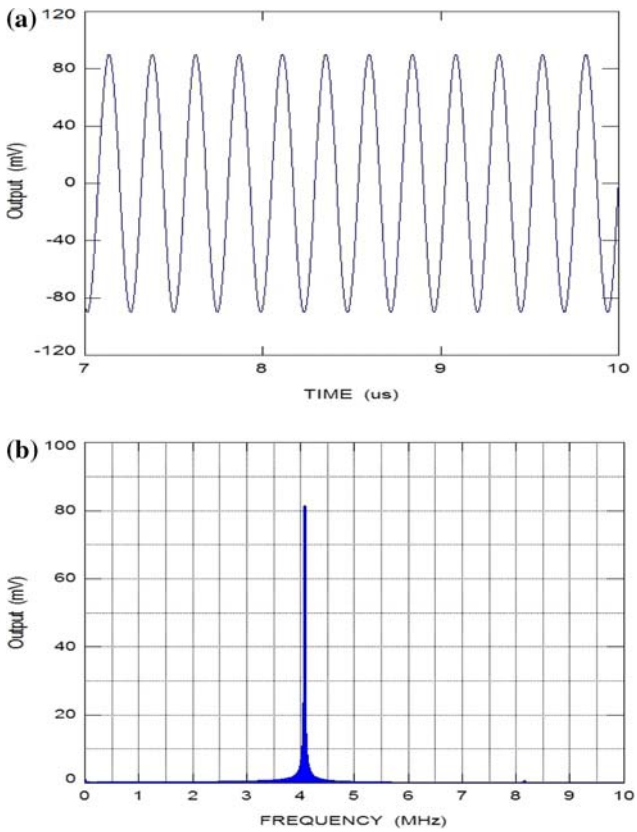

Fig. 9 (**a**) The output waveform of the proposed oscillator (**b**) The corresponding Fourier transform

4 New proposed ICCII– based floating inductor

A new proposed floating inductor using employing four ICCII–, two floating resistors, and a grounded capacitor is shown in Fig. 10. The proposed circuit is obtained from the previously reported CCII based floating inductor reported in [14] by modifying it using ICCII–. The transmission matrix of the proposed inductor is given as follows

$$T = \begin{pmatrix} 1 & sCR_1R_2 \\ 0 & 1 \end{pmatrix} \tag{12}$$

So between terminals 1 and 2, we can get a floating inductor of inductance:

$$L = CR_1R_2 \tag{13}$$

Spice simulation, shown in Fig. 11, is done to verify that the input impedance between the terminals 1 and 2 behaves as an inductor.

As a design example, a second order low pass filter is simulated using the proposed inductor and the simulation results are compared with the ideal curves when using an ideal floating inductor. The low pass filter component values are chosen to achieve $\omega_o = 50Mrad/\sec$ and maximally flat response. Simulations are shown in Fig. 12.

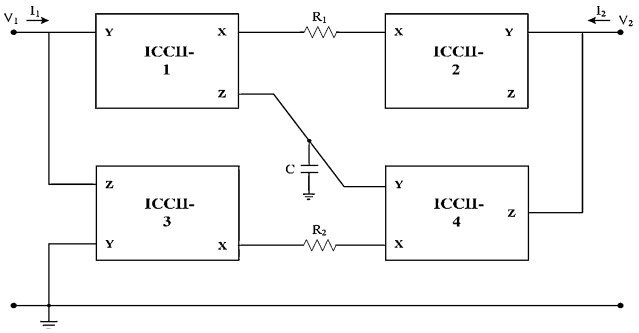

Fig. 10 Proposed ICCII– based floating inductor

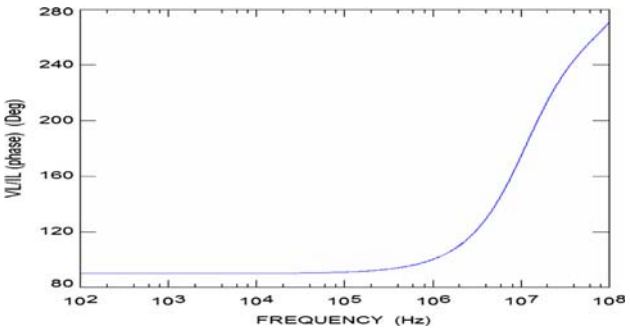

Fig. 11 The phase of the input impedance of the proposed inductor

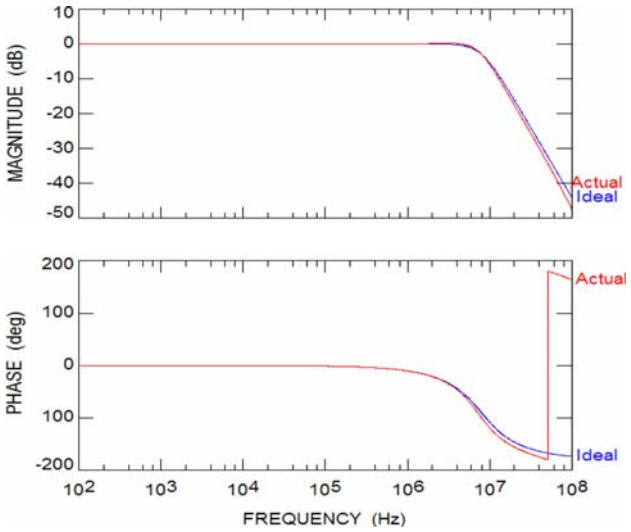

Fig. 12 AC response of the low pass filter using the proposed inductor compared with the ideal curves

5 Conclusion

Two new CMOS realizations for the ICCII– have been presented. The first one offers low power consumption and the second one offers good linearity and bandwidth. Also two new oscillator circuits based on using the ICCII– have been proposed as an application. Both the oscillation frequency and the oscillation condition of the proposed oscillator circuits can be adjusted independently. A floating inductor using the ICCII– is also proposed. A second order low pass filter is realized using this floating inductor.

References

1. Awad, I. A., & Soliman, A. M. (1999). Inverting second-generation current conveyors: the missing building blocks, CMOS realizations and applications. *International Journal of Electronics, 86*(4), 413–432.
2. Roberts, G. W., & Sedra, A. S. (1989). All current-mode selective circuits. *Electronics Letters, 25*(12), 759–761.
3. Carlosena, A., & Moschytz, G. S. (1993). Nullators and norators in voltage to current mode transformations. *International Journal of Circuit Theory and Applications, 21*(4), 421–424.
4. Elwan, H. O., & Soliman, A. M. (1997). A Novel CMOS differential voltage current conveyor and its applications. *IEE Proceedings. Circuits, Devices and Systems, 144*, 195–200.
5. Chiu, W., Liu, S. I., Tsao, H. W., & Chen, J. J. (1996). CMOS differential difference current conveyors and their applications. *IEE Proceedings. Circuits, Devices, 143*, 91–96.
6. Huang, S. C., Ismail, M., & Zarabadi, S. R. (1993). A wide range differential difference amplifier: A basic block for analog signal processing in MOS technology. *IEEE Transactions on Circuits and Systems, 40*, 289–300.
7. Mahmoud, S. A., & Soliman, A. M. (1999). The current feedback differential difference amplifier: New CMOS realization with rail-to-rail class AB output stage. *Proceedings of ISCAS, 2*, 120–123.

8. Arbel, A. F., & Goldminz, L. (1992). Ouput stage for current-mode feedback amplifiers, theory and applications. *Analog Integrated Circuits and Signal Processing, 2*, 234–255.
9. Bruun, E. (1994). CMOS current conveyors, IEEE International Symposium on Circuits and Systems. *Circuits and Systems Tutorial*, 632–641.
10. Hassan, H. M. (2005). Novel high performance CMOS analog building blocks suitable for analog signal processing, Master Thesis, Cairo University, Egypt.
11. Soliman, A. M. (1999). Synthesis of grounded capacitor and grounded resistor oscillators. *Journal of the Franklin Institute, 336*, 735–746.
12. Soliman, A. M. (1998). Current mode CCII oscillator using grounded capacitors and resistors. *International Journal of Circuit Theory and Applications, 26*(5), 431–438.
13. Soliman, A. M. (1998). Novel generation method of current mode Wien type oscillator using current conveyors. *International Journal of Electronics, 85*(6), 737–747.
14. Kiranon, W., & Pawarangkoon, P. (1997). Floating inductance simulation based on current conveyors. *Electronics Letters, 33*(21), 1748–1749.

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