

SYNTHESIS OF CONTROLLED SOURCES BY ADMITTANCE MATRIX EXPANSION*

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The admittance matrix expansion method based on using nullors and pathological mirror elements is used to provide a systematic synthesis method of controlled sources. Four new realizations of the current controlled voltage source (CCVS) using a single grounded resistor are given. Three new nodal admittance matrix expansions (NAM) for the voltage controlled voltage source (VCVS) are introduced in this paper. The voltage mirror current mirror pair is used as intrinsic element in the NAM expansion. Eight new realizations for the noninverting VCVS using two grounded resistors are given. Eight realizations for the inverting VCVS using two grounded resistors are also given. Two new NAM expansions for the current controlled current source (CCCS) are introduced in this paper. The voltage mirror current mirror pair is used as an intrinsic element in the NAM expansion. Eight realizations for the CCCS using two grounded resistors are given. The generation of the controlled sources using a single building block is also discussed and the adjoint relations between VCVS and CCCS are summarized.

Keywords: Admittance matrix expansion; VCVS; CCCS; VCCS; nullors; current conveyor; inverting current conveyor.

1. Introduction

A symbolic framework for systematic synthesis of controlled sources based on nodal admittance matrix (NAM) expansion was presented in Ref. 1. The matrix expansion process begins by introducing blank rows and columns, representing new internal nodes, in the admittance matrix. Then, nullators and norators are used to move the resulting admittance matrix elements to their final locations, properly describing either floating or grounded passive elements. Thus, the final NAM is obtained including finite elements representing passive circuit components and unbounded elements, so called infinity-variables, representing nullators and norators.

In this framework, nullators and norators^{2–4} shown in Fig. 1 ideally describe active elements in the circuit are used. The nullator and norator are pathological elements

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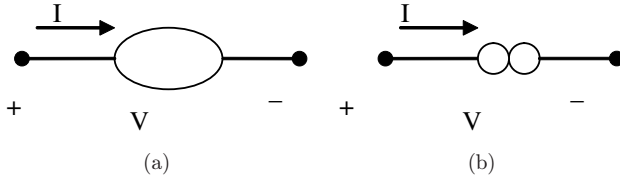


Fig. 1. The nullor elements (a) Nullator (b) Norator.

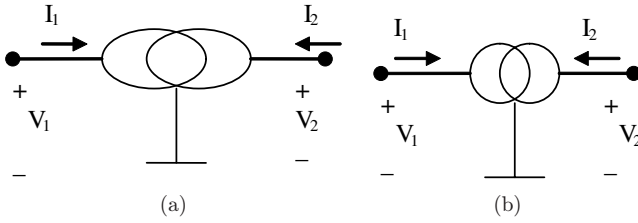


Fig. 2. The mirror elements (a) Voltage mirror (b) Current mirror.

that possess ideal characteristics and are specified according to the constraints they impose on their terminal voltages and currents. For the nullator $V = I = 0$, while the norator imposes no constraints on its voltage and current. A nullator-norator pair constitutes a universal active two-port network element called the nullor⁴ and hence, nullator and norator are also called nullor elements.

Additional pathological elements called mirror elements shown in Fig. 2 were introduced in Refs. 5 and 6 to describe the voltage and current reversing actions. The voltage mirror (VM), shown in Fig. 2(a), is a lossless two-port network element used to represent an ideal voltage reversing action and it is described by:

$$V_1 = -V_2, \tag{1a}$$

$$I_1 = I_2 = 0. \tag{1b}$$

The current mirror (CM), shown in Fig. 2(b), is a two-port network element used to represent an ideal current reversing action and it is described by:

$$V_1 \text{ and } V_2 \text{ are arbitrary,} \tag{2a}$$

$$I_1 = I_2, \text{ and they are also arbitrary.} \tag{2b}$$

Although the CM element shown in Fig. 2(b) has the same symbol as the regular current mirror, it is a bi-directional element and has a theoretical existence.

Very recently the systematic synthesis method based on admittance matrix expansion using nullor elements^{1,7-9} has been extended to accommodate mirror elements.^{10,11} This results in a generalized framework encompassing all pathological elements for ideal description of active elements. Accordingly, more alternative realizations are possible and a wide range of active devices can be used in the synthesis.

Although the nullor realization of different types of controlled sources has been described in the literature^{2,3} there was no generalized generation method available till the NAM expansion method was used in Ref. 1 to provide a systematic synthesis procedure to obtain the nullor realization of controlled sources.

In this paper the generation by NAM expansion method introduced in Ref. 1 to realize controlled sources is extended to accommodate the pathological VM and CM together with the nullor thus resulting in a complete set of active circuits realizing the controlled sources. For a physically realizable circuit, all the voltages and currents are always uniquely and definitely determined. This in turn implies that in the ideal representation of a physically realizable circuit, nullators (or VM) and norators (or CM) must occur in a pair.^{11,12}

2. Current-Controlled Voltage Sources (CCVS)

The transmission matrix of the CCVS is given by Refs. 1–3:

$$T = \begin{bmatrix} 0 & 0 \\ G & 0 \end{bmatrix}. \tag{3}$$

The admittance matrix Y for the CCVS using the linked infinity parameters is given in Ref. 1 as follows:

$$Y = \begin{bmatrix} 0 & G \\ \infty_1 & 0 \end{bmatrix}. \tag{4}$$

The nullor represented by the infinity term is referred to as the intrinsic nullor.¹

2.1. Positive gain CCVS

The admittance matrix expansion method was used in Ref. 1 to obtain the grounded resistor two nullors CCVS circuit shown in Fig. 3(a). Although this circuit has appeared before in Refs. 2 and 3, the expansion method reported in Ref. 1 provides a systematic generation method for this circuit. A second new realization for the noninverting CCVS using the intrinsic nullor and mirror elements is given next. It should be noted that the bracket notation for the VM and CM will be different from the brackets used for nullators and norators as was clarified in Refs. 10 and 11. Adding a third blank row and column, the G term in the first row and second

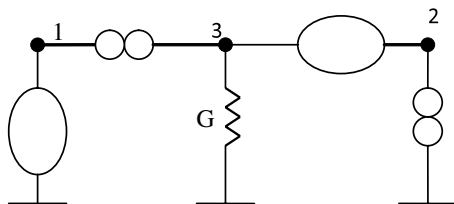


Fig. 3(a). Noninverting CCVS realization I using two nullors.^{1–3}

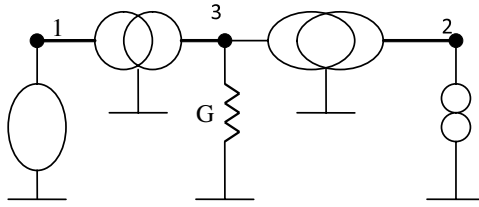


Fig. 3(b). A new noninverting CCVS realization II.

column, position 1, 2 is moved to position 1, 3 by the VM connected between nodes 2 and 3 and represented by the top bracket as follows:

$$Y = \begin{bmatrix} 0 & 0 & -G \\ \infty_1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}. \tag{5}$$

A CM is linked between nodes 1 and 3 and shown by the vertical bracket in order to move the $-G$ term to the diagonal position 3, 3 as shown below:

$$Y = \left[\begin{array}{ccc} 0 & 0 & 0 \\ \infty_1 & 0 & 0 \\ 0 & 0 & G \end{array} \right]. \tag{6}$$

The intrinsic nullor notation can also be represented by bracket notation used in Ref. 1 as follows:

$$Y = \left[\begin{array}{ccc} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & G \end{array} \right]. \tag{7}$$

The grounded G circuit is realizable directly from the above equation using a nullator, norator, a CM and a VM as shown in Fig. 3(b). It should be noted that the number of nullators plus the number of VM must equal to the number of norators plus the number of CM.⁵

2.2. Negative gain CCVS

The admittance matrix Y for the negative gain CCVS is given by:

$$Y = \begin{bmatrix} 0 & -G \\ \infty_1 & 0 \end{bmatrix}. \tag{8}$$

The well known single nullor floating G circuit^{2,3} was obtained in Ref. 1 using the intrinsic nullor only. The circuit is realizable by a grounded input operational amplifier (Op Amp) as given in Ref. 1.

Three new grounded G realizations are given next.

Adding a third blank row and column to Eq. (8) and using a nullator between nodes 2 and 3 to move $-G$ from the position 1, 2 to the position 1, 3 as follows:

$$Y = \begin{bmatrix} 0 & \overbrace{0 \ -G} \\ \infty_1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} . \tag{9}$$

A CM is added between nodes 1 and 3 to move the $-G$ to the diagonal position 3, 3 as shown below:

$$Y = \left. \begin{bmatrix} 0 & \overbrace{0 \ 0} \\ \infty_1 & 0 & 0 \\ 0 & 0 & G \end{bmatrix} \right\} . \tag{10}$$

Figure 4(a) represents the new inverting CCVS using two nullators, one norator and one CM. A practical realization for this realization using a grounded Y single current feedback operational amplifier (CFOA)¹³ is shown in Fig. 4(b).

A second new realization is obtained directly from Eq. (10) by replacing the norator of the intrinsic nullor from node 2 to ground by a CM resulting in the circuit shown in Fig. 4(c) which is practically realizable using two, CCII+. In this case the intrinsic element used is the nullator-CM pair. More details on the four possible types of the intrinsic element will be given in the next section.

The third new realization is obtained by adding a VM between nodes 2 and 3 in order to move the $-G$ from the 1, 2 position to $+G$ at the position 1, 3.

$$Y = \begin{bmatrix} 0 & \overbrace{0 \ G} \\ \infty_1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} . \tag{11}$$

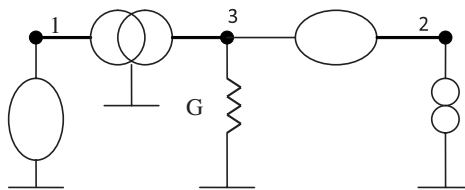


Fig. 4(a). Inverting CCVS realization I.

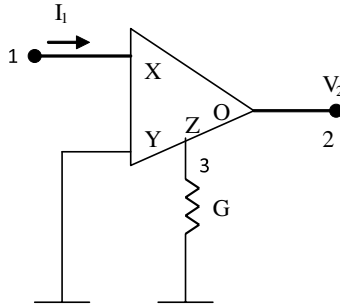


Fig. 4(b). Equivalent circuit to Fig. 4(a) using a CFOA.

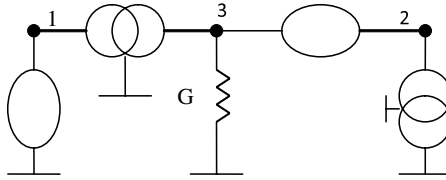


Fig. 4(c). Inverting CCVS realization II.

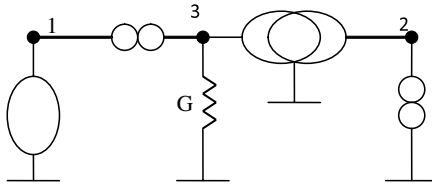


Fig. 4(d). Inverting CCVS realization III.

A norator is then used to move the G to the diagonal position 3, 3 as given by Eq. (12).

$$Y = \begin{bmatrix} 0 & \overbrace{0 \ 0} & \\ \infty_1 & 0 & 0 \\ 0 & 0 & G \end{bmatrix} \quad (12)$$

Figure 4(d) represents the third new inverting CCVS using one nullator, one VM and two norators.

Table 1 summarizes the grounded resistor realizations of the CCVS.

Table 1. Summary of the CCVS realizations using a grounded resistor.

Circuit figure	Gain polarity	Nullator	Norator	VM	CM	Circuit blocks	Ref.
3(a)	Positive	2	2	0	0	Two nullors (two CCII-)	1–3
3(b)	Positive	1	1	1	1	CCII+, ICCII-	New
4(a)	Negative	2	1	0	1	CCII+, CCII- (CFOA)	New
4(c)	Negative	2	0	0	2	Two CCII+ (CFOA)	New
4(d)	Negative	1	2	1	0	CCII-, ICCII-	New

3. Voltage Controlled Voltage Sources (VCVS)

Nullor realizations of the VCVS were given in Refs. 14–16. The transmission matrix for the VCVS is given by Refs. 1–3:

$$T = \begin{pmatrix} 1 & 0 \\ \frac{1}{A_V} & 0 \\ 0 & 0 \end{pmatrix}. \tag{13}$$

The voltage gain $A_V = V_2/V_1$ can be positive or negative. For the positive gain VCVS four alternative nullor realizations were given in Ref. 1, all of them provide infinite input impedance and employ one or two floating resistors. Eight new realizations of noninverting VCVS using grounded resistors are given next.

3.1. New NAM expansions for the VCVS

The types (i) and (ii) description of the admittance matrix Y for the VCVS are given in Table 2 together with the expanded 3×3 admittance matrices.¹ New expanded

Table 2. Admittance matrix description and its expansion for the VCVS.

Type	Admittance matrix	Expanded matrix	Ref.
(i)	$Y = \begin{bmatrix} 0 & 0 \\ -\frac{N}{D}\infty_1 & \infty_1 \end{bmatrix}$	$Y = \begin{bmatrix} 0 & 0 & 0 \\ 0 & \infty_1 & -\infty_1 \\ -N & 0 & D \end{bmatrix}$	1
		$Y = \begin{bmatrix} 0 & 0 & 0 \\ 0 & \infty_1 & \infty_1 \\ N & 0 & D \end{bmatrix}$	New
(ii)	$Y = \begin{bmatrix} 0 & 0 \\ \infty_1 & -\frac{D}{N}\infty_1 \end{bmatrix}$	$Y = \begin{bmatrix} 0 & 0 & 0 \\ \infty_1 & 0 & -\infty_1 \\ 0 & -D & N \end{bmatrix}$	1
		$Y = \begin{bmatrix} 0 & 0 & 0 \\ \infty_1 & 0 & \infty_1 \\ 0 & D & N \end{bmatrix}$	New
(iii)	$Y = \begin{bmatrix} 0 & 0 \\ \frac{N}{Q}\infty_1 & -\frac{D}{Q}\infty_1 \end{bmatrix}$ New	$Y = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & \infty_1 \\ -N & D & Q \end{bmatrix}$	New
		$Y = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & -\infty_1 \\ N & -D & Q \end{bmatrix}$	Equiv. to (iii) in 1

3×3 admittance matrices for types (i) and (ii) are introduced in the third column of Table 2. They employ an intrinsic VM-CM pair represented by the two infinities in the second row. They are equivalently represented by the bracket notation with different bracket type from the bracket used with the nullor. The intrinsic VM-CM pair used in the new expansion of type (i) is represented by a VM between nodes 2 and 3 and a CM between node 2 and ground. The intrinsic VM-CM pair used in the new expansion of type (ii) is represented by a VM between nodes 1 and 3 and a CM between node 2 and ground.

It should be noted that there are in fact four types of the intrinsic element used in the NAM expansion as explained next.

The nullor as intrinsic element and is represented by a nullator and a norator in the VCVS realization.

The nullator-CM pair as intrinsic element and is represented by a nullator and a CM in the VCVS realization.

The above two elements will appear in the same form in the second row of the NAM with opposite signs of the two infinities; their realization however will differ in using either a norator or a CM.

The VM-CM pair as intrinsic element is represented by a VM and a CM in the VCVS realization.

The VM-norator pair as intrinsic element is represented by a VM and a norator in the VCVS realization.

The above two elements will appear in the same form in the second row of the NAM with identical signs of the two infinities; their realization however will differ in using either a norator or a CM.

3.2. VCVS with positive gain $A_V = G_1/G_2$

The first realization given in this paper is based on expansion (i) Ref. 1, where N is taken as G_1 and D as G_2 . The NAM in this case which includes an intrinsic nullor is given by:

$$Y = \begin{bmatrix} 0 & 0 & 0 \\ 0 & \infty_1 & -\infty_1 \\ -G_1 & 0 & G_2 \end{bmatrix}. \tag{14}$$

The next step is to add a fourth blank row and column and use a CM between nodes 3 and 4 to move the $-G_1$ from the 3, 1 position to G_1 at the 4, 1 position as follows:

$$Y = \left. \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & \infty_1 & -\infty_1 & 0 \\ 0 & 0 & G_2 & 0 \\ G_1 & 0 & 0 & 0 \end{bmatrix} \right\}. \tag{15}$$

Finally a nullator is added between nodes 1 and 4 to move G_1 to the diagonal position 4, 4 as given by:

$$Y = \left[\begin{array}{cccc} 0 & 0 & 0 & 0 \\ 0 & \infty_1 & -\infty_1 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{array} \right] \quad (16)$$

The realization of the above equation is shown in Fig. 5(a). A practical realization of Fig. 5(a) using a CFOA is shown in Fig. 5(b).¹³ Representing the intrinsic element by a nullator between nodes 2 and 3 and a CM between node 2 and ground results in the circuit of Fig. 5(c).

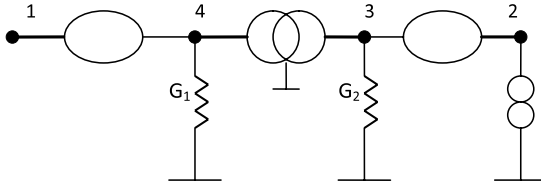


Fig. 5(a). Realization I-a of noninverting VCVS.

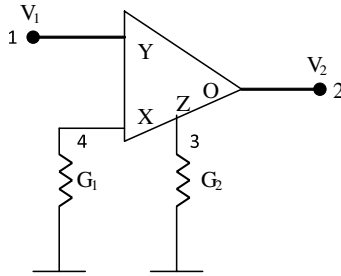


Fig. 5(b). Equivalent circuit to Fig. 5(a) using a CFOA.¹³

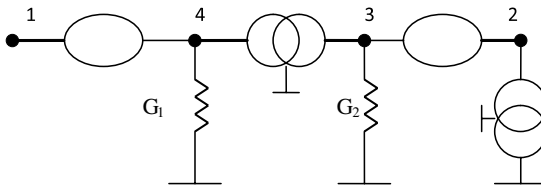


Fig. 5(c). Realization I-b of noninverting VCVS using two CCII+.

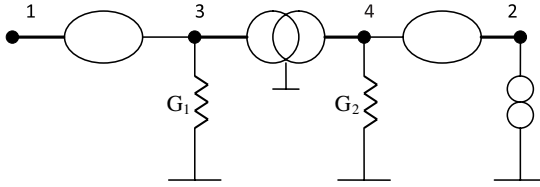


Fig. 5(d). Equivalent realization to Fig. 5(a).

The next realization given is based on expansion (ii) in Ref. 1 with N taken as G_1 and D as G_2 as given in Ref. 1 by:

$$Y = \begin{bmatrix} 0 & 0 & 0 \\ \infty_1 & 0 & -\infty_1 \\ 0 & -G_2 & G_1 \end{bmatrix}. \tag{17}$$

The above matrix was expanded in Ref. 1 resulting in a two nullor realization with a grounded G_1 and a floating G_2 . Next it is shown how to realize the above equation using grounded G_1 and grounded G_2 . Adding a fourth blank row and column and then adding a CM between nodes 3 and 4 to move $-G_2$ to be G_2 at the 4, 2 position as follows:

$$Y = \left. \begin{bmatrix} 0 & 0 & 0 & 0 \\ \infty_1 & 0 & -\infty_1 & 0 \\ 0 & 0 & G_1 & 0 \\ 0 & G_2 & 0 & 0 \end{bmatrix} \right\}. \tag{18}$$

Finally a nullator is added between nodes 2 and 4 to move G_2 to the diagonal position 4, 4 as given by

$$Y = \left. \begin{bmatrix} 0 & 0 & 0 & 0 \\ \infty_1 & 0 & -\infty_1 & 0 \\ 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{bmatrix} \right\}. \tag{19}$$

The grounded resistor realization of the above equation is shown in Fig. 5(d). This is similar to the realization given in Fig. 5(a) but nodes 3 and 4 are interchanged.

The second new realization given is based on the new NAM expansion given in Table 2 based on type (i) 2×2 admittance matrix, with N taken as G_1 and D taken as G_2 . The new NAM in this case is given by:

$$Y = \begin{bmatrix} 0 & 0 & 0 \\ 0 & \infty_1 & \infty_1 \\ G_1 & 0 & G_2 \end{bmatrix}. \tag{20}$$

The intrinsic VM-CM pair is realized by a VM between nodes 2 and 3 and a CM between nodes 2 and ground. Adding a fourth blank row and column and use a norator between nodes 3 and 4 to move G_1 to the position 4, 1 as described by:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & \infty_1 & \infty_1 & 0 \\ 0 & 0 & G_2 & 0 \\ G_1 & 0 & 0 & 0 \end{bmatrix} . \tag{21}$$

Finally a nullator is added between nodes 1 and 4 to move G_1 to the diagonal position 4, 4 as given by:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & \infty_1 & \infty_1 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} . \tag{22}$$

The new grounded resistor realizations of the above equation are shown in Figs. 6(a) and 6(b).

The third new realization is based on the new NAM expansion given in Table 2 based on modified type (ii), with N taken as G_1 and D taken as G_2 . The new NAM in this case is given by:

$$Y = \begin{bmatrix} 0 & 0 & 0 \\ \infty_1 & 0 & \infty_1 \\ 0 & G_2 & G_1 \end{bmatrix} . \tag{23}$$

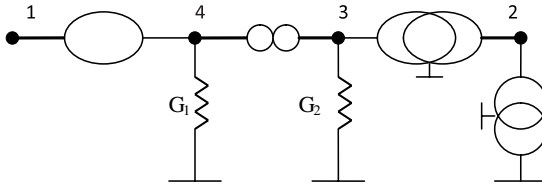


Fig. 6(a). Realization II-a of noninverting VCVS.

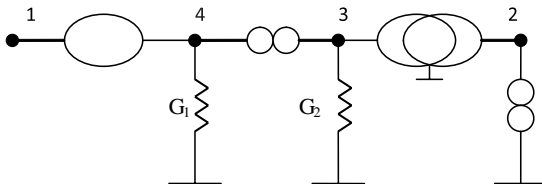


Fig. 6(b). Realization II-b of noninverting VCVS.

Adding a fourth blank row and column and use a norator between nodes 3 and 4 to move G_2 from the 3, 2 position to the 4, 2 position gives the following NAM:

$$Y = \left[\begin{array}{cccc} 0 & 0 & 0 & 0 \\ \infty_1 & 0 & \infty_1 & 0 \\ 0 & 0 & G_1 & 0 \\ 0 & G_2 & 0 & 0 \end{array} \right] . \tag{24}$$

A nullator is added next between nodes 2 and 4 to move G_2 to the diagonal position 4, 4 as follows:

$$Y = \left[\begin{array}{cccc} 0 & \overbrace{0 \ 0 \ 0 \ 0} & & \\ \infty_1 & 0 & \infty_1 & 0 \\ 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{array} \right] . \tag{25}$$

The new grounded resistor realizations of the above equation are shown in Figs. 7(a) and 7(b). The fourth new realization is based on the new NAM expansion given by Eq. (23). Adding a fourth blank row and column and use a CM between nodes 3 and 4 results in the following NAM:

$$Y = \left[\begin{array}{cccc} 0 & 0 & 0 & 0 \\ \infty_1 & 0 & \infty_1 & 0 \\ 0 & 0 & G_1 & 0 \\ 0 & -G_2 & 0 & 0 \end{array} \right] . \tag{26}$$

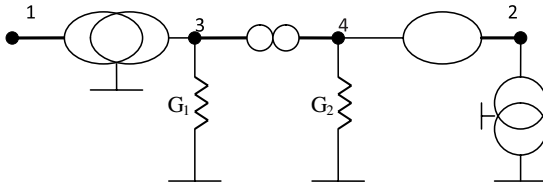


Fig. 7(a). Realization III-a of noninverting VCVS.

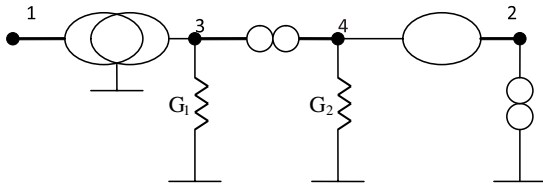


Fig. 7(b). Realization III-b of noninverting VCVS.

A VM is added between nodes 2 and 4 to move $-G_2$ to the diagonal position 4, 4 thus,

$$Y = \left[\begin{array}{cccc} 0 & 0 & 0 & 0 \\ \infty_1 & 0 & \infty_1 & 0 \\ 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{array} \right] \quad (27)$$

The new grounded resistor realization of the above equation is shown in Fig. 8(a). This realization includes two VM and two CM which is realizable using two, ICCII+. An alternative realization is shown in Fig. 8(b).

3.3. VCVS with negative gain $A_V = -G_1/G_2$

Two alternative realizations for the nullor based inverting VCVS are given in Ref. 1, both of them employ two floating resistors. In this section new circuits for realizing the inverting VCVS using grounded resistors are given.

The first realization is based on the NAM expansion (i) with $N = -G_1$ and $D = G_2$ resulting in the following Y expanded matrix:

$$Y = \left[\begin{array}{ccc} 0 & 0 & 0 \\ 0 & \infty_1 & -\infty_1 \\ G_1 & 0 & G_2 \end{array} \right] \quad (28)$$

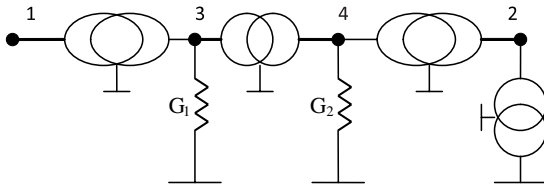


Fig. 8(a). Realization IV-a of noninverting VCVS.

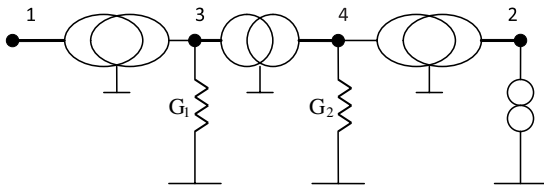


Fig. 8(b). Realization IV-b of noninverting VCVS.

Adding a fourth blank row and column and connect a norator between nodes 3 and 4 to move G_1 from the 3, 1 position to the 4, 1 position results in the following NAM:

$$Y = \left[\begin{array}{cccc} 0 & 0 & 0 & 0 \\ 0 & \infty_1 & -\infty_1 & 0 \\ 0 & 0 & G_2 & 0 \\ G_1 & 0 & 0 & 0 \end{array} \right]. \tag{29}$$

A nullator is added next between nodes 1 and 4 to move G_1 to the diagonal position 4, 4 as follows:

$$Y = \left[\begin{array}{cccc} 0 & 0 & 0 & 0 \\ 0 & \infty_1 & -\infty_1 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{array} \right]. \tag{30}$$

The grounded resistor realization of the above equation is shown in Fig. 9(a). The intrinsic nullor is realized with a nullator between nodes 2 and 3 and a norator between node 2 and ground, therefore this realization uses two nullors and was reported before in Refs. 2 and 3.

The second realization given is based on expansion type (ii) with $N = G_1$ and $D = -G_2$.

The Y expanded matrix is given by:

$$Y = \left[\begin{array}{ccc} 0 & 0 & 0 \\ \infty_1 & 0 & -\infty_1 \\ 0 & G_2 & G_1 \end{array} \right]. \tag{31}$$

Adding a fourth blank row and column and connect a norator between nodes 3 and 4 to move G_2 from the 3, 2 position to the 4, 2 position results in the following NAM:

$$Y = \left[\begin{array}{cccc} 0 & 0 & 0 & 0 \\ \infty_1 & 0 & -\infty_1 & 0 \\ 0 & 0 & G_1 & 0 \\ 0 & G_2 & 0 & 0 \end{array} \right]. \tag{32}$$

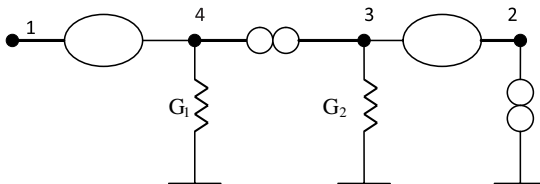


Fig. 9(a). Realization I of inverting VCVS using two nullors.²

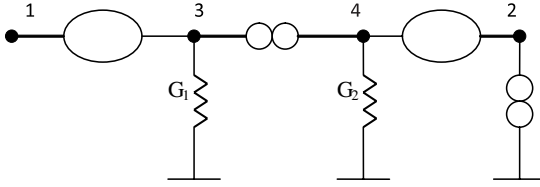


Fig. 9(b). Equivalent realization to Fig. 9(a).

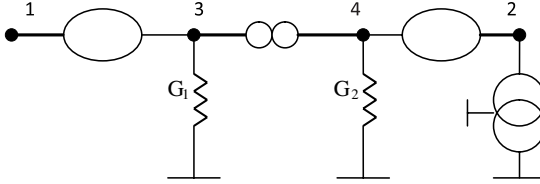


Fig. 9(c). Equivalent realization to Fig. 9(b).

A nullator is added next between nodes 2 and 4 to move G_2 to the diagonal position 4, 4 as follows:

$$Y = \left[\begin{array}{cccc} 0 & \overbrace{0} & 0 & 0 \\ \infty_1 & 0 & -\infty_1 & 0 \\ 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{array} \right]. \tag{33}$$

The grounded resistor realization of the above equation is shown in Fig. 9(b) which is equivalent to Fig. 9(a) except for the interchange of nodes 3 and 4.

Figure 9(c) represents a new equivalent realization to Fig. 9(b).

The second new realization is based on the new proposed NAM expansion number (i) in Table 2, which uses the two infinity terms with the same sign.

Taking $N = -G_1$ and $D = G_2$ resulting in the following Y expanded matrix:

$$Y = \left[\begin{array}{cccc} 0 & 0 & 0 & \\ 0 & \infty_1 & \infty_1 & 0 \\ -G_1 & 0 & G_2 & \end{array} \right]. \tag{34}$$

In this case the intrinsic element is represented by a VM between nodes 2 and 3 and a CM (or a norator) between node 2 and ground.

Adding a fourth blank row and column and connect a CM between nodes 3 and 4 to move $-G_1$ from the 3, 1 position to become G_1 in the 4, 1 position it follows that:

$$Y = \left[\begin{array}{cccc} 0 & 0 & 0 & 0 \\ 0 & \infty_1 & \infty_1 & 0 \\ 0 & 0 & G_2 & 0 \\ G_1 & 0 & 0 & 0 \end{array} \right]. \tag{35}$$

A nullator is added next between nodes 1 and 4 to move G_1 to the diagonal position 4, 4 as follows:

$$Y = \left. \begin{matrix} \overbrace{\begin{matrix} 0 & 0 & 0 & 0 \\ 0 & \infty_1 & \infty_1 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{matrix}} \\ \end{matrix} \right\} . \tag{36}$$

The grounded resistor realization of the above equation is shown in Fig. 10(a). This realization is based on representing the intrinsic element by a VM-CM pair. If the intrinsic element is represented however by a VM-norator pair Fig. 10(b) is obtained.

The third new realization is based on the new expansion type (ii) in Table 2 which uses the two infinity terms with the same sign. Taking $N = G_1$ and $D = -G_2$. The expanded matrix is given by:

$$Y = \begin{bmatrix} 0 & 0 & 0 \\ \infty_1 & 0 & \infty_1 \\ 0 & -G_2 & G_1 \end{bmatrix} . \tag{37}$$

Adding a fourth blank row and column and connect a CM between nodes 3 and 4 to move $-G_2$ from the position 3, 2 to become G_2 in the 4, 2 position thus:

$$Y = \left. \begin{matrix} \begin{matrix} 0 & 0 & 0 & 0 \\ \infty_1 & 0 & \infty_1 & 0 \\ 0 & 0 & G_1 & 0 \\ 0 & G_2 & 0 & 0 \end{matrix} \\ \end{matrix} \right\} . \tag{38}$$

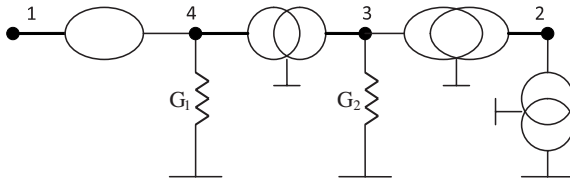


Fig. 10(a). Realization II-a of inverting VCVS.

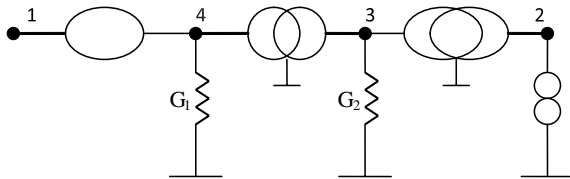


Fig. 10(b). Realization II-b of inverting VCVS.

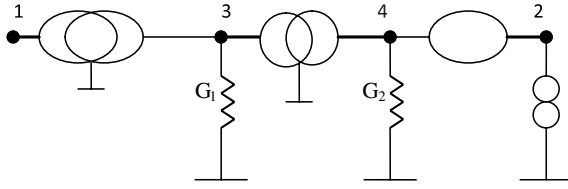


Fig. 10(c). Realization III-a of inverting VCVS.

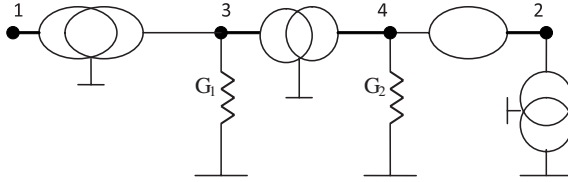


Fig. 10(d). Realization III-b of inverting VCVS.

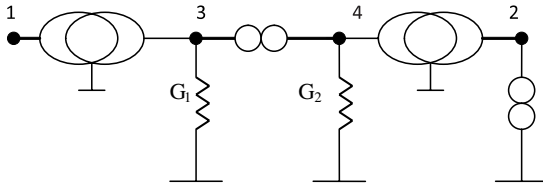


Fig. 10(e). Realization IV-a of inverting VCVS.

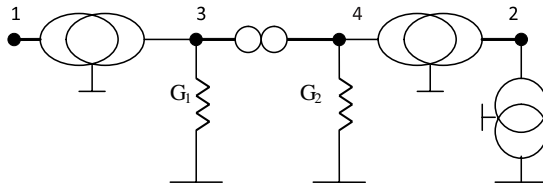


Fig. 10(f). Realization IV-b of inverting VCVS.

Adding a nullator between nodes 2 and 4 to move G_2 from the 4, 2 position to the diagonal position 4, 4 as follows:

$$Y = \left[\begin{array}{cccc} 0 & \overbrace{0 \quad 0} & 0 & 0 \\ \infty_1 & 0 & \infty_1 & 0 \\ 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{array} \right] . \quad (39)$$

Realizing the intrinsic element by a VM between nodes 1 and 3 and a norator between node 2 and ground results in realization III-a shown in Fig. 10(c).

If the intrinsic element however is realized by a VM-CM pair results in realization III-b shown in Fig. 10(d).

The next realization is also based on the new expansion (ii). Starting from Eq. (37) and adding a norator between nodes 3 and 4 it follows that:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ \infty_1 & 0 & \infty_1 & 0 \\ 0 & 0 & G_1 & 0 \\ 0 & -G_2 & 0 & 0 \end{bmatrix}. \tag{40}$$

Finally a VM is connected between nodes 2 and 4 to move G_2 to the diagonal position 4, 4 as follows:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ \infty_1 & 0 & \infty_1 & 0 \\ 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{bmatrix}. \tag{41}$$

The realizations IV-a, IV-b of the above equation based on the two alternative realizations of the intrinsic element are shown in Figs. 10(e) and 10(f).

Table 3 summarizes the grounded resistor pathological realizations of the VCVS.

Table 3. Summary of alternative grounded resistor VCVS realizations.

Circuit figure	Gain polarity	Nullator	Norator	VM	CM	Active blocks	Ref.
5(a), (b)	Positive	2	1	0	1	CCII+, CCII- (CFOA)	13,14
5(c)	Positive	2	0	0	2	Two CCII+	New
6(a)	Positive	1	1	1	1	CCII-, ICCII+	New
6(b)	Positive	1	2	1	0	CCII-, ICCII-	New
7(a)	Positive	1	1	1	1	ICCH-, CCII+	New
7(b)	Positive	1	2	1	0	ICCH-, CCII-	New
8(a)	Positive	0	0	2	2	Two ICCII+	New
8(b)	Positive	0	1	2	1	ICCH+, ICCII-	New
9(a), (b)	Negative	2	2	0	0	Two nullors (Two CCII-)	2,3
9(c)	Negative	2	1	0	1	CCII-, CCII+	New
10(a)	Negative	1	0	1	2	CCII+, ICCII+	New
10(b)	Negative	1	1	1	1	CCII+, ICCII-	New
10(c)	Negative	1	1	1	1	ICCH+, CCII-	New
10(d)	Negative	1	0	1	2	ICCH+, CCII+	New
10(e)	Negative	0	2	2	0	Two ICCH-	New
10(f)	Negative	0	1	2	1	ICCH-, ICCII+	New

4. Current Controlled Current Sources (CCCS)

The transmission matrix of the CCCS is given by Refs. 1–3:

$$T = \begin{pmatrix} 0 & 0 \\ 0 & \frac{1}{A_I} \end{pmatrix}. \tag{42}$$

The current gain $A_I = -I_2/I_1$ can be negative or positive. The polarity adopted for the current gain in this paper is the same as given in Ref. 1 which is the A_I (the negative of I_2/I_1 polarity with I_2 in the nominal direction being inward). For the negative gain CCCS three alternative nullor realizations are given in Ref. 1, two of them use floating resistors and the third one uses grounded resistors and was reported before in Ref. 2 without any generation method.

4.1. New NAM expansions for the CCCS

The types (i) and (ii) description of the admittance matrix Y for the CCCS are given in Table 4 together with the expanded 3×3 admittance matrices Ref. 1. New expanded 3×3 admittance matrices for types (i) and (ii) are introduced in the third column of Table 4. The proposed NAM has two identical infinities in the first column, this intrinsic element is realizable by a nullator (or VM)-CM pair.

The intrinsic element used in the new expansion of type (i) is represented by a nullator (or VM) between node 1 and ground and a CM between nodes 1 and 3. The intrinsic element used in the new expansion of type (ii) is represented by a nullator (or VM) between node 1 and ground and a CM between nodes 2 and 3.

4.2. Inverting A_I

Consider a CCCS with negative gain defined by:

$$A_I = -\frac{G_2}{G_1}. \tag{43}$$

Table 4. Admittance matrix description and its expansion for the CCCS.

Type	Admittance matrix	Expanded matrix	Ref.
(i)	$Y = \begin{bmatrix} \infty_1 & 0 \\ -\frac{N}{D}\infty_1 & 0 \end{bmatrix}$	$Y = \begin{bmatrix} \infty_1 & 0 & 0 \\ 0 & 0 & -N \\ -\infty_1 & 0 & D \end{bmatrix}$	1
		$Y = \begin{bmatrix} \infty_1 & 0 & 0 \\ 0 & 0 & N \\ \infty_1 & 0 & D \end{bmatrix}$	New
(ii)	$Y = \begin{bmatrix} -\frac{D}{N}\infty_1 & 0 \\ \infty_1 & 0 \end{bmatrix}$	$Y = \begin{bmatrix} 0 & 0 & -D \\ \infty_1 & 0 & 0 \\ -\infty_1 & 0 & N \end{bmatrix}$	1
		$Y = \begin{bmatrix} 0 & 0 & D \\ \infty_1 & 0 & 0 \\ \infty_1 & 0 & N \end{bmatrix}$	New

The first realization is based on expansion (i) and is shown in Fig. 11(a).^{1,2} Three new realizations of the negative gain CCCS using grounded resistors are given next.

The second realization is also based on using NAM expansion type (i) given by:

$$Y = \begin{bmatrix} \infty_1 & 0 & 0 \\ 0 & 0 & -N \\ -\infty_1 & 0 & D \end{bmatrix}. \tag{44}$$

Taking $N = -G_2$ and $D = G_1$ therefore:

$$Y = \begin{bmatrix} \infty_1 & 0 & 0 \\ 0 & 0 & G_2 \\ -\infty_1 & 0 & G_1 \end{bmatrix}. \tag{45}$$

Adding a fourth blank row and column and connect a CM between nodes 2 and 4 and a VM between nodes 3 and 4 are used to move G_2 to the diagonal position 4, 4 as follows:

$$Y = \left[\begin{array}{cccc} \infty_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -\infty_1 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{array} \right]. \tag{46}$$

Figure 11(b) represents the realization of the above equation.

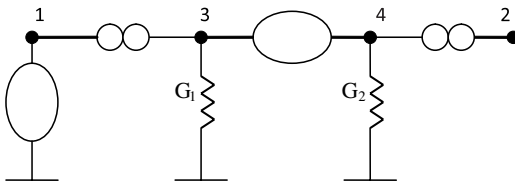


Fig. 11(a). Realization I of inverting CCCS.^{1,2}

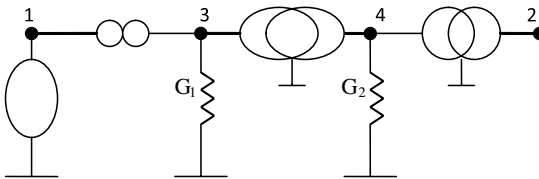


Fig. 11(b). Realization II of inverting CCCS.

The third realization is based on the new expansion type (i) given by:

$$Y = \begin{bmatrix} \infty_1 & 0 & 0 \\ 0 & 0 & N \\ \infty_1 & 0 & D \end{bmatrix}. \tag{47}$$

Taking $N = -G_2$ and $D = G_1$ therefore:

$$Y = \begin{bmatrix} \infty_1 & 0 & 0 \\ 0 & 0 & -G_2 \\ \infty_1 & 0 & G_1 \end{bmatrix}. \tag{48}$$

Adding a fourth blank row and column and connect CM between nodes 2 and 4 and a nullator between nodes 3 and 4 are used to move $-G_2$ to the diagonal position 4, 4 as follows:

$$Y = \left. \begin{bmatrix} \infty_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \infty_1 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{bmatrix} \right\}. \tag{49}$$

Figure 12(a) represents the realization of the above equation, with the intrinsic element realized by a CM between nodes 1 and 3 and a nullator between node 1 and ground.

The fourth realization is also based on new expansion type (i) with same choices for N and D as the previous case.

In this case however a VM between nodes 3 and 4 and a norator between nodes 2 and 4 are used to move $-G_2$ to the diagonal position 4, 4 as follows:

$$Y = \left. \begin{bmatrix} \infty_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \infty_1 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{bmatrix} \right\}. \tag{50}$$

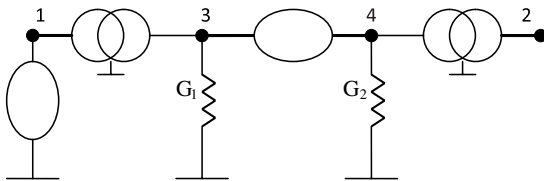


Fig. 12(a). Realization III of inverting CCCS.

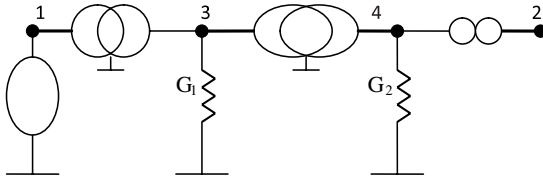


Fig. 12(b). Realization IV of inverting CCCS.

Figure 12(b) represents the realization of the above equation; with the intrinsic element realized as in the previous case by a CM between nodes 1 and 3 and a nullator between nodes 1 and ground.

4.3. Noninverting A_I

For the positive gain CCCS two alternative nullor realizations are given in Ref. 1, both of them use one floating resistor and one grounded resistor. The single nullor realization generated in Ref. 1 was reported before in Ref. 3. Four new grounded resistor CCCS are given next. Consider the current transfer function A_I given by:

$$A_I = \frac{G_2}{G_1}. \tag{51}$$

The first realization is based on NAM expansion type (i) Ref. 1 given by:

$$Y = \begin{bmatrix} \infty_1 & 0 & 0 \\ 0 & 0 & -N \\ -\infty_1 & 0 & D \end{bmatrix}. \tag{52}$$

Take $N = G_2$ and $D = G_1$, the NAM is given by:

$$Y = \begin{bmatrix} \infty_1 & 0 & 0 \\ 0 & 0 & -G_2 \\ -\infty_1 & 0 & G_1 \end{bmatrix}. \tag{53}$$

Adding a fourth blank row and column and connect CM between nodes 2 and 4 and a nullator between nodes 3 and 4 are used to move $-G_2$ to the diagonal position 4, 4 as follows:

$$Y = \left[\begin{array}{cccc} \infty_1 & 0 & \overbrace{0 \quad 0} & \\ 0 & 0 & 0 & 0 \\ -\infty_1 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{array} \right] . \tag{54}$$

Figure 13(a) represents the realization of the above equation.

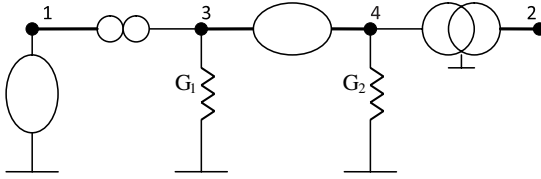


Fig. 13(a). Realization I of noninverting CCCS.

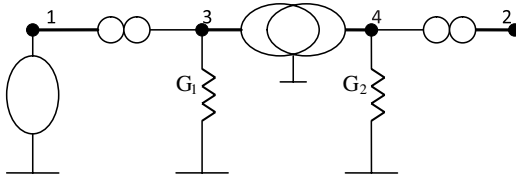


Fig. 13(b). Realization II of noninverting CCCS.

The second realization given is based also on expansion (i) with the same choice for N and D . From Eq. (53) and using a VM between nodes 3 and 4 and a norator between nodes 2 and 4 to move $-G_2$ to the diagonal position 4, 4 as follows:

$$Y = \left[\begin{array}{cccc} \infty_1 & 0 & \overbrace{0 \quad 0} & 0 \\ 0 & 0 & 0 & 0 \\ -\infty_1 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{array} \right]. \tag{55}$$

Figure 13(b) represents the realization of the above equation.

The third realization given is based on the new NAM expansion type (i) given in Table 4 which is given by:

$$Y = \begin{bmatrix} \infty_1 & 0 & 0 \\ 0 & 0 & N \\ \infty_1 & 0 & D \end{bmatrix}. \tag{56}$$

Take $N = G_2$ and $D = G_1$, the NAM is given by:

$$Y = \begin{bmatrix} \infty_1 & 0 & 0 \\ 0 & 0 & G_2 \\ \infty_1 & 0 & G_1 \end{bmatrix}. \tag{57}$$

Adding a fourth blank row and column and connect a VM between nodes 3 and 4 and a CM between nodes 2 and 4 to move G_2 to the diagonal position 4, 4 as follows:

$$Y = \left[\begin{array}{cccc} \infty_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \infty_1 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{array} \right] \cdot \quad (58)$$

Figure 14(a) represents the realization of the above equation.

The fourth realization given is based also on new NAM expansion type (i) with the same choice for N and D . From Eq. (57) and adding a fourth blank row and column and using a nullator between nodes 3 and 4 and a norator between nodes 2 and 4 to move G_2 to the diagonal position 4, 4 as follows:

$$Y = \left[\begin{array}{cccc} \infty_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \infty_1 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{array} \right] \cdot \quad (59)$$

Figure 14(b) represents the realization of the above equation.

It should be noted that all the controlled sources reported so far satisfy the ideality for the input and output impedances.

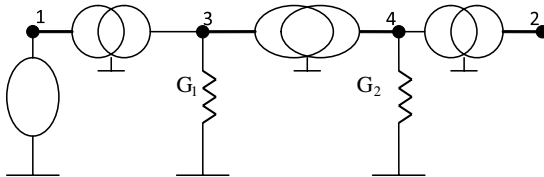


Fig. 14(a). Realization III of noninverting CCCS.

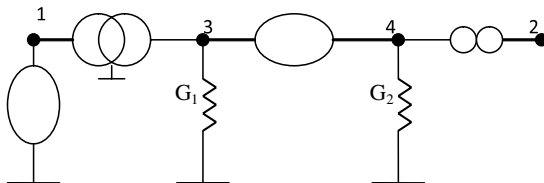


Fig. 14(b). Realization IV of noninverting CCCS.

Table 5. Summary of alternative grounded resistor CCCS realizations.

Circuit figure	Gain polarity	Nullator	Norator	VM	CM	Active blocks	Ref.
11(a)	Negative	2	2	0	0	Two nullors (Two CCII-)	1
11(b)	Negative	1	1	1	1	CCII-, ICCII+	New
12(a)	Negative	2	0	0	2	Two CCII+	New
12(b)	Negative	1	1	1	1	CCII+, ICCII-	New
13(a)	Positive	2	1	0	1	CCII-, CCII+	New
13(b)	Positive	1	2	1	0	CCII-, ICCII-	New
14(a)	Positive	1	0	1	2	CCII+, ICCII+	New
14(b)	Positive	2	1	0	1	CCII+, CCII-	New

5. Controlled Sources Using Single Building Block

The single nullor-inverting CCVS shown in Fig. 15 employ a single floating resistor and is practically realizable using a single Op Amp.^{1,3} It satisfies the zero input impedance and the low output impedance which are necessary for an ideal CCVS.

The single nullor positive gain VCVS shown in Fig. 16(a) employs one grounded resistor and one floating resistor and is practically realizable using a single Op Amp.^{1,3} It satisfies the infinite input impedance and the low output impedance which are necessary for an ideal VCVS.

If the requirement for ideality of the input or output impedance is relaxed, simple circuits employing a single building block can be generated for VCVS and CCCS and are summarized in Table 6. As an example the well known single nullor negative gain VCVS shown in Fig. 16(d) employ two floating resistors and is not ideal since its input impedance is finite. Similarly the CCCS shown in Fig. 17(a),

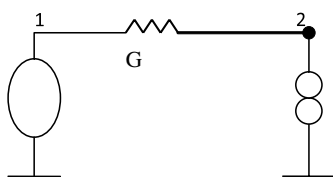


Fig. 15. Single nullor inverting CCVS.^{1,3}

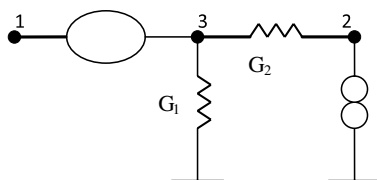


Fig. 16(a). Single nullor noninverting VCVS.^{1,15,16}

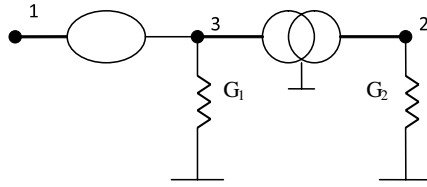


Fig. 16(b). Single CCII+ noninverting VCVS.

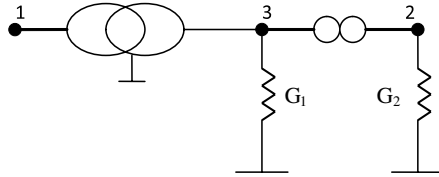


Fig. 16(c). Single ICCII- noninverting VCVS.

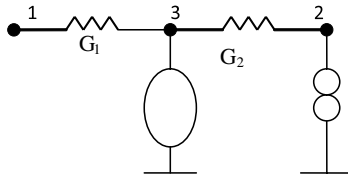


Fig. 16(d). Non-ideal single nullor inverting VCVS.¹

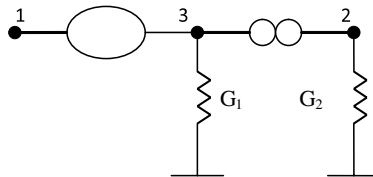


Fig. 16(e). Non-ideal single CCII- inverting VCVS.¹⁸

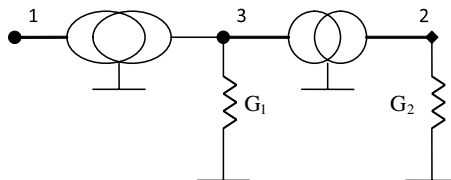


Fig. 16(f). Non-ideal single ICCII+ inverting VCVS.

Table 6. Single building block CCVS, VCVS and CCCS realizations.

Circuit figure	Type	Gain a polarity	Nullator	Norator	VM	CM	Active block	Ref.
15	CCVS	Negative	1	1	0	0	Nullor	1, 3
16(a)	VCVS	Positive	1	1	0	0	Nullor	1, 15, 16
16(b)	VCVS	Positive	1	0	0	1	CCII+	14, 18
16(c)	VCVS	Positive	0	1	1	0	ICCH-	New
16(d)	VCVS	Negative	1	1	0	0	Nullor	1
16(e)	VCVS	Negative	1	1	0	0	CCII-	18
16(f)	VCVS	Negative	0	0	1	1	ICCH+	New
17(a)	CCCS	Negative	1	1	0	0	Nullor	1
17(b)	CCCS	Negative	1	0	0	1	OMA	New
17(c)	CCCS	Negative	1	1	0	0	CCII-	New
17(d)	CCCS	Negative	0	0	1	1	ICCH+	New
17(e)	CCCS	Positive	1	1	0	0	Nullor	1
17(f)	CCCS	Positive	1	0	0	1	CCII+	New
17(g)	CCCS	Positive	0	1	1	0	ICCH-	New

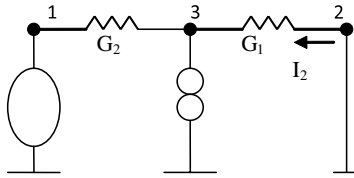


Fig. 17(a). Non-ideal single nullor inverting CCCS.¹

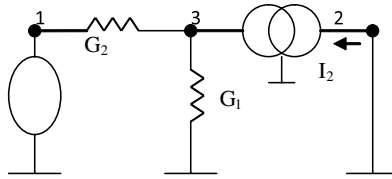


Fig. 17(b). Non-ideal single OMA inverting CCCS.

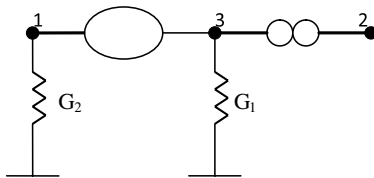


Fig. 17(c). Non-ideal single CCII- inverting CCCS.

which is based on imposing the condition $V_2 = 0$ by the load,¹ and is shown here with a shorted output. Therefore the desirable infinite output impedance for the ideal CCCS is not achieved by this CCCS, so it is identified here as a non-ideal CCCS.

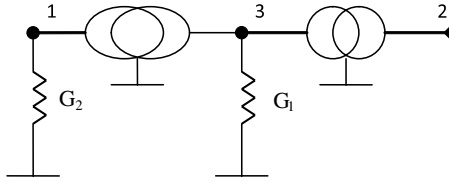


Fig. 17(d). Non-ideal single ICCII+ inverting CCCS.

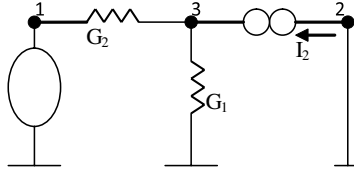


Fig. 17(e). Non-ideal single nullor noninverting CCCS.¹

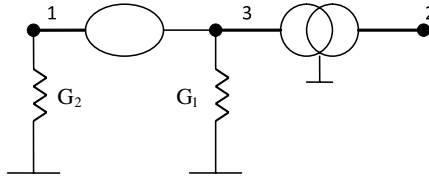


Fig. 17(f). Non-ideal single CCII+ noninverting CCCS.

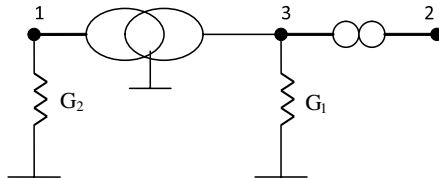


Fig. 17(g). Non-ideal single ICCII- noninverting CCCS.

Next generation of some of the non-ideal single building block controlled sources are discussed.

For VCVS if the requirement of low output impedance is relaxed on the account of the VCVS being loaded at port 2 by a high impedance such as port 1 of another VCVS, then the Y matrix can be simplified as follows:

$$Y = \begin{bmatrix} 0 & 0 \\ -N & D \end{bmatrix}. \tag{60}$$

For a positive gain VCVS take $N = G_1$ and $D = G_2$ therefore:

$$Y = \begin{bmatrix} 0 & 0 \\ -G_1 & G_2 \end{bmatrix}. \tag{61}$$

Adding a third blank row and column and use a CM between nodes 2 and 3 to move $-G_1$ to the 3, 1 position, it follows that:

$$Y = \left[\begin{array}{ccc} 0 & 0 & 0 \\ 0 & G_2 & 0 \\ G_1 & 0 & 0 \end{array} \right] . \tag{62}$$

Adding a nullator between nodes 1 and 3 to move the G_1 to the diagonal position 3, 3 it follows that:

$$Y = \left[\begin{array}{ccc} \overbrace{0 & 0 & 0} \\ 0 & G_2 & 0 \\ 0 & 0 & G_1 \end{array} \right] . \tag{63}$$

The VCVS is shown in Fig. 16(b) which is practically realizable by a single CCII+¹⁷ as given in Refs. 14 and 18.

An alternative expansion for Y in Eq. (61) is possible using a VM between nodes 1 and 3 and a norator between nodes 2 and 3 as follows:

$$Y = \left[\begin{array}{ccc} \overbrace{0 & 0 & 0} \\ 0 & G_2 & 0 \\ 0 & 0 & G_1 \end{array} \right] . \tag{64}$$

The new VCVS realization using ICCII– is shown in Fig. 16(c).

The generation of the floating resistor inverting VCVS of Fig. 16(d) using a single nullor was given in Ref. 1. Single CCII– and ICCII+ grounded resistor realizations are given next.

For a negative gain VCVS and from Eq. (61) and taking $N = -G_1$ and $D = G_2$ therefore:

$$Y = \begin{bmatrix} 0 & 0 \\ G_1 & G_2 \end{bmatrix}. \tag{65}$$

Adding a third blank row and column and use a nullator between nodes 1 and 3 and a norator between nodes 2 and 3 to move the G_1 to the diagonal position 3, 3 it follows that:

$$Y = \left[\begin{array}{ccc} \overbrace{0 & 0 & 0} \\ 0 & G_2 & 0 \\ 0 & 0 & G_1 \end{array} \right] . \tag{66}$$

The well known grounded resistor inverting VCVS realization using CCII⁻¹⁸ is shown in Fig. 16(e).

From Eq. (65) adding a VM between nodes 1 and 3 and a CM between nodes 2 and 3 to move the G_1 to the diagonal position 3, 3 it follows that:

$$Y = \left[\begin{array}{ccc} 0 & 0 & 0 \\ 0 & G_2 & 0 \\ 0 & 0 & G_1 \end{array} \right] \cdot \quad (67)$$

This is realizable by a single ICCII⁺ as shown in Fig. 16(f).

Several realizations for the CCCS are given in Fig. 17. Figure 17(b) represents a new realization of the inverting CCCS using operational mirror amplifier.¹⁹

To demonstrate the relation between VCVS and CCCS based on the adjoint theorem.^{20,21} Table 7 is given which includes four VCVS and their adjoint CCCS.

6. Floating Controlled Sources

It is of interest to notice that some of the reported controlled sources have a zero grounded current indicating that the controlled source has a floating nature. To demonstrate this property, consider the CCCS realization of Fig. 11(a) which uses two nullators and two norators. The circuit is shown in Fig. 18 using two CCII⁻. The source current and the load current must be taken into consideration in examining the floatation property of the circuit. It is seen that by using KCL, the current I_G equals to zero.

Other circuits reported in this paper and having a floating property are shown in Figs. 3(a) and 4(d) for CCVS. For VCVS, Figs. 6(b), 7(b), 9(a), 9(b) and 10(e) represent floating VCVS. The floating CCCS are shown in Figs. 11(a) and 13(b). Among the single building block controlled sources, controlled sources shown in Figs. 15, 16(c), 16(e), 17(c), 17(e) and 17(g) are floating.

7. Applications

Two examples of a voltage mode and a current mode filter using alternative types of VCVS and CCCS are given next. For a fair comparison the different types of current conveyors are realized using the same CMOS circuit. The generalized CMOS circuit realizing both types of CCII and of ICCII is shown in Fig. 19.²² The CCII is obtained by using Y_1 as the Y input and grounding Y_2 , on the other hand the ICCII is obtained by using Y_2 as the Y input and grounding Y_1 .

The transistor aspect ratios are given in Table 8 based on the $0.5 \mu\text{m}$ CMOS model from MOSIS. The supply voltages used are $\pm 1.5 \text{ V}$ and $V_{B1} = -0.52 \text{ V}$ and $V_{B2} = 0.33 \text{ V}$.

Table 7. Single current conveyor VCVS and CCCS as adjoint to each other.

Circuit	VCVS	CCCS
1	<p>$A_V = G_1/G_2$</p>	<p>$A_1 = G_1/G_2$</p>
2	<p>$A_V = G_1/G_2$</p>	<p>$A_1 = G_1/G_2$</p>
3	<p>$A_V = -G_1/G_2$</p>	<p>$A_1 = -G_1/G_2$</p>
4	<p>$A_V = -G_1/G_2$</p>	<p>$A_1 = -G_1/G_2$</p>

7.1. Sallen–Key voltage mode highpass filter

Figure 20(a) represents the well known Sallen–Key highpass filter² with the non-inverting VCVS realized using two ICCII+ as given in Fig. 8(a). Using equal R equal C design and for $Q = 0.707$ and f_o of 1 MHz, the circuit parameters are obtained as

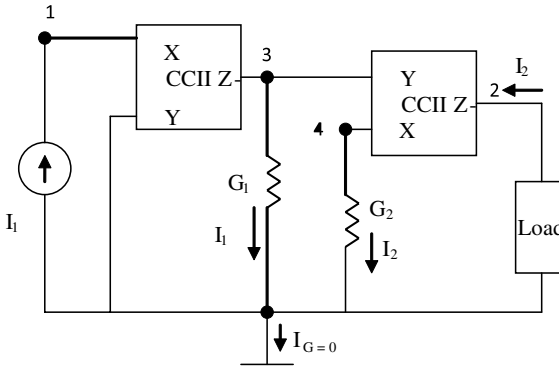


Fig. 18. Two CCII- realization of the CCCS of Fig. 11(a).

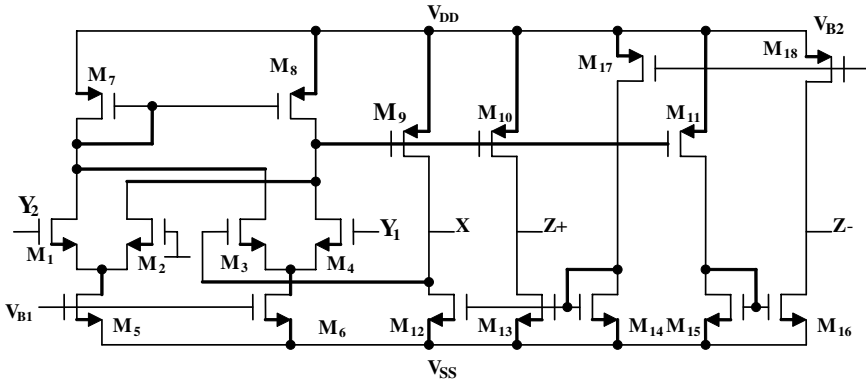


Fig. 19. The generalized CMOS current conveyor circuit.

Table 8. Transistor aspect ratios of the generalized conveyor of Fig. 19.

NMOS transistors	$W(\mu\text{m})/L(\mu\text{m})$
M_1, M_2, M_3, M_4	8/1
M_5, M_6	8/1
$M_{12}, M_{13}, M_{14}, M_{15}, M_{16}$	20/2.5
PMOS transistors	$W(\mu\text{m})/L(\mu\text{m})$
M_7 and M_8	10/1
$M_9, M_{10}, M_{11}, M_{17}, M_{18}$	40/2

follows: $R_1 = R_2 = 10 \text{ k}\Omega$, $C_1 = C_2 = 15.9 \text{ PF}$ and gain of the VCVS = 1.586. Taking $R_3 = 10 \text{ k}\Omega$, therefore $R_4 = 15.86 \text{ k}\Omega$. Figure 20(b) represents the simulated magnitude and phase responses of the highpass filter. The simulated results are very close to the ideal responses as shown in Fig. 20(b).

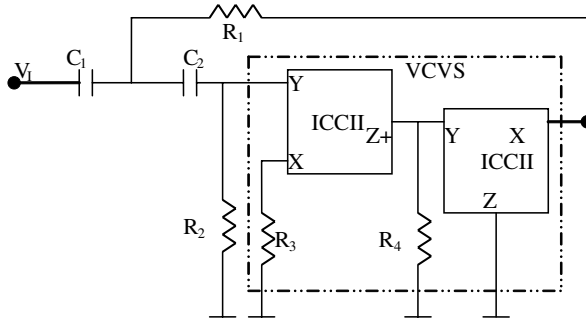


Fig. 20(a). Sallen–Key highpass filter using noninverting VCVS.

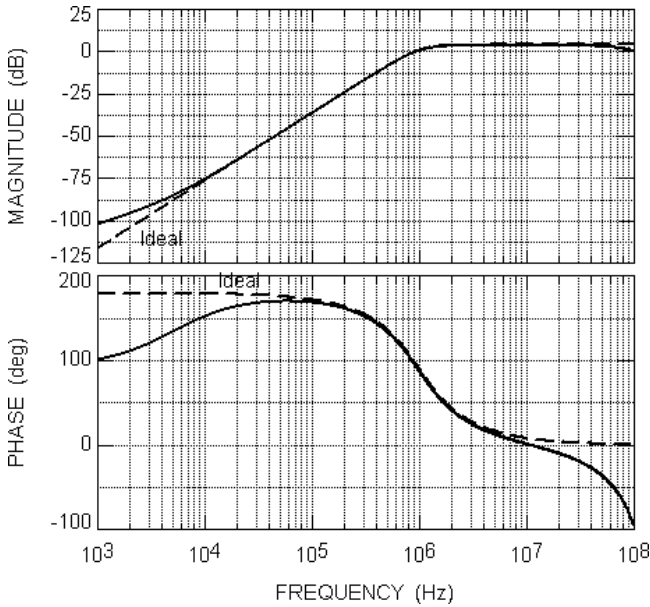


Fig. 20(b). Simulation results of Sallen–Key highpass filter using VCVS of Fig. 8(a).

The same highpass filter is simulated with the VCVS given in Fig. 6(a) which uses CCII– and ICCII+ and the simulation results which is in good agreement with the theoretical one is shown in Fig. 20(c). The same highpass filter is simulated with the VCVS given in Fig. 5(c) which uses two CCII+ and the simulation results which is in good agreement with the theoretical one is shown in Fig. 20(d).

From the simulations it is seen that the three alternative realizations of noninverting VCVS that are used provide results that are very close to the ideal responses.

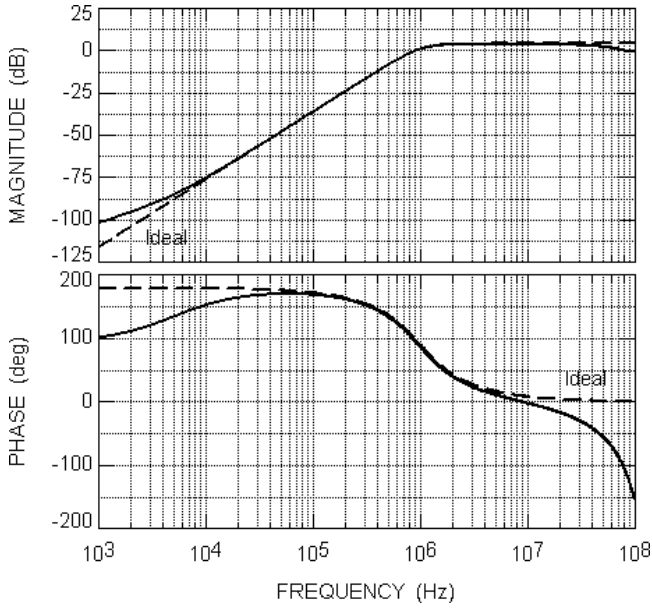


Fig. 20(c). Simulation results of Sallen–Key highpass filter using VCVS of Fig. 6(a).

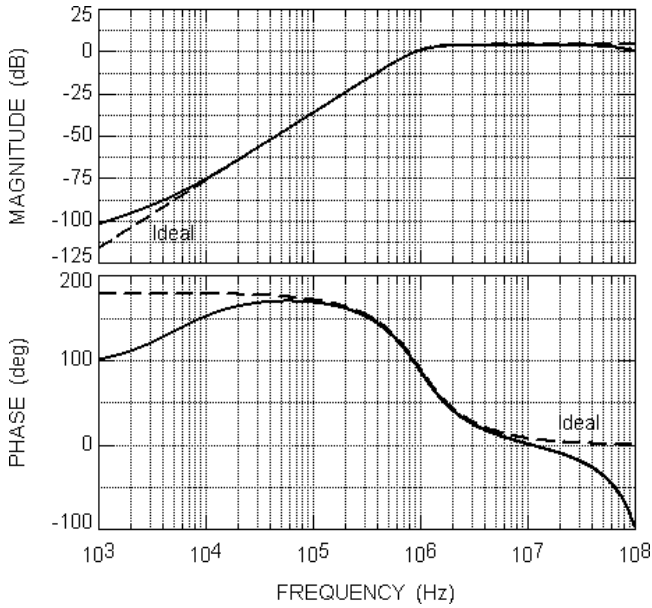


Fig. 20(d). Simulation results of Sallen–Key highpass filter using VCVS of Fig. 5(c).

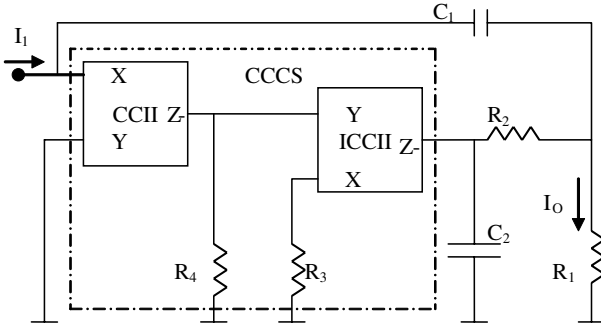


Fig. 21(a). Current mode Sallen–Key lowpass filter using CCCS.

7.2. Sallen–Key current mode lowpass filter

Figure 21(a) represents the Sallen–Key current mode lowpass filter obtained from the well known voltage mode lowpass filter² using the adjoint network theorem.^{20,21} The noninverting CCCS is realized using a CCII– and ICCII– as given in Fig. 13(b). Using equal R equal C design and for $Q = 0.707$ and f_0 of 1 MHz, the circuit parameters are obtained as follows:

$R_1 = R_2 = 10\text{ k}\Omega$, $C_1 = C_2 = 15.9\text{ PF}$ and gain of the CCCS = 1.586. Taking $R_3 = 10\text{ k}\Omega$, therefore $R_4 = 15.86\text{ k}\Omega$. Figure 21(b) represents the simulated magnitude and phase responses of the lowpass filter. The simulated results are very close to the ideal responses as shown in Fig. 21(b).

The same lowpass filter is simulated with the CCCS given in Fig. 14(b) which uses CCII+ and CCII– and the simulation results which is in good agreement with the theoretical one is shown in Fig. 21(c).

8. Conclusions

The admittance matrix expansion method based on using nullors and pathological mirror elements is used to provide a systematic synthesis method of controlled sources. It is pointed out that the use of the nullor as the intrinsic element in the NAM expansion represents a special case from four possible intrinsic elements. The intrinsic elements are the nullor, VM-CM pair, nullator-CM pair and the VM-norator pair. Four new realizations of the current controlled voltage source (CCVS) using a single grounded resistor are given. Eight new realizations for the noninverting voltage controlled voltage source (VCVS) using two grounded resistors are given. Three new nodal matrix expansions (NAM) for the VCVS are introduced in this paper. The voltage mirror current mirror pair is used as intrinsic element in the NAM expansion. Seven new realizations for the inverting VCVS using two grounded resistors are given thus completing the set of eight circuits since one realization was reported before in the literature.^{2,3} Seven new realizations for the CCCS using two

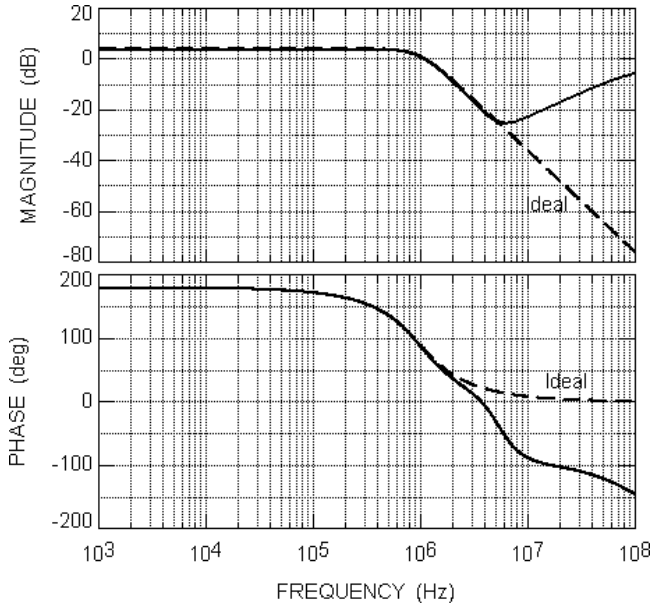


Fig. 21(b). Simulation results of current mode lowpass filter using CCCS of Fig. 13(b).

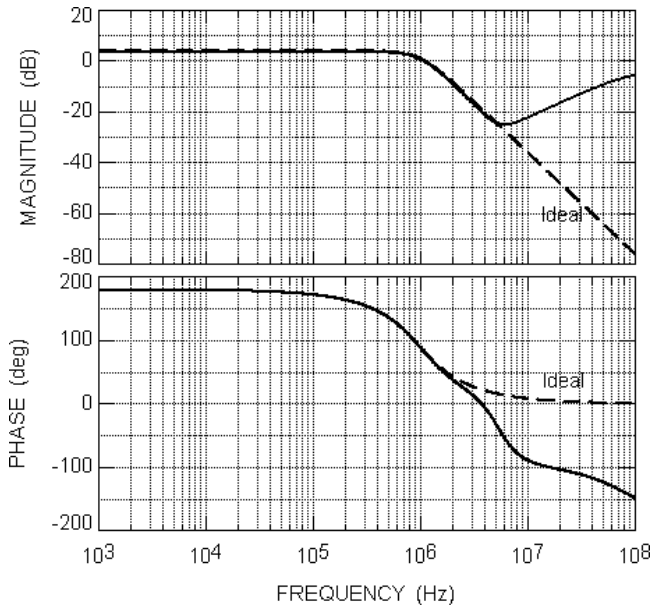


Fig. 21(c). Simulation results of current mode lowpass filter using CCCS of Fig. 14(b).

grounded resistors are given thus completing the set of eight circuits since one realization was reported before in the literature.^{1,2} The single building blocks controlled sources are summarized in Table 6 and some of the circuits are new. Table 7 summarizes the adjoint relation between the VCVS and the CCCS. The floatation property of some of the reported controlled sources is discussed.

Example of a voltage mode highpass filter using three different realizations of the noninverting VCVS are included. From the simulations it is seen that the three alternative realizations of noninverting VCVS that are used provide results that are very close to the ideal responses.

A second example of a current mode lowpass filter using two different realizations of the noninverting CCCS are included. From the simulations it is seen that the two alternative realizations of noninverting CCCS that are used provide results that are very close to the ideal responses.

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