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LETTER

A modified CMOS differential operational transresistance amplifier (OTRA)

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Abstract

A modified CMOS realization of the differential operational transresistance amplifier (OTRA) is presented. A fair comparison with Mostafa and Soliman OTRA [Mostafa H, Soliman A. A modified CMOS realization of the operational transresistance amplifier. Frequenz 2006;60:70–6] shows that the modified differential OTRA provides better performance in most parameters. The OTRA is suitable for analog VLSI applications since it does not suffer from constant gain bandwidth product. Hence, it can exhibit wide bandwidth at high gain values. Moreover, an OTRA-based variable gain amplifier (VGA) is also introduced.

Keywords: CMOS operational transresistance amplifier; Analog VLSI applications; Variable gain amplifier; Wireless communications

1. Introduction

Recently, great interest has been devoted to the design of the operational transresistance amplifiers (OTRAs) [1–3]. This great interest is mainly because the OTRA is not slew limited in the same fashion as voltage op amps. It can provide a high bandwidth independent of the gain. Hence, it does not suffer from constant gain bandwidth product like voltage op amps circuits.

The OTRA is a three-terminal analog building block that is defined by the following matrix equation:

$$\begin{bmatrix} V_+ \\ V_- \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_+ \\ I_- \\ I_o \end{bmatrix} \quad (1)$$

where R_m is the transresistance gain.

The block diagram of the OTRA is shown in Fig. 1. The input terminals are virtually grounded, leading to circuits that are insensitive to stray capacitances. Ideally the transresistance gain R_m approaches infinity and applying external negative feedback will force the two input currents, I_+ and I_- to be equal.

In the next section of this paper a novel large open loop transresistance gain and high gain bandwidth product differential OTRA is proposed. The CMOS model for all circuits is identical. The transistor model is 0.25 μm CMOS process provided by MOSIS (AGILENT).

2. The proposed modified differential OTRA

2.1. Circuit description

The CMOS realization of the proposed high open loop gain differential OTRA is shown in Fig. 2. It is based on the same input stage of the Mostafa and Soliman OTRA proposed in [1] while a differential gain stage is used instead of

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the single common source amplifier. The transistors Mx4–Mx7 produce the non-inverting output, while the transistors My4–My7 produce the inverting output. It is clear that the differential gain stage added has reduced the DC offset current and increased the DC open loop transresistance gain.

2.2. Simulation results

Transistors aspect ratios are reported in Table 1. The biasing current IB = 29.1 μA. The biasing voltage VB1 = −0.9018 V simulation results are tabulated in Table 2 and shown in Figs. 3 and 4. These results can be described as follows. The input differential current range is from −50 to 50 μA (Fig. 3). The offset current equals 0.1 μA.

The differential input resistance is similar to realization proposed in [1], which equals 26.07 kΩ. The DC open loop transresistance gain equals 163.2 dBΩ(=144 MΩ) (Fig. 4). The gain bandwidth product equals 57 600 GHz Ω (Fig. 4). The power dissipation of the circuit equals 0.82 mW.

The advantage of the proposed modified differential OTRA circuit shown in Fig. 2 is proved by the comparison in Table 2. It is clear that the proposed OTRA provides less offset current and also OTRA exhibits more DC open loop transresistance gain and more gain bandwidth product than the realization in [1].

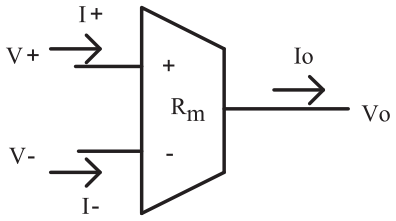

Fig. 1. Block diagram of the OTRA.

3. OTRA-based digitally controlled voltage mode (VGA)

3.1. Introduction

Variable gain amplifiers (VGAs) are used in many applications in order to maximize the dynamic range of the overall system. Disk drivers [4,5] and wireless communications are examples of such systems.

In wireless communication systems, the received signal has a very wide dynamic range; so an automatic gain control (AGC) has to be used. Its function is to automatically adjust the gain of the receive path so that the signal processed by the baseband section circuitry appears to be at a constant level, regardless of the actual signal strength received at the antenna.

The AGC contains a VGA which is used to adjust the gain of the AGC. In modern wireless systems, the VGA has to be digitally controlled to avoid the use of DAC in the AGC loop. The gain of VGA should increase linearly on the decibel scale in order to achieve a wide gain control. Although traditional VGA topologies based on high open loop gain op amps or operational transconductance amplifiers (OTAs) provide good results, they suffer from slew rate limitations and finite gain bandwidth product.

Table 1. Transistors aspect ratios of the circuit shown in Fig. 2

Transistors	W (μm)	L (μm)
M1–M3	30	1.25
M4	10	1.25
M5, M6	30	1.25
M8–M11	90	1.25
M12, M13	90	1.25
Mx4, Mx5	5.25	0.25
My4, My5	0.25	0.25
Mx6, Mx7, My6 and My7	0.25	1.25

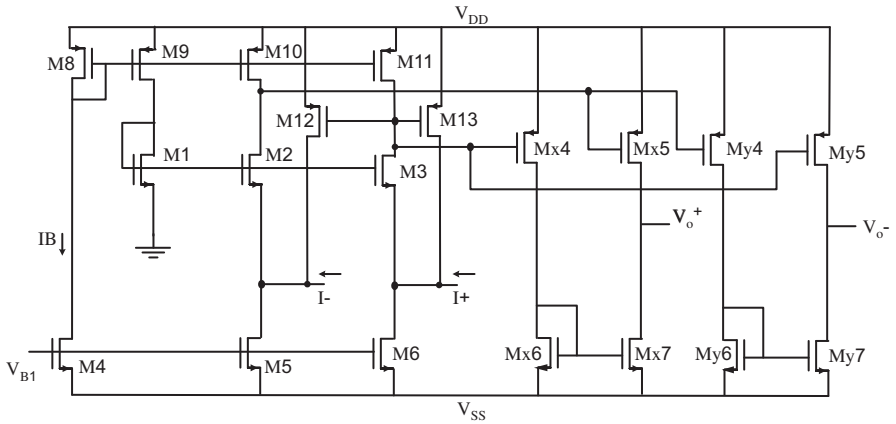

Fig. 2. The proposed modified differential OTRA.

Table 2. Performance comparison of the proposed differential OTRA and OTRA presented in [1]

Parameters	OTRA proposed in [1]	Proposed differential OTRA
Power supply (VDD, VSS)	1.5 V, −1.5 V	1.5 V, −1.5 V
No. of transistors	14	20
Total power dissipation	0.709 mW	0.82 mW
PSRR+	90.2 dB Ω	186.8 dB Ω
PSRR−	97.3 dB Ω	150.1 dB Ω
Input current dynamic range	−50 to 50 μA	−50 to 50 μA
Offset current	0.3 μA	0.1 μA
DC open loop transresistance gain	130 dB Ω	163.2 dB Ω
Gain bandwidth product	3.16 THz Ω	57.6 THz Ω
Transresistance gain B.W. (−3 dB)	1 MHz	0.4 MHz
Rise time/fall time (at 1 MHz,1 V p–p)	0.023/1.74 ns	0.025/1.1 ns

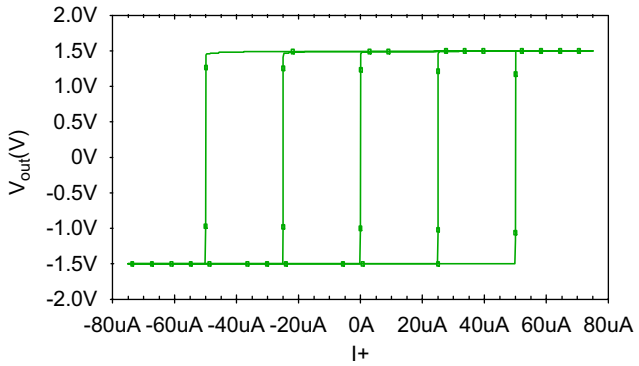

Fig. 3. The output voltage (V_{o+}) of the circuit shown in Fig. 2.

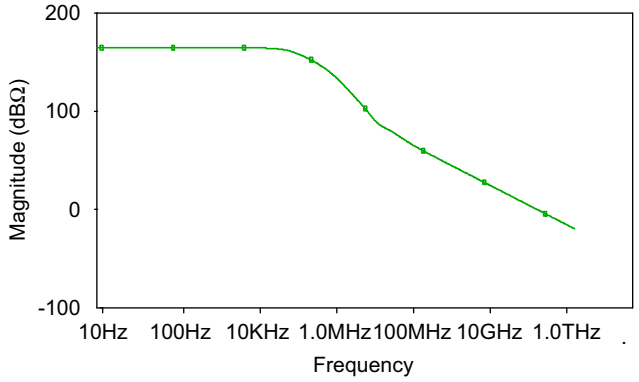

Fig. 4. Frequency characteristics of the open loop transresistance gain for the circuit shown in Fig. 2.

Third-generation wireless communication systems utilize wide band code division multiple access (WCDMA) techniques [3]. Thus the transmitted signal is to be spread over a wider range of bandwidth. It is thus necessary to investigate new CMOS amplifier-based VGA structures that is not slew limited and also can provide large bandwidth independent of the gain. This can be done by using the OTRA-based voltage-mode digitally controlled VGA.

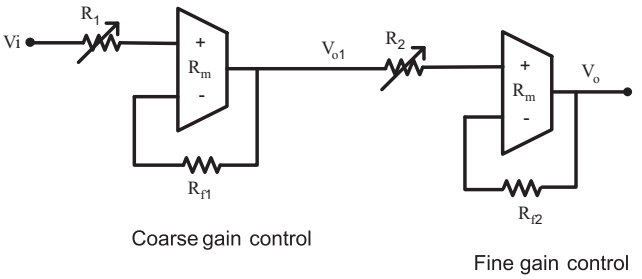

Fig. 5. The voltage-mode digitally controlled VGA.

3.2. Circuit description

The voltage-mode digitally controlled VGA configuration is shown in Fig. 5. The VGA circuit is operating in a coarse and fine arrangement. It consists of two stages. The first stage represents a coarse gain control stage. The second stage represents a fine gain control stage.

Taking the effect of finite transresistance gain R_m and using the single pole model, the transresistance gain is given by

$$R_m(s) = \frac{R_{mo}}{1 + s/\omega_0} \tag{2}$$

where R_{mo} is the DC open loop transresistance gain and ω_0 is the transresistance cutoff frequency. For high-frequency applications, the transresistance gain $R_m(s)$ may be expressed as

$$R_m(s) = \frac{1}{sC_p} \tag{3}$$

where

$$C_p = \frac{1}{R_{mo}\omega_0} \tag{4}$$

Hence, the voltage gain of the first stage is given by

$$\frac{v_{o1}}{v_{in}} = \frac{R_{f1}}{R_1}\frac{1}{1 + sR_{f1}C_p} \tag{5}$$

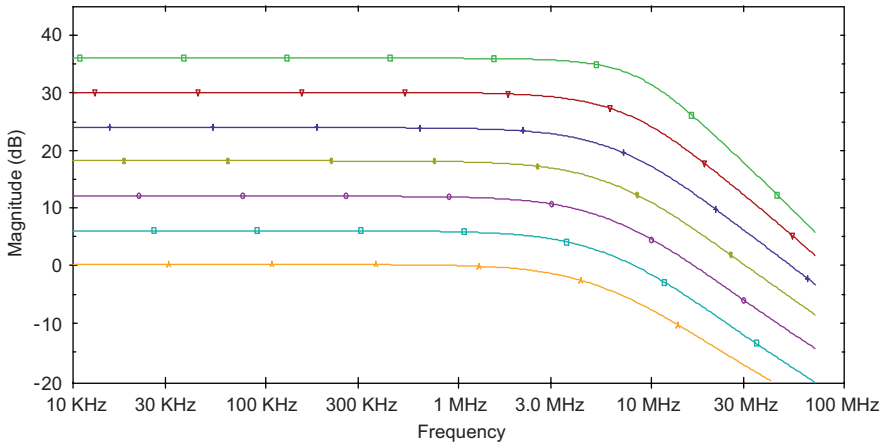

Fig. 6. Frequency characteristics of the first stage of the voltage-mode digitally controlled VGA for different gains from 0 to 36 dB with 6-dB gain step.

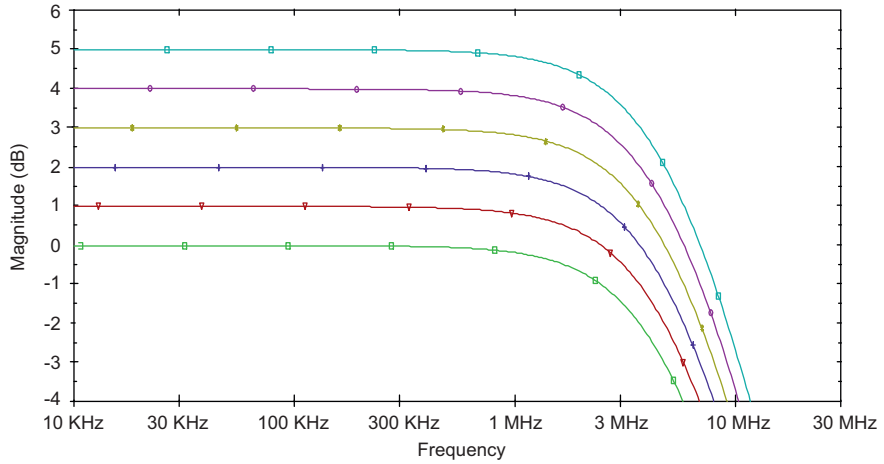

Fig. 7. Frequency characteristics of the second stage of the voltage-mode digitally controlled VGA for different gains from 0 to 5 dB with 1-dB gain step.

And the voltage gain of the second stage is given by

$$\frac{v_o}{v_{o1}} = \frac{R_{f2}}{R_2}\frac{1}{1+sR_{f2}C_p} \tag{6}$$

where R_{f1} and R_{f2} are the feedback resistors of the first and second stages, respectively. It is clear from Eq. (5) that the gain of the first stage can be varied independently of the bandwidth by changing the resistance R_1 and from Eq. (6) that the gain of the second stage can be varied independently of the bandwidth by changing R_2. The first stage operates in a 6-dB step (coarse gain control), while the second VGA stage provides the precise 1-dB gain stepping (fine gain control).

The digital control structure of the resistors R_1 and R_2 is similar to the structure given in [6].

3.3. Simulation results

The voltage-mode digitally controlled VGA is simulated using $R_{f1}=64\,k\Omega$ and $R_{f2}=20\,k\Omega$. Fig. 6 shows the different gains of the first stage ranging from 0 to 36 dB with a 6-dB gain step. Fig. 7 shows the different gains of the second stage ranging from 0 to 5 dB, with a 1-dB gain step. Fig. 8 shows the different gains of the overall VGA circuits ranging from 6 to 41 dB with a 6-dB gain step.

It is clear that the bandwidth is about 21 MHz for the maximum gain of 41 dB. The average gain error is about 0.25 dB. The power dissipation of the circuit is about 1.59 mW.

4. Conclusion

This paper presents a modified CMOS realization of the differential operational transresistance amplifier and its application. Simulation results and a fair comparison between the proposed modified differential OTRA and OTRA given in [1] proved the strength of the proposed realization. Digitally controlled voltage-mode variable gain amplifier (VGA) based on the proposed realization is also introduced.

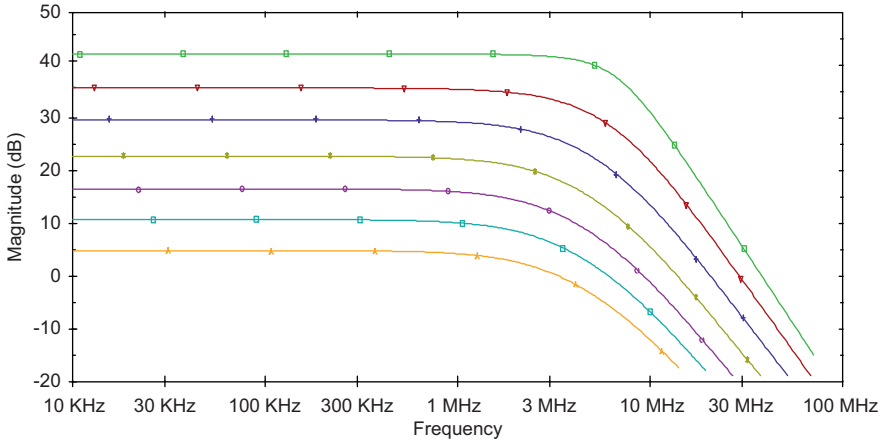

Fig. 8. Frequency characteristics of the overall voltage-mode digitally controlled VGA for different gains from 5 to 41 dB with 6-dB gain step.

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