A Comparative Study of the Voltage-to-Time Converters (VTCs) and the Voltage-to-Frequency Converters (VFCs) Circuits

Mohammed A. ElGabry
Electronics and
Electrical Communication Engineering
Cairo University
Giza, Egypt
Email: maelgabry@outlook.com

Hassan Mostafa
Electronics and
Electrical Communication Engineering
Cairo University
Giza, Egypt
Email: hmostafa@uwaterloo.ca

Ahmed M. Soliman
Electronics and
Electrical Communication Engineering
Cairo University
Giza, Egypt
Email: asoliman@ieee.org

***Abstract*—Nowadays ADC becomes more essential in emerging applications. ADC is starting to become hindrance to the system in the performance and the power consumption. For high-speed applications, pipelined and flash ADC has dominantly been used over the past decade. Technology scaling and the focus on digital systems with high-performance offer better time resolution by decreasing the gate delay. If the input analog voltage signal is represented in the form of time or frequency, rather than voltage, we can make use of the scaled technologies, low power consumption and die area. Time based ADC (TADC) is different from conventional ADC, because the signal is represented in the form of a stream of series time events. This architecture places the ADC at the front end to create more complex digital circuits for low power applications, and low voltage design. Simulation results show that Voltage-to-Frequency converter (VFC) circuit is better than Voltage-to-Time converter (VTC) circuit in the sensitivity, signal to noise and distortion ratio, effective number of bits, and maximum input frequency, while VTC is better than VFC with respect to the power consumption. VFC is better to be used with the applications that require high input frequency, while VTC is better to be used in applications that require low power consumption.**

I. Introduction

The rapidly evolving capabilities of digital electronic makes software defined radio "SDR" concept very important nowadays. SDR is a radio communication system where components that have been typically implemented in hardware (i.e., filters, amplifiers, modulators / demodulators, detectors, etc.) are implemented by using software instead. A basic SDR system consists of a digital processing module equipped with ADC, preceded by some form of RF front end. The ultimate objective receiver design would be to connect an ADC to an antenna directly.

A digital signal processing (DSP) module reads the converter, and then its software would convert the obtained data stream from the converter to any other form the application requires. The ideal scheme is not completely reachable due to the actual technology limits. The main dilemma is the difficulty of conversion between the digital and the analog domains at a high enough rate and a high enough accuracy concurrently, and without depending upon physical processes like interference and electromagnetic resonance.

Therefore, if we represent a signal in the form of time or frequency, rather than voltage, we can take the benefits of technology scaling, high speed, low power consumption and low die area.

TADC is composed of two parts: the first part is converting the voltage to time using voltage to time converter (VTC) circuit and the second part is converting this time to digital using time to digital converter (TDC) circuit, for VTC we have two methods to represent the voltage either by converting the voltage to time (VTC) or frequency (VFC). The main contribution of this work is to provide a comparative study between the two methods (i.e., the VTC circuit and the VFC circuit).

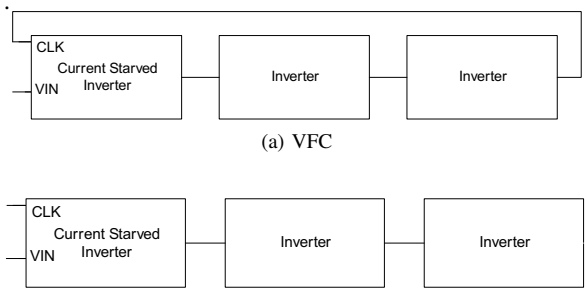
The comparison aspects between the two circuits are dynamic range, sensitivity, linearity error, signal to noise and distortion ratio (SNDR), effective number of bits (ENOB), maximum input frequency, and power consumption.

The rest of the paper is arranged as follows. Section II introduces the circuit descriptions of the VTC and the VFC implementations. Section III includes the simulation results and the comparative study. Finally, conclusion results are presented in Section IV..

II. Circuit description

Several Voltage-to-Time Converters (VTC) circuits and Voltage-to-Frequency Converters (VFC) circuits have been introduced. Most of these circuits depend on the simple current starved inverter shown in Figure 2. In our circuit we use the simple current starved inverter with inherited sample-and-hold. VFC is an inverter based ring oscillator, where the CLK of the circuit is the feedback of the output as shown in Figure 1.a. VTC uses the current starved inverter followed by two stage inverters to assure almost the same load of the circuit output similar to the VFC circuit for fair comparison as shown in Figure 1.b.

978-1-4673-8937-2/16/$31.00



(a) VFC

(b) VTC

Fig. 1. VFC and VTC circuits block diagram

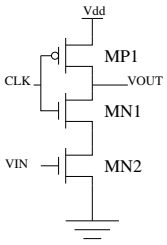


Fig. 2. Current starved inverter

Simulation is performed using Cadence based on TSMC 65nm CMOS technology and by applying the same design parameters for both circuits.

The input supply voltage is 1.2 V. The CLK used with the VTC circuit is 51 ns as the maximum pulse width that can be achieved is 50 ns within the dynamic range we are working on (0.12 V). At the rising edge of the CLK, the output of the current starved inverter (VOUT) starts to decrease gradually depending on the value of the input voltage (VIN), then as VOUT crosses Vthreshold of the inverter which is almost $Vdd/2$ the inverter output will be Vdd and will not be affected by any change of the value of VIN till the next rising edge of the CLK. This shows how the sample-and-hold is operated inherently, where the sampling begins at the rising edge of the CLK and ends when VOUT crosses Vthreshold of the inverter, by crossing Vthreshold of the inverter the hold state begins and lasts till the next rising edge of the CLK.

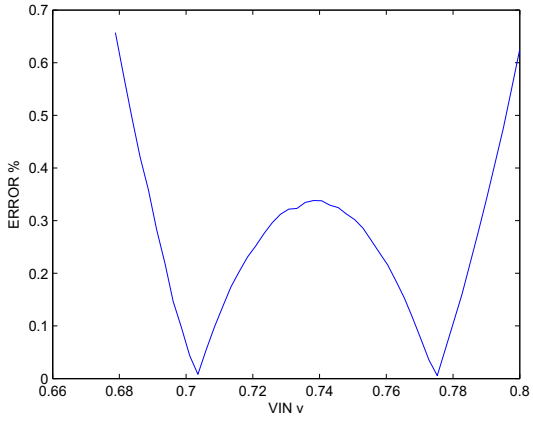
III. Simulation Results and Comparative Study

A. Dynamic Range

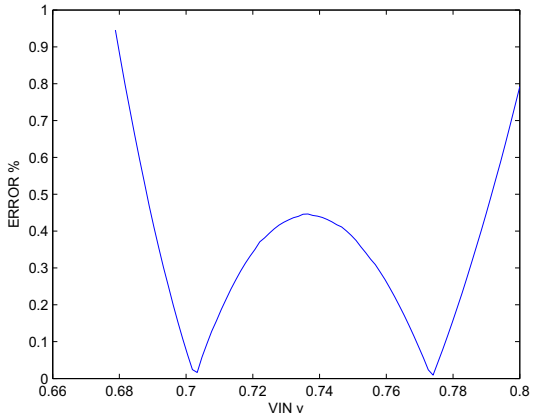
Dynamic range is chosen to specify a linearity error of about 0.9% for the two circuits as shown in Figure 3. The Dynamic range for both circuits equals to 0.12 V ranging from 0.68 V to 0.8 V.

B. Sensitivity

All the Analog to Digital converters suffer from non-linearity error, causing their output to depart from the linear functionality of their input. Sensitivity is calculated for both circuits by performing parametric sweep analysis for the input voltage within the calculated dynamic range 0.12 V, the sweep



(a)



(b)

Fig. 3. Error at dynamic range 120 mV, (a) VFC linearity error is 0.66% and (b) VTC linearity error is 0.95%

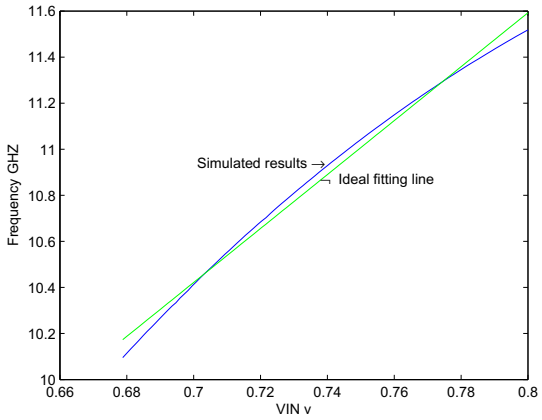
analysis is performed by varying the input voltage from 0.68 V to 0.8 V. As the CLk in VFC is the feedback from the output, resulting in a high sampling frequency resulting in capturing more samples so becomes more sensitive to the input supply variation. The CLK is a function of the input voltage which differs from VTC. It is shown that VFC is better than VTC as shown in Figure 4. Sensitivity is the slope of the linear range from the graph it is shown that the simulated results for VFC is much linear than that of VTC.

C. Power

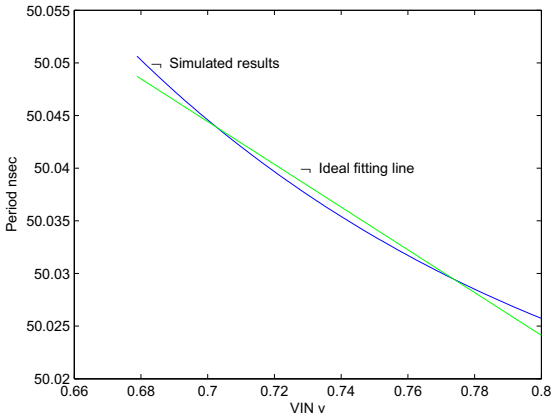
The power consumption is calculated at an input frequency (Fin) at 0.195 MHZ (the maximum input frequency for VTC at 5 bits resolution) for both circuits. As VFC uses its output as its CLK resulting in a higher sampling frequency, it consumes more power than VTC. It is found that the VTC circuit exhibits much lower power consumption than the VFC, (i.e., VTC exhibits 418.5 nW, while VFC exhibits 171 μW).

D. Signal to Noise and distortion Ratio (SNDR)

Signal to noise and distortion ratio (SNDR) is the measure used to compare the level of the wanted signal to the level



(a)



(b)

Fig. 4. Sensitivity, (a) VFC Linearity is 11.71 GHZ/V and (b) VTC Linearity is 0.2 ns/V

of the noise. It is also used to identify the ratio of the useful information to false data. It is calculated as the signal power to the noise power in dB, the SNDR can be expressed as

$$SNDR = 10\log_{10}\left(\frac{Spwr}{Npwr}\right) dB \quad (1)$$

Where $S_{pwr}$is the signal power and $N_{pwr}$is the noise power. It is found that VFC has better SNDR compared to VTC, i.e., VFC introduces less noise than VTC does, as shown in Figure 5. This is due to the CLk in VFC is the feedback from the output which leads to have a high sampling frequency, and as the current supplying the circuit increases the SNDR increases as explained in [4]. VFC consumes much current than what VTC consumes due to the feedback.

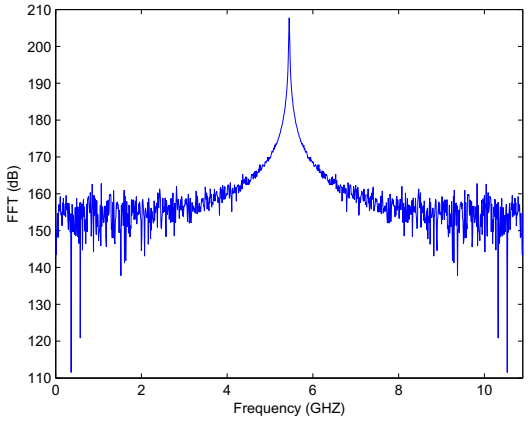
E. Effective number of bits (ENOB)

Resolution of Analog to Digital converters (ADC) is the number of discrete values that can be produced within the range of the analog values. The resolution of ADC is specified by the number of bits that can represent analog values; these bits represent the number of levels that can be used to represent the analog values. The number of levels is a power of two; i.e., for N bits resolution we have 2^N levels to represent the analog values. However ADC circuits introduce noise and distortion.

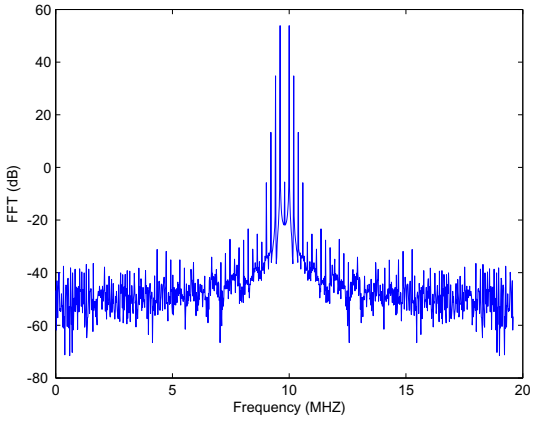
Effective number of bits (ENOB) is the resolution of an ideal ADC circuit that would have the same resolution as the circuit under consideration. The Effective number of Bits can be expressed as function of SNDR as

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad (2)$$

As the CLk in VFC is the feedback from the output which leads to a higher sampling frequency. It is found that the ENOB for VFC is better than VTC, (i.e., VFC ENOB is 3.8 bits, while VTC ENOB is 2.7 bit).



(a)



(b)

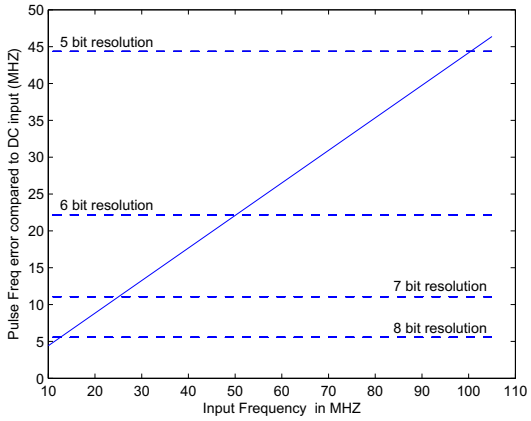
Fig. 5. Signal to noise ratio and effective number of bits at input frequency 0.195 MHZ, (a) VFC SNR is 22.9 dB and (b) VTC SNR is 16.1 dB

F. Maximum Input Frequency

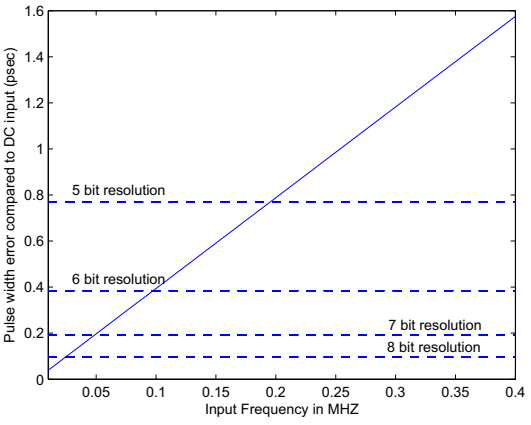
The maximum input frequency is the frequency that can be used in the circuit without having a significant error when the circuit is used without sample-and-hold. The maximum input frequency of VFC and VTC is determined by using sinusoidal input signals at multiples of the clock frequency

(i.e., (4/3)*f$_{CLK}$, 2*f$_{CLK}$, and 4*f$_{CLK}$) as performed in [1]. The simulated results are shown in Figure 6 where the delay and frequency error is plotted versus the input frequency.

The error for VTC is calculated as the deviation between the output pulse width compared to the output pulse width with DC input voltage equal to the sinusoidal input voltage at the sampling instant, while for VFC is calculated as the deviation between the output frequency compared to the output frequency with DC input voltage equal to the sinusoidal input voltage at the sampling instant. The maximum tolerable error due to an input signal changing rapidly during the time when that signal is effectively being sampled is equal to one Least Significant Bit (LSB) of the ADC resolution [1]. For example, for 5 bit ADC resolution with an input dynamic range of 120 mV and a sensitivity of 0.2 ns/V for VTC and 11.71 GHZ/V for VFC, one LSB corresponds to 3.75 mV (=120 mV / 2^5) or 0.75 ps (=3.75 mV * 0.2 ns/V) pulse width for VTC and 44.39 MHZ (3.75 mV*11.71 GHZ/V) for VFC. Several lines indicating the maximum delay and frequency error for 5 bits, 6 bits, 7 bits, and 8 bits ADC resolutions are shown in Figure 6.



(a)



(b)

Fig. 6. Maximum input frequency, (a) VFC and (b) VTC

It is shown at 5 bits resolution that the maximum input frequency (Fin) is 0.195 MHZ without the need of sample-and-hold for VTC while for VFC the maximum input frequency (Fin) is 100.4 MHZ without the need of sample-and-hold. This is due to the CLk in VFC is the feedback from the output which leads to a higher sampling frequency compared to VTC which is 51 ns.

G. Design recommendation

After comparing the two circuits using the same design parameters for fair comparison, Simulation results show that the VFC circuit is better than the VTC circuit, however it consumes much power. VTC is preferred for applications that require low power consumption such as medical applications. To use VTC in high input frequency applications S/H circuits should be used. While VFC is preferable for applications that require high input frequency as RF applications, however the drawback will be the large power consumption with respect to VTC.

IV. Conclusions

As shown in Table 1 Voltage-to-Frequency Converter (VFC) circuit is found to be better than Voltage-to-Time Converter (VTC) circuit in the maximum input frequency, signal to noise and distortion ratio (SNDR), effective number of bits (ENOB) at the same input frequency (Fin is 0.195 MHZ), and sensitivity. However Voltage-to-Time Converter (VTC) circuit is better in the power consumption, while VTC and VFC are almost similar in the linearity error.

TABLE I
Comparison between VFC and VTC

Comparison aspects	VFC	VTC
Dynamic Range	0.12 V	0.12 V
Power	171 μW	418.5 nW
Sensitivity (Linearity)	11.71 GHZ/V	0.2 ns/V
Error	0.66 %	0.95 %
Signal to Noise ratio (SNR)	22.9 dB	16.1 dB
Max input Freq. at 5 bits resolution	100.4 MHZ	0.195 MHZ
ENOB at Fin = 0.195 MHZ	3.8	2.7

Acknowlegment

This work was partially funded by Zewail City of Science and Technology, AUC, Cairo University, NTRA, ITIDA, SRC, ASRT, the STDF, Intel, Mentor Graphics, MCIT, NSERC.

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