Field Programmable Analog Array based on CMOS CFOA and its Application

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***Abstract*—A proposed configurable analog block (CAB) is presented, simulated and analyzed. The CAB consists of a CMOS current feedback operational amplifier (CFOA), presented by the authors, as the main active block, programmable resistor array, programmable capacitor array and MOSFET switches. Using the CABs, the universal field programmable analog array (FPAA) has been constructed, which can realize many signal-processing functions including variable gain amplifiers, filters. The core of the chip is occupied by an array of 16 (four by four) CAB cells. Each of these CABs' are identical and each may communicate with any other in the array via field programmable interconnect. The input and output pins are provided around the chip and each contains a single operational amplifier, which may drive onto or off the chip. To show the reliability of the proposed CAB, different filter structures responses have been realized using the proposed CAB.**

Index Terms— CMOS, current feedback operational amplifier, configurable analog blocks, Field programmable analog Arrays, filters

I. Introduction

The role of analog integrated circuits in modem electronic systems remains important, even though digital circuits dominate the market for VLSI solutions. Analog systems have always played an essential role in interfacing digital electronics to the real world in applications such as analog signal processing and conditioning, industrial process, motion control and biomedical measurements[1]-[23]. An important advantage of digital integrated circuits has been their relative ease of design over analog circuits. In particular, since digital circuit design is amenable to automation, several CAD- compatible digital integrated circuit design methodologies have been developed, including design-for-testability, design optimization, rapid prototyping in Field-Programmable Gate Arrays (FPGAs) and, more recently, hardware synthesis from behavioral descriptions.

The drive towards shorter design cycles for analog integrated circuits has demanded the development of high performance analog circuits that are reconfigurable and suitable for CAD methodologies [1].

There have been some programmable analog circuits in the literature [1]-[12] as well as commercial chips (MPAA020 from Motorola, AN10E40 from Anadigm). However, general-purpose FPAAs suitable for high-frequency signal processing applications were rare [10].

Analog circuits based on the continuous time current feedback operational amplifier (CFOA) technique are suitable for high frequency applications [13]. Having a CFOA with programmable capacitor and programmable resistor arrays, it is possible to build filters for wide frequency range.

The CFOA a versatile building block for continuous time analog signal processing. The CFOA closed-loop bandwidth is independent of its close-loop gain (provided that the feedback resistance is kept constant and much higher than the CFOA inverting input resistance) [14] unlike VOA-based circuits, which are limited by a constant gain-bandwidth product. The current feedback operational amplifier (CFOA), is a four-port network with a describing matrix of the form,

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_O \end{bmatrix} \quad (1)$$

Several CMOS realizations for the CFOA have been reported in the literature [13]-[22].

In this paper, a new CMOS configurable analog block (CAB) based on CFOA suitable for filtering applications has been presented. Using the proposed CAB, a universal field programmable analog array is constructed, which is suitable for realizing different signal-processing blocks. The structure of the FPAA is composed of universal configurable analog block (CABs). The proposed FPAA has been configured to realize different filter structures responses.

This paper is organized as follows; in section II the proposed CAB architecture has been presented. In section III, a global view of the proposed FPAA architecture and its routing matrix have been illustrated. In section IV, to show the reliability of the proposed CAB, a second order low-pass, high-pass, band-pass and all-pass filters have been realized using the proposed CAB. Finally, the conclusion is drawn in section V.

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II. PROPOSED CONFIGURABLE ANALOG BLOCK (CAB)

The Configurable analog blocks (CABs) are tiled across the chip in regular mesh-type architecture with busses and local interconnects in-between as shown in Fig. 3. The configurable blocks were designed to provide a sufficiently flexible, generic architecture while optimizing certain frequently used signal processing blocks.

Fig. 1 shows the proposed analog CAB, Each CAB could be viewed as a functional block consists of one CFOA as an active block, three programmable resistor arrays, two programmable capacitor arrays, a programmable shift register and a set of MOSFET switches. This CAB could be used to realize different filters responses and also some analog functions like subtraction, addition, integration …etc.

The CAB interconnection matrix has been designed to give internal interconnections flexibility and guaranteed high frequency performance for the CAB. Each input for the CFOA block could be connected to the input directly or to another port from the CAB through internal switching matrix. Also, the output terminal could be connected as feedback to any input terminals in the CAB or outside the CAB. All the inputs could be connected to internal ground line through the switching matrix. All the connections could be configured using the configuration shift register.

Fig. 2 gives the CAB configuration shift register consisting of 22 controlling bits. The first four bits are used to configure the value of the array of resistors connected to the Y terminal; the next four bits configure the array of resistors connected to the X terminal, while the last array of resistors connected to the Z terminal is configured by the next four bits. The two capacitor arrays are configured using ten bits (5 bits for each array). The configuration shift register is connected serially to the pervious and next CABs shift register. The first CAB in the upper left of the chip is connected to a serial programmable pin to load a bit stream of binary data serially to program the FPAA chip. Depending on the application the configuration switches could be programmed to provide the required functional block.

A. CMOS Realization of the CFOA [13]

The CMOS realization of the CFOA used here has been presented by the authors in [13].

B. Programmable Capacitor Array

The programmable capacitor array is shown in Fig. 4. It consists of capacitors C_0 and switches S_n. The capacitor array built of an appropriate number of capacitors connected in parallel. Switches are realized using MOSFETs. When switch S_n, where n is the switch number $\in$ {1, 5} is closed the equivalent capacitance to the array could be expressed as

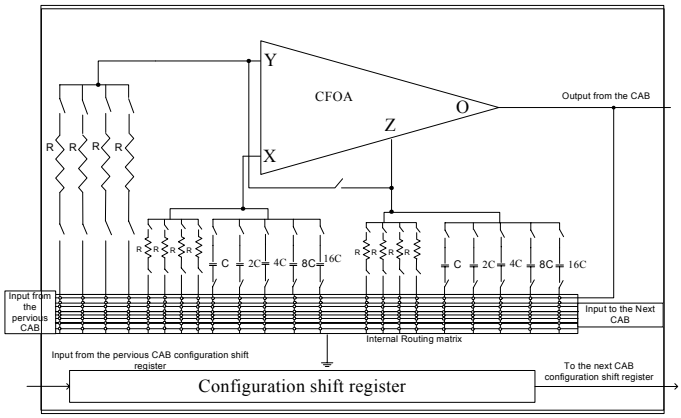

Fig.1 Proposed Configurable Analog Block (CAB)

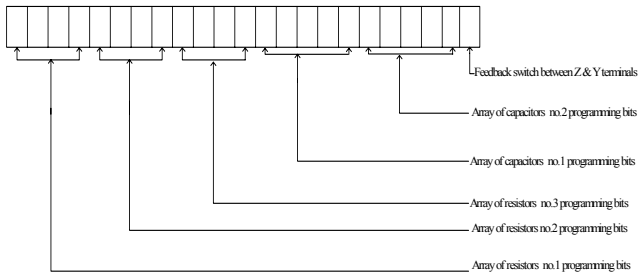

Fig. 2. The CAB Configuration Shift registers

$C_{eq} = C_{array} + C_{par}$ where C_{par} is the parasitic capacitance of connections when all switches open and C_{array} is the equivalent capacitance of the array can be expressed as follows:

$$C_{array} = \sum_{n=1}^{5} S_n C_n \qquad (4)$$

where S_n is equal to 1 when switches are closed and equal to 0 when switches are open. The minimum equivalent capacitance equal to 1pF and the maximum is equal to 7pF.

C. Programmable Resistor Array

The programmable resistor array is shown in Fig. 5. It consists of resistors R_0 and switches S_n. The Resistor array built of an appropriate number of resistors connected in parallel. Switches are realized using MOSFETs. When switch S_n, where n is the switch number $\in$ {1, 4} is closed the equivalent resistance to the array could be expressed as follows:

$$R_{eq} = \sum_{n=1}^{4} S_n \frac{R_0}{n} \qquad (5)$$

where R_{eq} is the equivalent resistance of the array and S_n is equal to 1 when switches are closed and equal to zero when switches are open. The minimum equivalent resistance equal to 10 Kohm and the maximum is equal to 40Kohm.

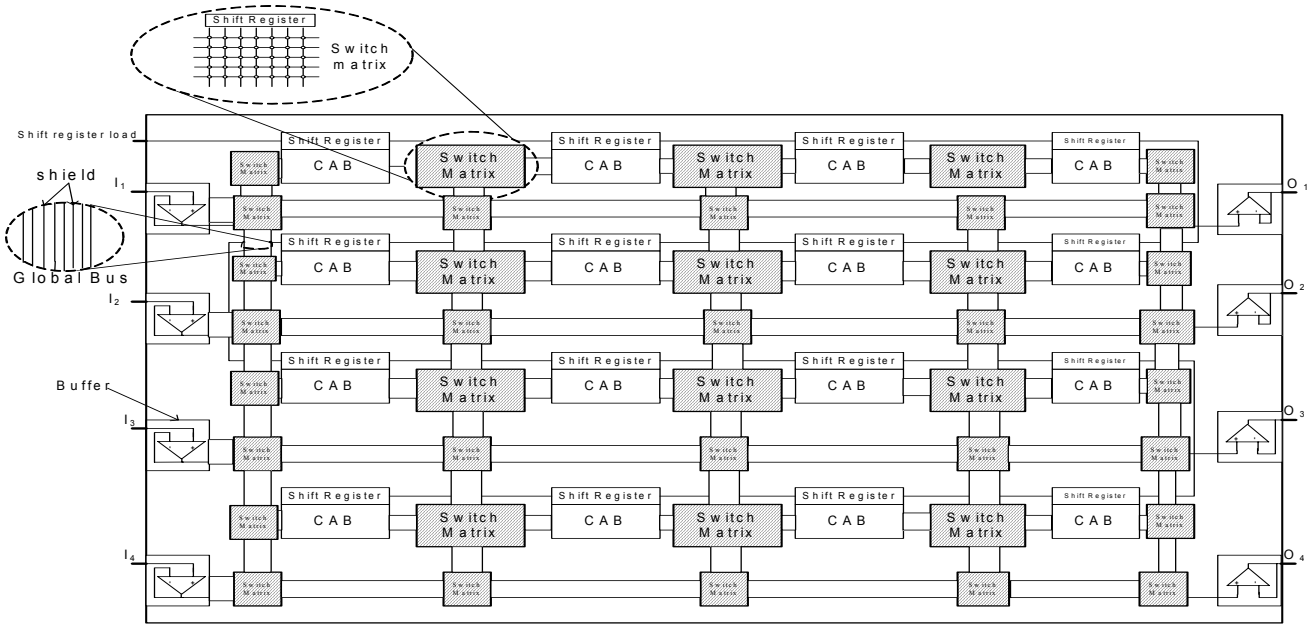

Fig.3 The proposed FPAA design approach with detailed switching matrix

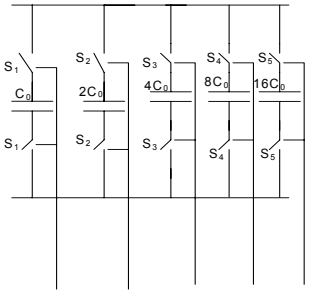

Fig. 4 Programmable Capacitor array

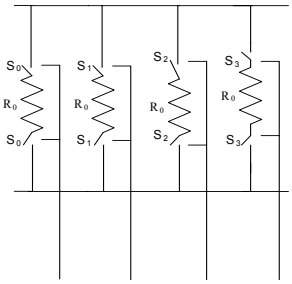

Fig. 5 Programmable Resistor array

III. FPAA Architecture and Interconnection

FPAA have achieved great benefits in analog circuits and system design. However, the most challenges for the FPAAs are high-frequency analog signal processing applications [1]-[13]. Having a current feedback operational amplifier and programmable capacitor array, it is possible to build applications for wide range of frequencies. A new approach used to develop FPAA based on a CFOA which allows easy adaptability to implement the most analog signal processing blocks. High frequency operation, simple programming methodology and use of standard CMOS fabrication process are the main features of the proposed FPAA.

A. FPAA Architecture

Fig. 3 shows a schematic view of the FPAA architecture at highest hierarchical level. The core of the chip is occupied by an array of 16 (four by four) core cells. Each of these cells are identical and each may communicate with any other in the array via field programmable interconnect. The input and output pins are provided around the chip and each contains a single operational amplifier, which may drive onto or off the chip. These cells may also be used as unity gain buffers. In the left upper side, a configuration pin connected to the first CABs' configuration shift register.

B. FPAA Interconnection

Connectivity between CAB blocks in the array plays a significant role on the performance of the circuit realized on the FPAA [4]. The FPAA is a regular square array of CABs interconnected, as shown in fig. 3, with a crossbar structure having horizontal and vertical interconnection lines. In this cross-bar structure, inputs and output of CAB's can be connected via switches placed in the intersection of the vertical and horizontal lines. With this crossbar structure each CAB could be connected to any neighboring CAB or to the input to the FPAA chip directly.

Configuration of this interconnection network could be done by loading design-specific programming stream of bits into FPAA to define their interconnections. Each configuration bit defines the state of an interconnect pass transistor. A global clock line has been added in the FPAA interconnection network for the shift register clock.

The characteristics of the configured function can be programmed through configurable word. The desired connectivity between CABs in an array is determined by the routing word. The digital control words are stored in a single shift register inside the CAB. Shift register inside the CAB could be used to program the resistor arrays, the capacitor arrays, and the interconnection of the input, output, and feedback switches. All shift registers in CABs are connected in series and collectively acts as a single shift register which can be loaded with the desired programming bit stream through one external pin Fig. 3.

IV. Applications: Reliability of the Proposed CAB to Realize Different Filter Structures Responses

To show the reliability of the proposed CAB, it is used to

realize a second-order low-pass, high-pass, band-pass, and all-pass filters structure as shown in Figs. 6 a, b, c, d respectively. The filter consists of three cascading blocks: the first block, is a weighted differential voltage integrator, the second block is a weighted differential voltage adder integrator, and the last block is a weighted differential voltage adder amplifier. By cascading an (n-1) times from the second block between the first and last block, an N–order low-pass, high-pass, band-pass, and all-pass filters can be realized. By direct analysis, the following transfer functions is obtained,

$$\frac{V_{outlow-pass}}{V_{in}}=\frac{R_3(R_2-R_1)}{R_1R_2}\frac{\left(\left(\frac{1}{C_1C_2}\right)\left(\frac{(R_2-R_1)}{R_1R_2}\right)^2\right)}{s^2+s\left(\frac{1}{C_2}\frac{(R_2-R_1)}{R_1R_2}\right)+\left(\left(\frac{1}{C_1C_2}\right)\left(\frac{(R_2-R_1)}{R_1R_2}\right)^2\right)} \quad (6)$$

$$\frac{V_{outhigh-pass}}{V_{in}}=\frac{R_3(R_2-R_1)}{R_1R_2}\frac{s^2}{s^2+s\left(\frac{1}{C_2}\frac{(R_2-R_1)}{R_1R_2}\right)+\left(\left(\frac{1}{C_1C_2}\right)\left(\frac{(R_2-R_1)}{R_1R_2}\right)^2\right)} \quad (7)$$

$$\frac{V_{outband-pass}}{V_{in}}=\frac{R_3(R_2-R_1)}{R_1R_2}\frac{-s\left(\frac{1}{C_2}\frac{(R_2-R_1)}{R_1R_2}\right)}{s^2+s\left(\frac{1}{C_2}\frac{(R_2-R_1)}{R_1R_2}\right)+\left(\left(\frac{1}{C_1C_2}\right)\left(\frac{(R_2-R_1)}{R_1R_2}\right)^2\right)} \quad (8)$$

$$\frac{V_{outall-pass}}{V_{in}}=\frac{R_3(R_2-R_1)}{R_1R_2}\frac{s^2-s\left(\frac{1}{C_2}\frac{(R_2-R_1)}{R_1R_2}\right)+\left(\left(\frac{1}{C_1C_2}\right)\left(\frac{(R_2-R_1)}{R_1R_2}\right)^2\right)}{s^2+s\left(\frac{1}{C_2}\frac{(R_2-R_1)}{R_1R_2}\right)+\left(\left(\frac{1}{C_1C_2}\right)\left(\frac{(R_2-R_1)}{R_1R_2}\right)^2\right)} \quad (9)$$

The ω_O, Q, and DC gain H of the filters are given by:

$$\omega_o=\frac{(R_2-R_1)}{R_1R_2\sqrt{C_1C_2}},\ Q=\sqrt{\frac{C_2}{C_1}},\ H=\frac{R_3(R_2-R_1)}{R_2R_1} \quad (10)$$

Fig. 7 a, b, c, d show the simulated magnitude responses of the second order low-pass, high-pass, band-pass, and all-pass filters, where R_2 =20KΩ, R_1=10KΩ, R_3=20KΩ, and C_1=C_2= 0.005nf. From the pervious filter realizations, the proposed CAB could be programmed to realize different filter structures using special configurations bits.

V. CONCLUSION

A new design for configurable analog block suitable for high frequency applications is introduced. The proposed CAB consists of a current feedback operational amplifier (CFOA) as a main active block, programmable resistor, programmable capacitor arrays and MOSFET switches. Using the CAB, a universal field programmable analog array is constructed, which is suitable for realizing different analog signal-processing blocks. As a design example to show the reliability of the proposed CAB, a realization of low-pass, high-pass, band-pass, and all-pass filters has been designed and simulated.

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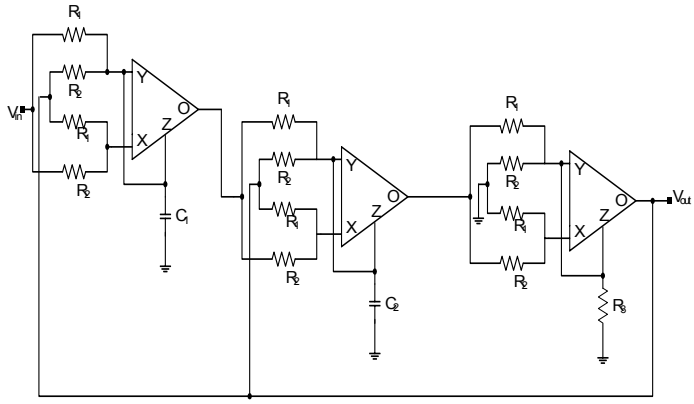

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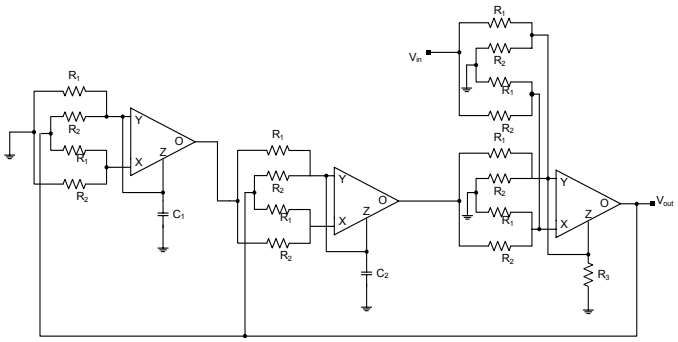

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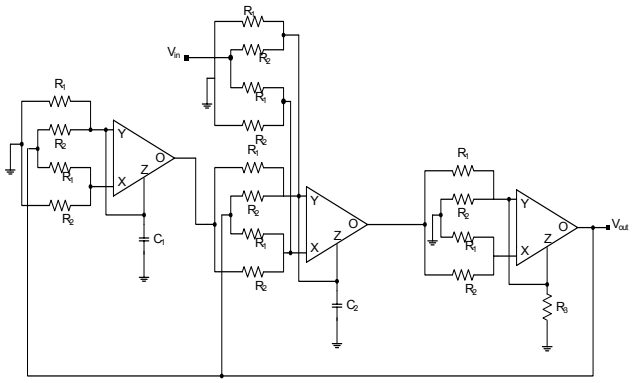

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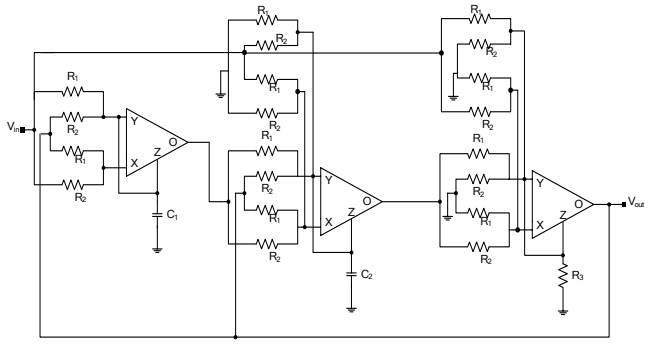
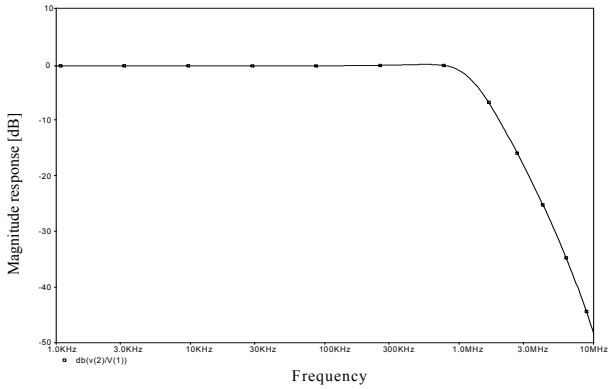


(d)

Fig. 6. The CAB-based grounded-C second-order filters (a) low-pass, (b) high-pass, (c) band-pass, and (d) all-pass.



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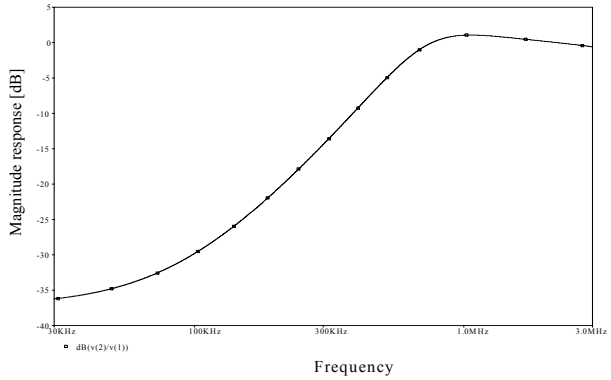

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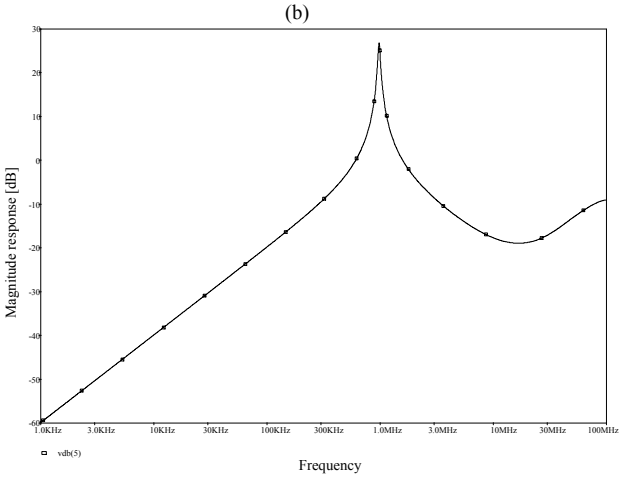

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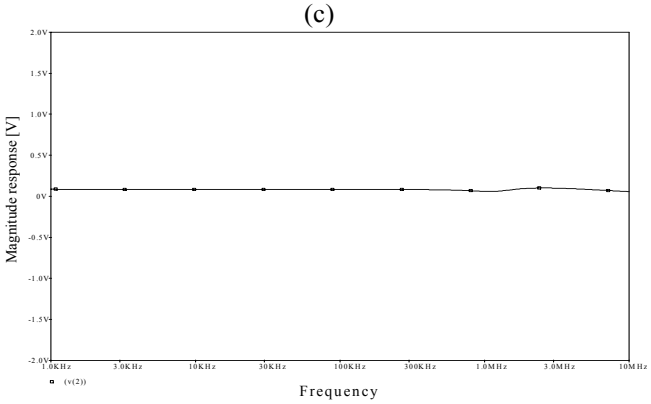

(d)

Fig. 7. Magnitude responses of the second-order filters (a) low-pass, (b) high-pass, (c) bandpass, and (d) all-pass based on the proposed-CAB.