New 1.5-V CMOS Current Feedback Operational Amplifier

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Abstract— a **novel CMOS low-voltage current feedback operational amplifier (CFOA) is presented. The proposed CFOA based on a new positive second-generation current conveyor (CCII+). The new circuit allows almost a rail-to-rail input and output operation; also, it reduces the offset voltage and provides high driving current capabilities. The CFOA is operating at supply voltages of ±0.75 V with a total standby current of 338 µA. The circuit exhibits better than 10 MHz bandwidth and ±1mA current drive capability. PSpice simulation results are given using 0.35µm technology for the proposed CFOA.**

***Index Terms*— CMOS, current feedback op-amp, low-voltage, rail-to-rail.**

I. INTRODUCTION

In recent years, great interest has been devoted to the analysis and design of current feedback op-amp and current-conveyor integrated circuits [1]-[13], mainly because these circuits exhibits better performance, particularly higher speed and better bandwidth, than classic voltage-mode operational amplifiers (VOA). The CFOA close-loop bandwidth is independent of its close-loop gain (provided that the feedback resistance is kept constant and much higher than the CFOA inverting input resistance) [6] unlike VOA-based circuits, which are limited by a constant gain-bandwidth product. The current feedback operational amplifier (CFOA), whose symbol shown in Fig. 1(a), is a four-port network which has a describing matrix of the following form,

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_O \end{bmatrix} \quad (1)$$

Originally, CFOAs were implemented using only bipolar processes technology. This technology is intrinsically well suited to processing signals in the form of currents given the high bipolar junction transistor (BJT) transconductance. More recently, Several CMOS realizations for the CFOA have been reported in the literature [4]-[6], [9]-[12]. The CFOA has been always seen as an extension of the CCII, therefore, the design approach was to cascade a CCII+ with a voltage follower to realize the complete circuit [2]. The obtained bandwidth was always a degraded version of the CCII+ bandwidth. Several CMOS CFOA implementations have been presented to provide offset compensation [4], high current drive capability [6], and large bandwidth [5]. The low-power/low-voltage issue, increasingly important in very large scale integrated (VLSI) circuits, was partially addressed in [9].

In this paper, a novel CMOS current-feedback operational amplifier is presented. The CFOA is capable of operating under a minimum supply voltage of $(|V_{Tp}|+V_{Tn}+V_{DS,sat})$ and with reduced power dissipation. The new circuit includes a class AB output stage exhibiting high current drive capability and good power conversion efficiency. Almost a rail to rail input and output voltage operation is also achieved.

This paper is organized as follows; In Section II, the circuit description and CMOS realization of the proposed CFOA is illustrated, In Section III, PSpice simulations of the proposed CFOA are given using CMOS 0.35 µm technology. In Section IV, conclusion has been drawn.

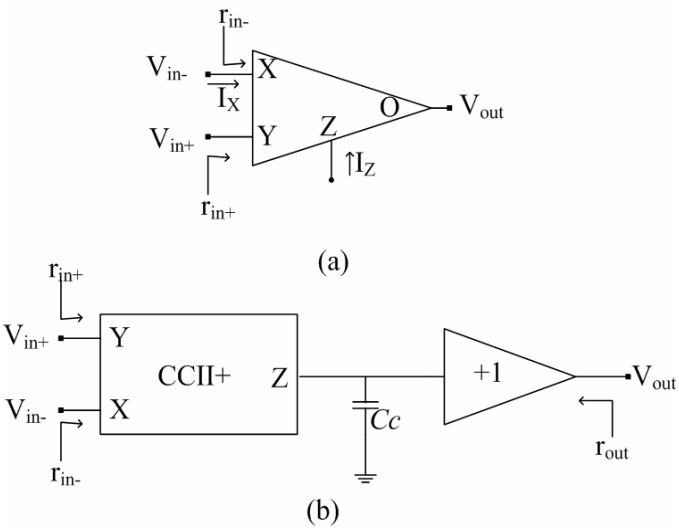

Figure 1. (a) Current feedback op-amp symbol, (b) CFOA block diagram [2]

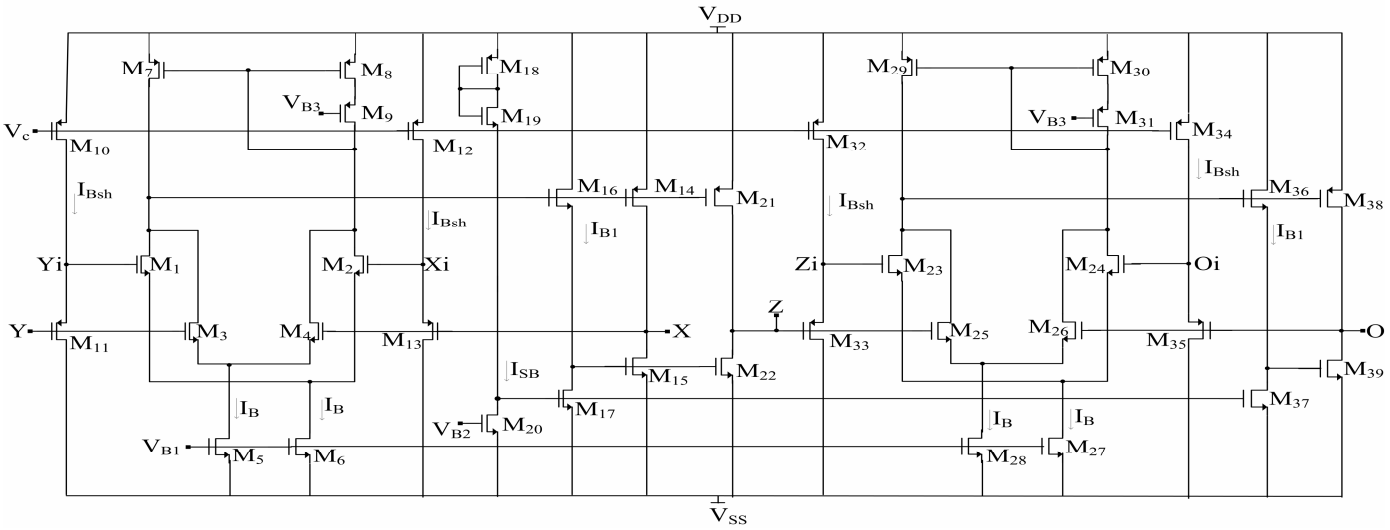

Figure 2. CMOS realization of the proposed CFOA.

II. Proposed CMOS Current Feedback Op-Amp

As stated in the introduction the CFOA could be realized by using the second generation current conveyor cascaded with a voltage follower [2], as shown in Fig. 1(b). The CMOS realization of the proposed CFOA offers both low-voltage and high drive capability will be described.

The CMOS realization of the proposed CFOA, shown in Fig. 2, consists of two matched parallel connected n-differential pairs (M_1, M_2) and (M_3, M_4), two matched biasing current source transistors (M_5, M_6), cascoded current mirror formed of two matched transistors (M_7, M_8), transistor (M_9), and two pairs of matched source followers transistors (M_{10}, M_{11}) and (M_{12}, M_{13}). Transistors M_5 and M_6 carry equal biasing currents (I_B), while transistors (M_{10}, M_{11}) and (M_{12}, M_{13}) produce a positive voltage shift for the input voltage applied on transistor M_{11} and M_{13}, respectively. All transistors are operating in the saturation region; the control voltage V_C applied to transistors M_{10} and M_{12} gates controls the shifting value as follows,

$$V_{Yi} = V_Y + (V_{DD} - V_C) \tag{2}$$

$$V_{Xi} = V_X + (V_{DD} - V_C) \tag{3}$$

where V_{Yi} and V_{Xi} are the output voltages from the source followers, V_Y is the high input impedance voltage, and V_X is the low input impedance terminal.

The circuit regions of operation could be explained as follows, for V_Y and V_X voltages are close to the negative supply voltage V_{SS} ($V_{SS} \le V_Y, V_X < 2V_{Tn} + V_{SS}$), the current source transistor M_5 and, hence, the differential pair M_3 and M_4 are cut-off. Then, the small and large signal behaviour of the whole circuit result only from the contribution of the differential pair M_1 and M_2, biased with current source transistor M_6. In the middle range ($2V_{Tn} + V_{SS} \le V_Y, V_X < V_C + 2V_{Tn} - 2V_{DD}$), both input pairs ($M_1$-$M_2$) and ($M_3$-$M_4$) are active and the small and large signal behaviour of the whole circuit result from the contribution of both differential pairs. Finally, when V_Y and V_X are very close to V_{DD} the positive supply voltage ($V_C + 2V_{Tn} - 2V_{DD} \le V_Y, V_X \le V_{DD}$), the current sources of the shifters M_{10} and M_{12} are cut-off. Therefore, the small- and large signal behaviour of the whole circuit contribution result only from the differential pair M_3 and M_4 biased with current source transistor M_5. This ensures a rail-to rail operation.

It is apparent, that this structure does not provide constant transconductance over the variations of the input voltages V_Y and V_X. A feed forward section could be added to guarantee a constant transconductance over the variations of the input voltages V_Y and V_X. However this is not a real drawback so long as the loop gain is sufficiently high. Indeed, variations of the open loop parameter were greatly reduced by feedback action.

The structure of the CFOA input stage (voltage follower) requires that the X terminal must have low input impedance. So, a suitable buffer circuit should be used to fulfill this condition and to provide a rail-to-rail swing capability. Transistors (M_{14}-M_{20}) fulfill the required buffering action with a rail-to-rail swing capability, as shown in Figure 2. Transistors M_{14} and M_{15} form the push pull output stage at the X terminal, transistors M_{16} and M_{17} are level shifting transistors providing proper biasing for transistor M_{15}. This push-pull action of M_{14} and M_{15} reduce the power dissipation. To prevent the cross over distortion, both transistors M_{14} and M_{15} must be ON when no current is withdrawn from the X terminal (standby mode), this current should be small and controllable. This is achieved by using a suitable gate voltage of M_{20}, which sets the voltage level shift between the gates of M_{14} and M_{15}. The standby power consumption of the overall circuit for dual power supply is given by:

$$P_{SB} = 2V_{DD}(4I_{SB} + 4I_B + 4I_{Bsh} + 2I_{B1}) \tag{4}$$

The last term in the above equation is the current passing through the level shifting transistors (M_{16} and M_{17}). This

current can be kept small by choosing small aspect ratio for transistors (M_{16} and M_{17}). The class AB output stage enables the circuit to drive the heavy resistive and capacitive load with low standby power dissipation and no slewing. It is worth mentioning that smaller miller compensation capacitors can be connected between the gate and drain of transistors M_{14} and M_{21} to ensure good transient response under all loads.

Transistors M_7 and M_8 force the currents in transistors M_1 and M_3 to be equal to the currents in transistors M_2 and M_4. Therefore,

$$I_{M_1} + I_{M_3} = I_{M_2} + I_{M_4} \tag{5}$$

From (5), the matched differential pair transistors are carrying equal currents. Therefore,

$$V_X = V_Y \tag{6}$$

The current follower stage, as shown in Fig. 2, is made up of transistors (M_{21}, M_{22}). They are conveyed the X terminal current into the Z terminal current. Therefore,

$$I_Z = I_X \tag{7}$$

Finally, a suitable buffer must be available between the Z and O terminals. It is similar to the buffer between the Y and X terminals and consisting from transistors M_{23} to M_{39}. This yield,

$$V_O = V_Z \tag{8}$$

It is worth to mention that, the proposed CFOA input stage is a dual circuit. This means that when the input stage formed from transistors M_1 to M_6 changed to PMOS, the current source formed from transistors M_7 to M_9 and the biasing circuits M_{10} to M_{12} will be NMOS and vice versa.

III. SIMULATION RESULTS

The performance of the proposed CFOA circuit was simulated using PSpice, supply voltages ±0.75V, 0.35µm CMOS technology parameters and transistor aspect ratios given in table 1.

Fig. 3 shows the output voltage swing of the proposed CFOA, a ±0.75V input sweep voltage was applied at the non-inverting input terminal voltage, the output voltage obtained at the O terminal; the inverting input and the Z terminals are terminated with 2kΩ for each. Fig. 4 shows the output voltage V_O when CFOA used to realize amplifier with gain equals two. The input terminal voltage is scanned from -0.75V to 0.75V while the X and Z terminals are terminated with 2kΩ and 4kΩ respectively. The total standby power dissipation is 0.507 mW. Fig. 5 shows the variations of the offset voltage across the X terminal versus the variation in the input current applied across X terminal (I_X) when V_Y is equal to zero. The X terminal input resistance R_X is less than 120Ω and the offset voltage is less than 40 mV. Fig. 6 shows the magnitude response of the CFOA when it is used to realize a variable gain amplifier, where, V_{in+} is the AC-Varying signal with 1V magnitude, the inverting terminal is terminated with a 0.75 kΩ and the Z terminal is terminated with a variable resistance taking the following values: 0.75kΩ, 1.5kΩ, 3kΩ, 6kΩ. The CFOA shows a constant bandwidth for different gains. The CFOA has a 3-dB bandwidth around 11MHz and the phase margin of 100^o. The input and output referred noise spectral densities, shown in Fig. 7, are less than 320nV/$\sqrt{Hz}$. Table 2 gives summary of the simulated results of the proposed CFOA.

TABLE I. TRANSISTOR ASPECT RATIOS OF THE CFOA

Transistor	W [µm]	L [µm]
$M_1 – M_4$, M_{23} - M_{26}	14	0.7
M_5, M_6, M_{27}, M_{28}	1.4	1.4
M_7, M_8, M_{29}, M_{30}	140	1.4
M_9, M_{31}	210	1.4
$M_{10} – M_{13}$, M_{32}-M_{35}	140	1.4
M_{14}, M_{18}, M_{21}, M_{38}	350	1.4
M_{15}, M_{19}, M_{20}, M_{22}, M_{39}	140	1.4
M_{16}, M_{17}, M_{36}, M_{37}	1.4	1.4

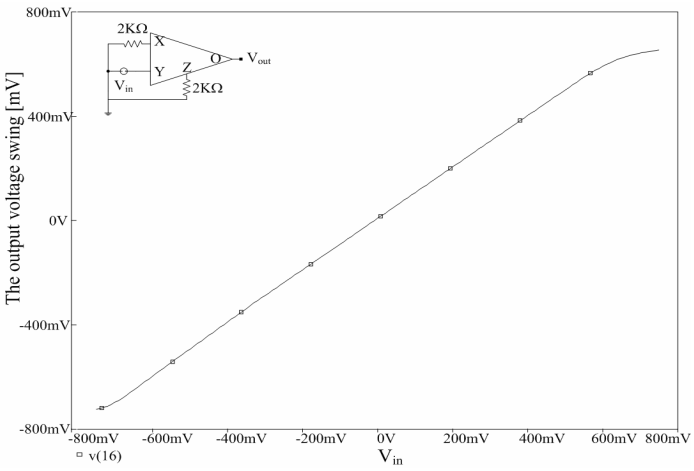

Figure 3. The output voltage swing.

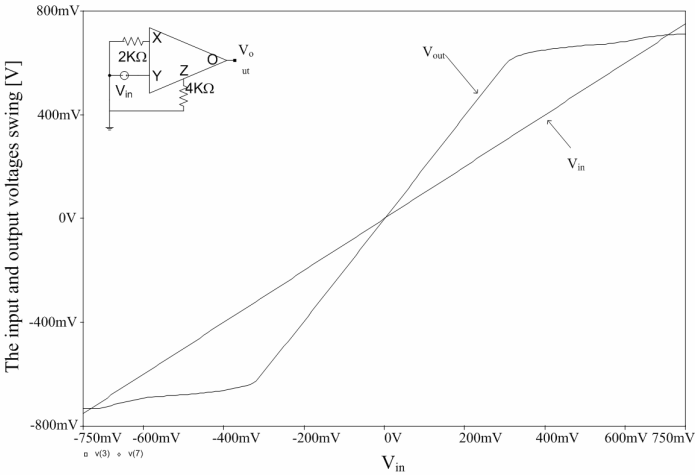

Figure 4. The input and output voltage swing for CFOA-based amplifier.

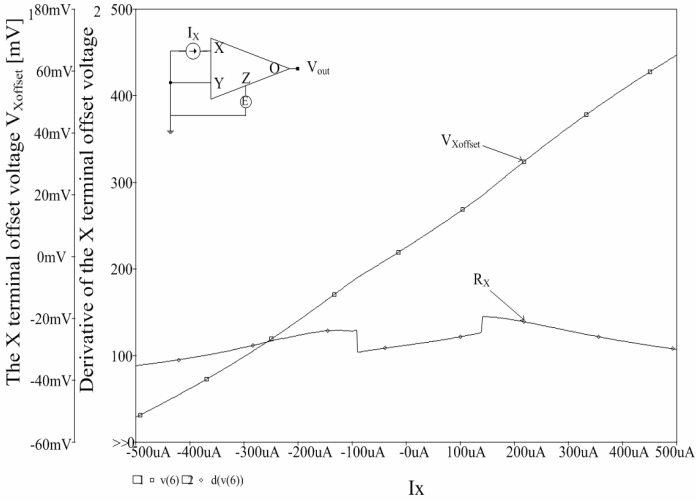

Figure 5. The X terminal offset voltage and its derivative versus input current I_X.

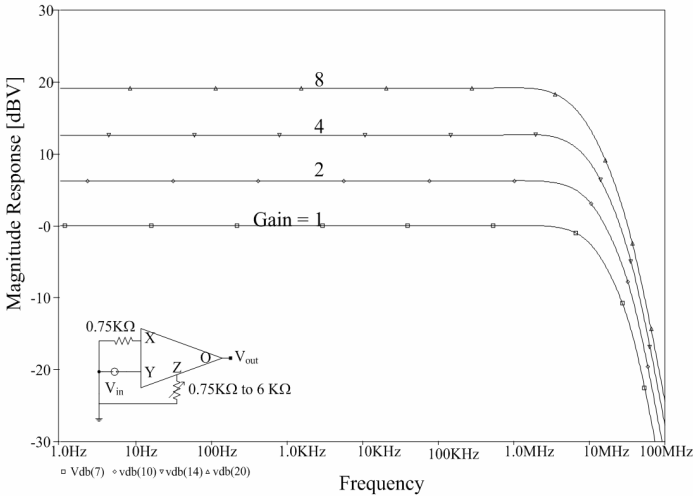

Figure 6. The magnitude response of the CFOA-based variable gain amplifier.

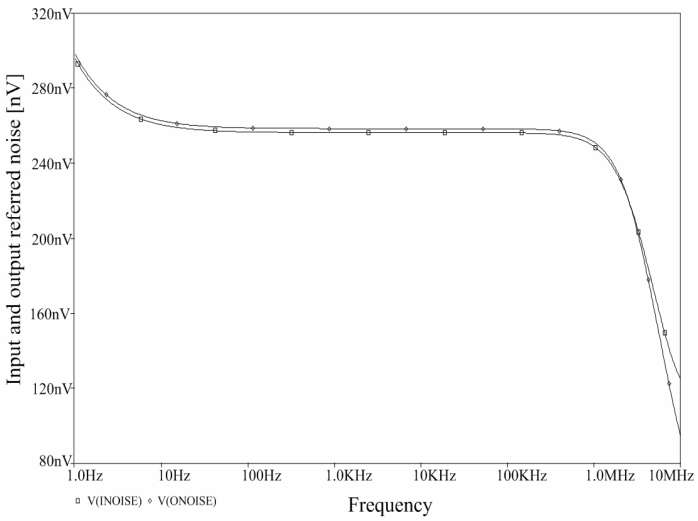

Figure 7. The input and output referred noise spectral densities.

IV. CONCLUSION

A new CMOS CFOA was presented, analyzed and simulated. The CFOA has improved the input stage open-loop bandwidth and reduced the voltage transfer error. The CFOA block is suitable for low-voltage, low-power applications and characterized by the ability to achieve small voltage, current transfer errors and high output driving current capability. Simulation results summary of the proposed CFOA were given in table 2.

TABLE II. SIMULATION RESULTS OF THE CFOA

Parameters	Proposed CFOA
CMOS Technology	0.35 μm
Power supply (V_{DD}, V_{SS})	(0.75 V, -0.75 V)
Total Power dissipation	0.507 mW
Input Voltage Dynamic range	-0.65 V to 0.65 V
The X terminal offset voltage while Y terminal is grounded	< 40 mV
Current driving capability	-1.mA, +1mA
Voltage transfer error	-0.012 dB
R_X	< 120 Ω
The CFOA Bandwidth	11.3 MHz

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