NOVEL COMPENSATED CMOS BUFFER

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ABSTRACT

A new CMOS buffer is introduced. A compensation circuit is used to cancel the output voltage offset resulting from the body effect. The voltage offset cancellation is achieved over all the input range hence resulting in a highly linear voltage transfer gain, which is independent of process variation. Class AB output stage is used in order to minimize the power consumption and increase the driving capability of the buffer. PSpice simulations for the proposed buffer are given to confirm the theoretical analysis.

1. INTRODUCTION

The voltage buffer is a versatile analog building block that is used in many applications [1]. Buffer circuits are also important in realizing many current-mode building blocks such as the current conveyor [2] and the current feedback op-amp [3]. Recently, high-performance buffer circuits have been designed in CMOS process [4-5]. The main requirements of a high performance voltage buffer are accurate voltage transfer, wide dynamic range, wide bandwidth as well as low output impedance. Voltage buffers based on source followers stages feature high performance voltage tracking gain that is independent on transistors mismatches [6]. However, the body effect can cause a voltage offset that is dependent on the input voltage, hence, resulting in a distortion in the voltage transfer gain. In this paper, a novel CMOS voltage buffer is presented. The proposed architecture is based on using source follower stages resulting in a voltage transfer gain that is independent of transistors mismatches. Moreover, a compensation circuit is used to cancel the voltage offset at different input values, hence resulting in accurate voltage tracking property that is independent of the body effect and the process variations. Low output impedance is achieved by applying negative feedback to a high gain loop. Class AB output stage is used in order to provide low power consumption and increase the capability of the buffer to drive high capacitive loads. PSpice simulations are included in order to verify the theoretical analysis.

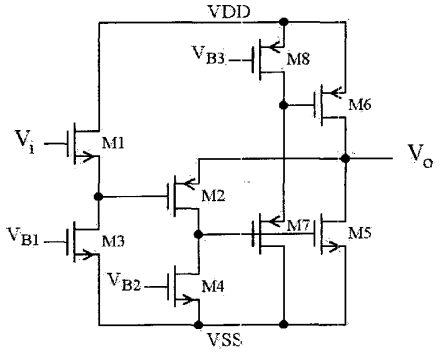

Figure 1. The uncompensated voltage buffer.

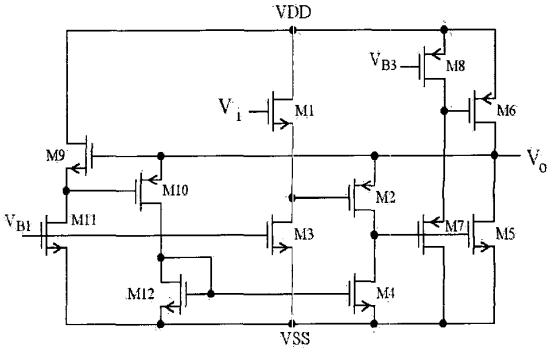

Figure 2. The compensated buffer circuit.

2. THE PROPOSED BUFFER CIRCUIT

Fig. 1 shows the uncompensated version of the proposed buffer. Transistors M1 through M4 are responsible for transferring the voltage from the input terminal to the output terminal. Transistor M5 is connected in negative feedback topology in order to achieve low output impedance. The level shift circuit formed by M7 and M8 is added to make the output transistors M5 and M6 operate in Class AB mode of operation. V_{B3} is used to control the standby currents following through M5 and M6.

Referring to Fig. 1, and assuming all transistors are operating in the saturation region, the voltage offset is

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obtained by writing the currents flowing through M1 and M2 as:

$$I_1 = I_3 = \frac{K_1}{2}(V_i - V_{S1} - V_{Tn1}(V_{S1}))^2 \quad (1)$$

$$I_2 = I_4 = \frac{K_2}{2}(V_o - V_{S1} - |V_{Tp2}(V_o)|)^2 \quad (2)$$

Where K is the transistor transconductance, V_S is the transistor source voltage, $V_{Tni}(V_{Si})$ and $V_{Tpi}(V_{Si})$ are the threshold voltages of the i^{th} NMOS and PMOS transistor respectively. The body effect is taken into consideration; hence, the threshold voltage is written as function of the transistor source voltage V_{Si}.

The voltage offset is defined as the difference between V_o and V_i and it is obtained from (1) and (2) as:

$$V_{off} = [|V_{Tp2}(V_o)| - V_{Tn1}(V_{S1})] + [\sqrt{\frac{2I_4}{K_2}} - \sqrt{\frac{2I_3}{K_1}}] \quad (3)$$

As given by (3), and considering the case where I_3 and I_4 are constant current sources as shown in Fig. 1, the mismatch between M1 and M2 due to process variations and the body effect will result in an uncontrolled voltage offset which is dependent on the input and output voltage values, hence, resulting in a distortion in the voltage transfer gain.

A solution for design is to choose I_3 and I_4 such that I_3/K_1 is equal to I_4/K_2 in order to minimize the voltage offset. However, the buffer will suffer from an offset voltage due to the threshold voltage mismatch. A better design can be achieved by keeping I_3 constant while generating I_4 in such a way to cancel the voltage offset.

Fig. 2 shows a modified version of the basic buffer circuit of Fig. 1, the circuit formed from M9 through M12 is used to generate the current I_4. Assuming M9 through M12 are matched to M1 to M4 respectively, the voltage offset of the compensated buffer can be obtained as follows:

$$I_9 = I_3 = \frac{K_9}{2}(V_o - V_{S9} - V_{Tn9}(V_{S9}))^2 \quad (4)$$

$$I_{10} = I_4 = \frac{K_{10}}{2}(V_o - V_{S9} - |V_{Tp10}(V_o)|)^2 \quad (5)$$

Since K_9 and K_{10} are equal to K_1 and K_2 respectively and from (4) and (5), the current I_4 is given according to the following relation:

$$|V_{Tp10}(V_o)| - V_{Tn9}(V_{S9}) + \sqrt{\frac{2I_4}{K_2}} - \sqrt{\frac{2I_3}{K_1}} = 0 \quad (6)$$

Since M2 and M10 have a common source, $V_{Tp2}(V_o)$ is equal to $V_{Tp10}(V_o)$, hence, the voltage offset can be rewritten from (3) and (6) as:

$$\begin{aligned} V_{off} &= |V_{Tp2}(V_o)| - |V_{Tp10}(V_o)| + V_{Tn9}(V_{S9}) - V_{Tn1}(V_{S1}) \\ &= V_{Tn9}(V_{S9}) - V_{Tn1}(V_{S1}) \end{aligned} \quad (7)$$

As given by (7), the voltage offset of the compensated buffer is equal to the voltage difference between the threshold voltages of M1 and M9. This voltage difference is caused by the body effect and depends on the difference between the sources of M1 and M9. From (1) and (4), the voltage V_{S9} is related to the voltage V_{S1} and the voltage offset V_{off} according to the following nonlinear relation:

$$V_{S9} - V_{S1} = V_{off} - [V_{Tn9}(V_{S9}) - V_{Tn1}(V_{S1})] \quad (8)$$

Substituting (7) into (8) results in V_{S9} equal to V_{S1} and consequently $V_{Tn1}(V_{S1})$ equal to $V_{Tn9}(V_{S9})$. Hence, the voltage offset described by (7) is equal to zero.

It is seen that complete voltage offset cancellation is achieved even in the presence of the body effect and independent of the value of the input or output voltage, hence, increasing the linearity of the voltage transfer gain.

Assuming that the transistors M9 through M12 are matched to transistors M1 through M4, the small signal voltage gain of the compensated buffer of Fig. 2 is approximately given by:

$$A_v \approx \frac{1}{1 + \alpha_1 + \alpha_2 + \alpha_3} \quad (9)$$

Where

$$\alpha_1 = (\frac{g_{d1} + g_{d3}}{g_{m1}} + \frac{g_{d2}}{g_{m2}})(\frac{g_{d10} + g_{d12}}{g_{m12}}),$$

$$\alpha_2 = -(\frac{g_{d1} + g_{d3}}{g_{m1}})^2 \text{ and}$$

$$\alpha_3 = (\frac{g_{d2} + g_{d4}}{g_{m5} + g_{m6}})(\frac{g_{d5} + g_{d6} + g_{d10}}{g_{m2}} + \frac{g_{d9} + g_{d11}}{g_{m1}})$$

As given by (9), the voltage gain is very close to unity and the gain error is of order of $(g_d/g_m)^2$. Also, it is seen that the voltage gain is independent of the transistors mismatches. As shown in Fig. 2, a negative feedback loop is used and results in a small output resistance which is approximately given by:

$$r_{out} \approx \frac{g_{d2} + g_{d4}}{(g_{m5} + g_{m6})\, g_{m2}} \quad (10)$$

Table 1. Transistor aspect ratios of the two buffer realizations of Figs. 1 and 2.

Transistor	W(μm)/L(μm)
M1, M9	200 / 1
M2, M10	10 / 1
M3, M11	10 / 4
M4, M12	30 / 4
M5, M6, M8	120 / 4
M7	40 / 4

Table 2. Simulation results of the two buffer circuits of Figs. 1 and 2.

Parameter	Fig. 1	Fig. 2	Unit
DC Gain error (at $V_i = 0$)	0.186	88 E-6	-
DC Gain (at $V_i = 0$)	0.814	1	-
Maximum deviation from DC gain	-0.22	-0.001	-
Input voltage linear range	-0.75 to 1.3	-0.75 to 1.3	V
V_{off} (at $V_i = 0$)	-23	45	μV
Maximum deviation from V_{off}	225	0.4	mV
Bandwidth	211	24	MHz
A_V	-1.78	0	dB
r_{out}	0.7	0.7	Ω

3. SIMULATION RESULTS

PSpice simulations are carried out with model parameters of 0.5 μm CMOS process. The supply voltages are equal to ± 1.5V. The dimensions of the two buffer realizations shown in Figs. 1 and 2 are given in Table 1. V_{B1} is set to 0.7 V resulting in $I_3 = 5$ μA while V_{B3} is equal to 0.3 V. Simulation results are given in Table 2.

Fig. 3 shows a comparison between the voltage gain and the voltage offset variations with respect to the input voltage for the uncompensated and compensated buffers of Figs. 1 and 2 respectively. As shown in Fig. 3, the uncompensated buffer suffers from a large gain error due to the body effect while the compensated buffer has a negligible gain error over the input range. Also, the compensated buffer features offset cancellation over a wide dynamic range, from 0.75V to 1.3V.

The two buffer circuits have small r_{out} which is equal to 0.7Ω. The magnitude and phase responses of the two buffer circuits are shown in Fig. 4. The compensation circuit resulted in a reduced bandwidth compared to the uncompensated buffer. Fig. 5 shows the output response when a 1p-p, 250kHz square wave is applied to the input of the compensated buffer of Fig. 2.

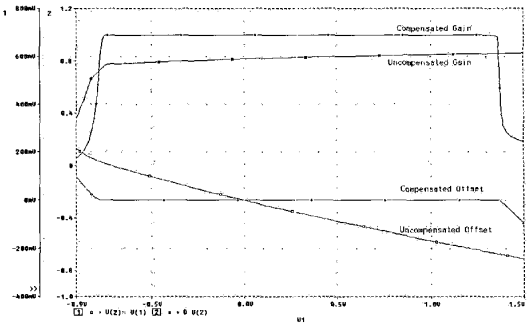

Figure 3. The voltage transfer gain and the voltage offset variations with respect to the input voltage for the buffer circuits of Figs. 1 and 2.

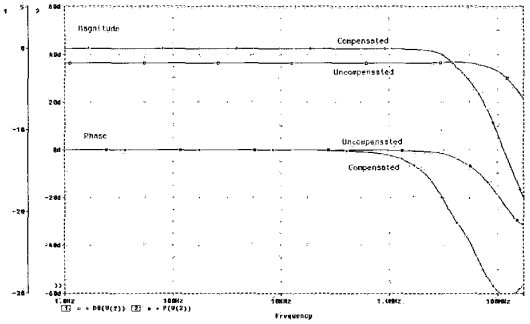

Figure 4. The magnitude and phase responses of the buffer circuits of Figs. 1 and 2.

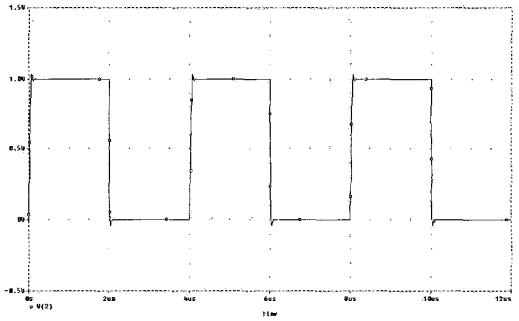

Figure 5. Transient response of the buffer circuit of Fig.2.

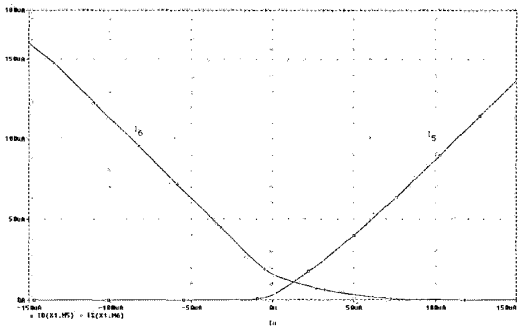

Figure 6. The push-pull action provided by the output stage of the buffer circuit of Fig.2.

Table 3 THD percentage values of the output voltage for the two buffer circuits.

Frequency (kHz)	THD (%)	
	Fig. 1	Fig. 2
62.5	0.5	0.017
125	0.5	0.033
250	0.5	0.07
500	0.51	0.13
1000	0.52	0.3

The standby current flowing through M6 when zero current is drawn from the output terminal is equal to 16 μA. The class AB mode-operation of operation provided by the buffer output stage is illustrated by drawing the current flowing through M5 and M6 with respect to the variations in the output current as shown in Fig. 6. It is worth noting that the currents flowing through M4 and M12 cause the standby current flowing through M5 to differ from that flowing through M6. However, the currents I_4 and I_{12} have no effect on the push-pull action provided by M5 and M6, since they only depend on the buffer input voltage.

Table 3 shows the THD percentage values obtained when a sinusoidal input signal of 1Vp-p is applied to the input of each the two buffer circuits of Figs. 1 and 2. The input frequency is varied over a range of 62.5kHz to 2MHz. It is clear that the realization of Fig. 2 features negligible THD values at low frequencies. The THD percentage is less than 0.3% at 1MHz.

4. SUMMARY

A novel buffer realization was presented. The proposed buffer features complete voltage offset cancellation over the input dynamic range independent of the body effect. The architecture used resulted in a high accuracy voltage tracking gain, which is independent of transistors mismatches. Class AB output stage was used in order to minimize the power consumption of the buffer. PSpice simulations were included and results showed good agreement with theoretical analysis.

5. REFERENCES

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