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Realizations of fully differential voltage second generation current conveyor with an application

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SUMMARY

Three novel CMOS realizations for the fully differential voltage second-generation inverting current conveyor (FDVCCII-) are proposed in this paper. The first realization has a limited input range, and the other two realizations have a rail to rail input range and show excellent features in linearity and bandwidth. As an application to the FDVCCII-, a floating gyrator is proposed. A floating inductor is realized using the floating gyrator and it is used in realizing a second-order low-pass filter, which is simulated and compared with the ideal result. All circuits are simulated with SPICE using CMOS 0.35 μm technology and supply voltages ±1.5 V to verify the theoretical results. Copyright © 2008 John Wiley & Sons, Ltd.

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KEY WORDS: current conveyor; floating current source; differential amplifier; gyrator

1. INTRODUCTION

Since the introduction of the second-generation current conveyor [1], it has shown high performance in terms of speed, bandwidth, linearity and power consumption. Recently differential circuit configurations based on current conveyors have been widely used to handle differential signals. As compared with single-ended devices, differential circuits have the advantages of higher rejection capabilities to noise, larger dynamic range and reduced harmonic distortion. Different CMOS realizations of the differential current conveyors and applications have been introduced in the literature [2–6], such as the differential voltage current conveyor [2] also known as the differential difference current conveyor [6].

In this paper, three new CMOS realizations for the fully differential voltage second-generation current conveyor with inverting current terminals (FDVCCII-) are introduced. It is a six terminal

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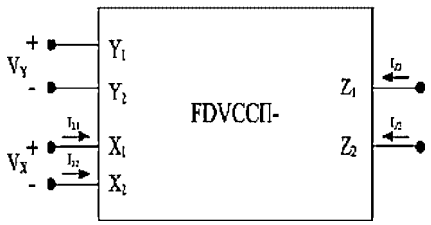

Figure 1. Block diagram of FDVCCII-.

device. Its symbol is shown in Figure 1. The relation between terminal voltages and currents is given by the following matrix equation:

$$\begin{pmatrix} V_{\mathrm{X}} \\ I_{\mathrm{Y}_i} \\ I_{\mathrm{Z}_i} \end{pmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & -1 & 0 \end{pmatrix} \begin{pmatrix} V_{\mathrm{Y}} \\ I_{\mathrm{X}_i} \\ V_{\mathrm{Z}_i} \end{pmatrix} \quad \text{for } i = 1 \text{ and } 2 \tag{1}$$

The Y_1 and Y_2 terminals are high impedance terminals while X_1 and X_2 are low impedance terminals. The differential input voltage V_Y applied across Y_1 and Y_2 terminals is conveyed to a differential voltage V_X across the X_1 and X_2 terminals. The input currents applied to the X_1 and X_2 terminals are conveyed outward from the Z_1 and Z_2 terminals. The Z_1 and Z_2 terminals are high-impedance terminals suitable for current outputs.

In the following section of this paper, the three realizations of the FDVCCII- are presented. The principle of operation of each circuit will be described followed by SPICE simulations. A comparison is done between the three realizations showing their features and characteristics. In the last section, a novel floating gyrator is proposed using two FDVCCII- blocks and two resistors.

2. THE PROPOSED FDVCCII-

2.1. The first proposed FDVCCII-

Figure 2 shows the first new CMOS realization of the FDVCCII-. The input stage is formed from two simple differential amplifiers (M_1–M_{10}). The NMOS transistors M_1, M_2, M_5 and M_6 are matched. Also the PMOS transistors M_3, M_4, M_7 and M_8 are matched. The transistors are biased to operate in the saturation region and the two differential amplifiers are connected with each other such that

$$I_{\mathrm{M}_1} - I_{\mathrm{M}_2} = I_{\mathrm{M}_5} - I_{\mathrm{M}_6} \tag{2}$$

$$I_{\mathrm{M}_1} + I_{\mathrm{M}_2} = I_{\mathrm{M}_5} + I_{\mathrm{M}_6} \tag{3}$$

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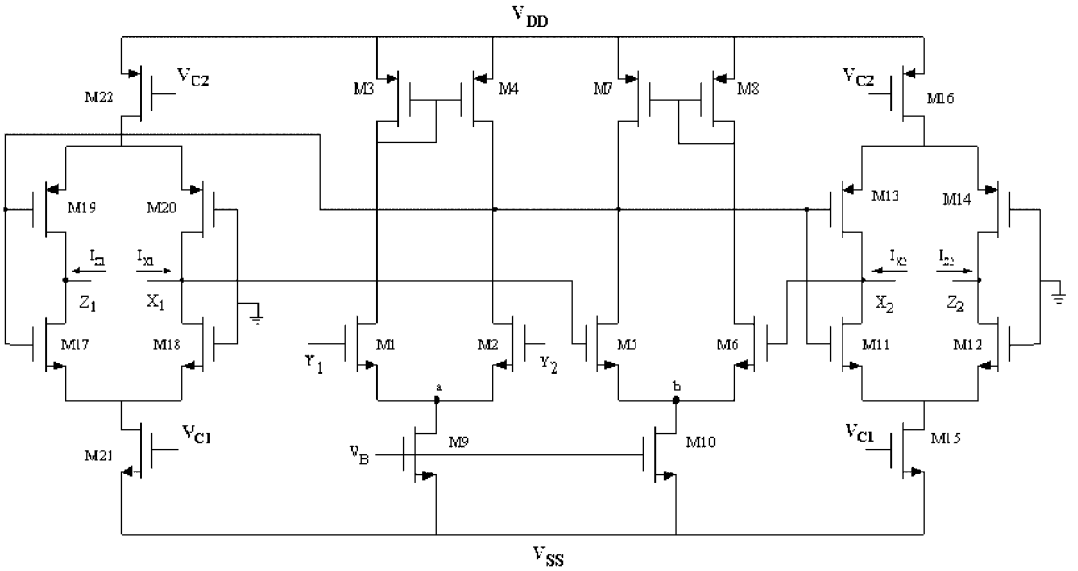

Figure 2. The first proposed FDVCCII- CMOS realization.

where

$$I_{M_1} = \frac{K}{2}(V_{Y_1} - V_a - V_T)^2 \tag{4}$$

$$I_{M_2} = \frac{K}{2}(V_{Y_2} - V_a - V_T)^2 \tag{5}$$

$$I_{M_5} = \frac{K}{2}(V_{X_1} - V_b - V_T)^2 \tag{6}$$

and

$$I_{M_6} = \frac{K}{2}(V_{X_2} - V_b - V_T)^2 \tag{7}$$

where $\{K = \mu_n C_{ox} W/L\}$ is the transconductance parameter of transistors M_1, M_2, M_5 and M_6, μ_n is the electron mobility, C_{ox} is the oxide capacitance per unit area and W/L is the aspect ratio.

Equations (2) and (3) imply that $I_{M5} = I_{M1}$ and $I_{M6} = I_{M2}$ Therefore,

$$V_{X_1} - V_b = V_{Y_1} - V_a \tag{8}$$

and

$$V_{X_2} - V_b = V_{Y_2} - V_a \tag{9}$$

Subtracting the above two equations, therefore,

$$V_{X_1} - V_{X_2} = V_{Y_1} - V_{Y_2} \tag{10}$$

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Table I. Transistor aspect ratios of the FDVCII- shown in Figure 2.

Transistor	W (μm)/L (μm)
M_1, M_2, M_5, M_6	$\frac{4.2}{1.05}$
M_3, M_4, M_7, M_8	$\frac{21}{0.7}$
M_{11}, M_{12}, M_{17}, M_{18}	$\frac{17.5}{0.35}$
M_{13}, M_{14}, M_{19}, M_{20}	$\frac{35}{0.35}$
M_9, M_{10}, M_{15}, M_{21}	$\frac{27.65}{1.05}$
M_{16}, M_{22}	$\frac{57.75}{1.05}$

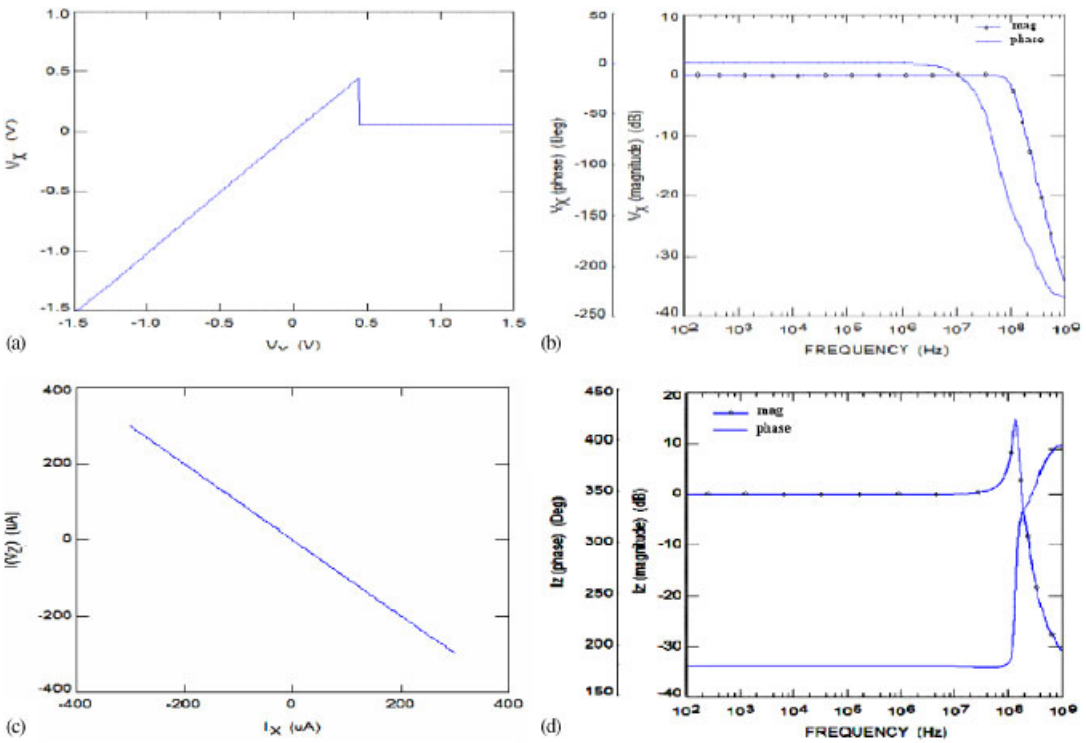

Figure 3. Simulation results of the first proposed FDVCCII-.

The output stage of the proposed FDVCCII- is formed from two floating current sources (FCSs) (M_{11}–M_{22}) to achieve the negative current following action between the Z and X terminals.

SPICE simulations of the FDVCCII- shown in Figure 2 are done. The aspect ratios of the transistors are given in Table I. The simulation results are shown in Figure 3. The DC and AC characteristics between the Y and X terminals voltages are shown in Figure 3(a), (b) and (c), respectively. The DC and AC characteristics between the X and Z terminals' currents are shown

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in Figure 3(d), (e) and (f), respectively by connecting a floating input current source I_X between X_1 and X_2 terminals while the differential voltage across Y_1 and Y_2 terminals is set to zero.

2.2. The second proposed FDVCCII-

The first proposed FDVCCII- has a limitation in the voltage linearity range as shown in the simulation results. The second new CMOS realization of the FDVCCII- offers a solution for this problem by using two NMOS and PMOS complementary differential amplifiers (M_1–M_{20}) for the input stage. The NMOS transistors pairs (M_1 and M_2), (M_7 and M_8), (M_9 and M_{10}) and (M_{15} and M_{16}) are matched. The PMOS transistor pairs (M_3 and M_4), (M_5 and M_6), (M_{11} and M_{12}) and (M_{13} and M_{14}) are also matched. The two differential amplifiers are connected with each other as shown in Figure 4. The transistors are biased properly to operate in saturation. The output stage is formed from two FCSs. The first FCS is formed of transistors (M_{21}–M_{26}). The second FCS is formed of transistors (M_{27}–M_{32}).

The analysis in Section 2.1 also applies to this circuit.

Simulation results, with aspect ratios given in Table II, are shown in Figure 5 and it is clear that the linearity has been enhanced to cover all the supply range.

2.3. The third proposed FDVCCII-

The FCS introduced in [7] was previously used as an output stage for the current conveyors [8]. The idea of using the FCS as an input stage was first introduced in the literature by Bruun [9]. The same idea is used here to build the third proposed FDVCCII-. A new symbolic representation of the FCS shown in Figure 6(a) is given in Figure 6(b). For the transistors working in saturation,

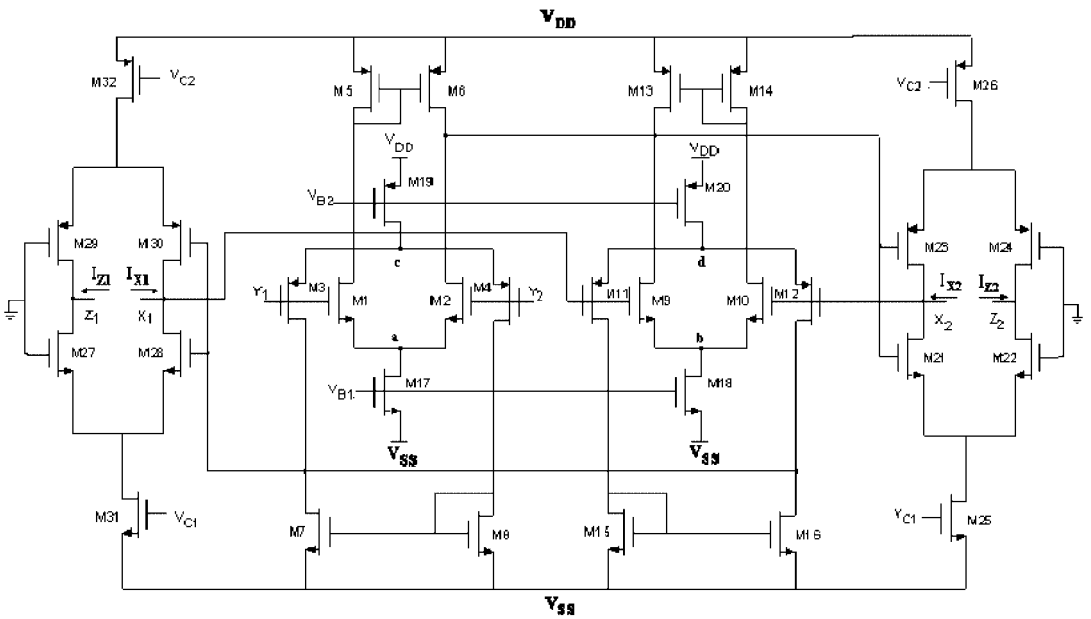

Figure 4. The second proposed FDVCCII- CMOS realization.

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Table II. Transistor aspect ratios of the FDVCII- shown in Figure 4.

Transistor	W (μm)/L (μm)
M_1, M_2, M_9, M_{10}	$\frac{4.2}{1.05}$
M_3, M_4, M_{11}, M_{12}	$\frac{10.5}{1.05}$
M_7, M_8, M_{15}, M_{16}	$\frac{6.3}{0.7}$
M_5, M_6, M_{13}, M_{14}	$\frac{21}{0.7}$
M_{17}, M_{18}, M_{25}, M_{31}	$\frac{27.65}{1.05}$
M_{19}, M_{20}, M_{26}, M_{32}	$\frac{57.75}{1.05}$
M_{21}, M_{22}, M_{27}, M_{28}	$\frac{17.5}{0.35}$
M_{23}, M_{24}, M_{29}, M_{30}	$\frac{35}{0.35}$

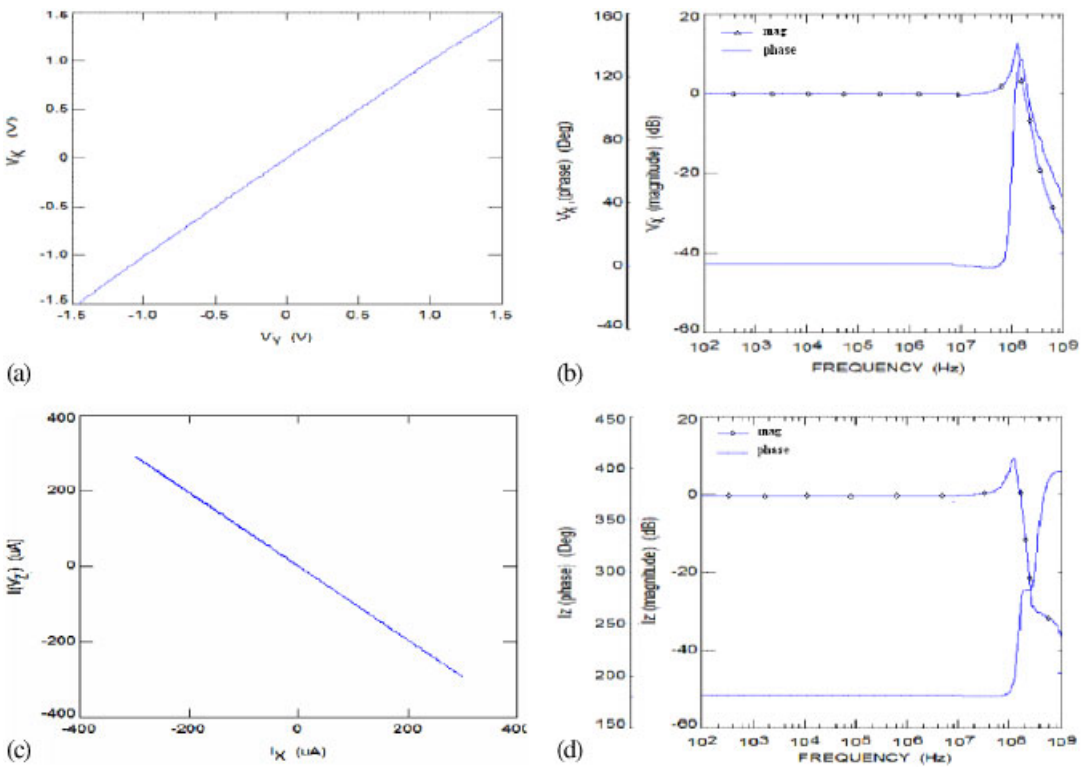

Figure 5. Simulation results of the second proposed FDVCCII-.

the relation between the terminals' currents and voltages can be given by

$$I_{Z_1} = -I_{Z_2} = -\frac{1}{2} v_d \left(\sqrt{K_n} \sqrt{2I_B - \frac{K_n v_d^2}{4}} + \sqrt{K_p} \sqrt{2I_B - \frac{K_p v_d^2}{4}} \right) \tag{11}$$

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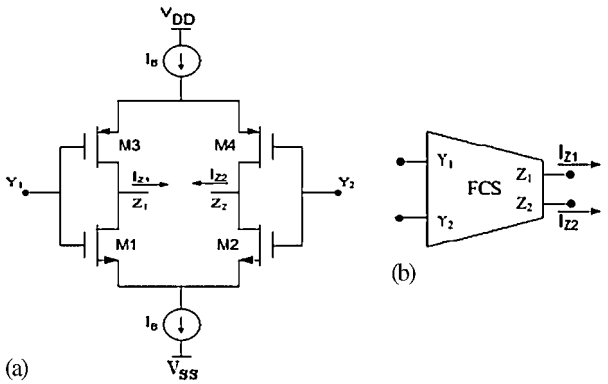

Figure 6. (a) The CMOS FCS circuit [4] and (b) a proposed symbolic representation of the FCS.

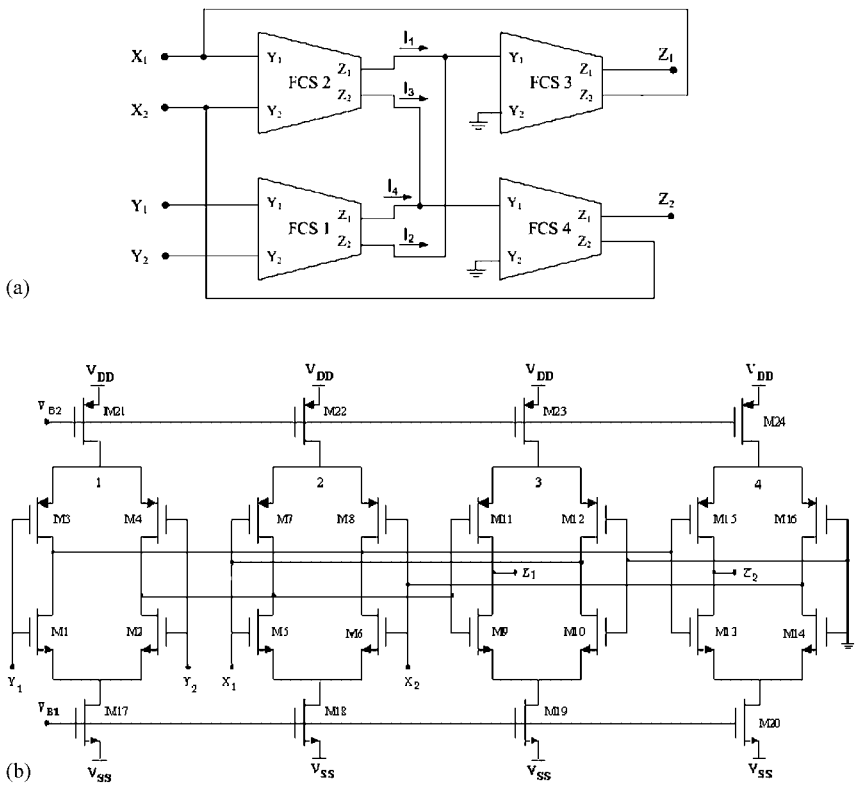

Figure 7. (a) The third proposed FDVCCII- block diagram; (b) the third proposed FDVCCII- CMOS realization.

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Table III. Transistor aspect ratios of the FDVCII- shown in Figure 7(b).

Transistor	W (μm)/L (μm)
M_1, M_2, M_5, M_6	$\frac{1.05}{2.1}$
M_3, M_4, M_7, M_8	$\frac{2.1}{2.1}$
M_9, M_{10}, M_{13}, M_{14}	$\frac{17.5}{0.35}$
M_{11}, M_{12}, M_{15}, M_{16}	$\frac{35}{0.35}$
M_{17}, M_{18}, M_{19}, M_{20}	$\frac{27.65}{1.05}$
M_{21}, M_{22}, M_{23}, M_{24}	$\frac{57.75}{1.05}$

where

$$v_d = V_{Y_1} - V_{Y_2}, \quad K_n = \mu_n C_{ox} \frac{W_{1,2}}{L_{1.2}} \quad \text{and} \quad K_p = \mu_p C_{ox} \frac{W_{3,4}}{L_{3.4}} \tag{12}$$

Figure 7(a) shows the block diagram of the third proposed FDVCCII-. The CMOS circuit realization of the third FDVCCII- is given in Figure 7(b). The input stage is formed from two of the FCSs numbers 1 and 2 for the voltage following action. The output stage is formed from the FCSs numbers 3 and 4 for the current following action.

From Figure 7(a) it is seen that

$$I_1 = -I_2, \quad I_3 = -I_4 \tag{13}$$

By substituting (11) in (13)

$$\frac{1}{2}(V_{X_1} - V_{X_2}) \left(\sqrt{K_n} \sqrt{2I_B - \frac{K_n (V_{X_1} - V_{X_2})^2}{4}} + \sqrt{K_p} \sqrt{2I_B - \frac{K_p (V_{X_1} - V_{X_2})^2}{4}} \right)$$
$$= \frac{1}{2}(V_{Y_1} - V_{Y_2}) \left(\sqrt{K_n} \sqrt{2I_B - \frac{K_n (V_{Y_1} - V_{Y_2})^2}{4}} + \sqrt{K_p} \sqrt{2I_B - \frac{K_p (V_{Y_1} - V_{Y_2})^2}{4}} \right) \tag{14}$$

From the above equation therefore,

$$V_{X_1} - V_{X_2} = V_{Y_1} - V_{Y_2} \tag{15}$$

Thus, the voltage following action is achieved.

The FCSs numbers 3 and 4 provide the current following action and results in

$$I_{Z_1} = -I_{X_1} \quad \text{and} \quad I_{Z_2} = -I_{X_2} \tag{16}$$

The aspect ratios of the transistors used are given in Table III.

Simulation results are shown in Figure 8.

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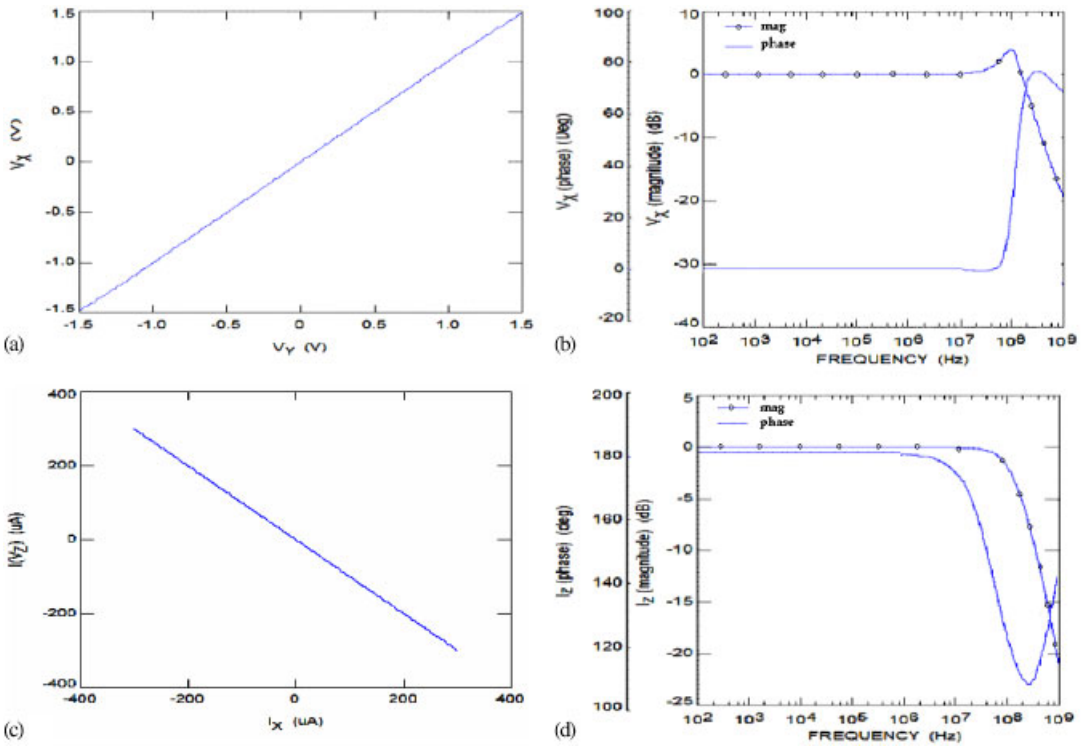

Figure 8. Simulation results of the third proposed FDVCCII-.

3. COMPARISON AND DISCUSSION

A comparison is done between the three proposed FDVCCII- circuits. From Table IV, one can easily notice that the three circuits offer very high bandwidths in voltages and currents transfer gains. Also the second and third FDVCCII- have rail to rail linear region in voltage input range. The three circuits also offer very small offset in voltages and currents. Also simulation results for the total harmonic distortion (THD) and the power dissipation are shown in Table IV. It is clear that the second realization offers the best performance from the THD point of view. It has, however, the highest power consumption.

The third realization of the FDCCII- given in Figure 7(b) has the lowest power dissipation among the three realizations given in this paper.

4. A FLOATING GYRATOR

Gyrators [10, 11] and floating gyrators [12] are important building blocks in active circuits.

A new floating gyrator circuit is proposed in this section. The proposed gyrator is shown in Figure 9. It uses two FDVCCII- blocks and two resistors and it has two floating ports.

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Table IV. Parameters of the three FDVCCII-.

Parameters	Units	The first proposed FDVCCII-	The second proposed FDVCCII-	The third proposed FDVCCII-
Input voltage range (V_Y)	V	−1.5 to 0.44	−1.5 to 1.5	−1.5 to 1.5
Voltage offset	mV	3.27	2.76	−0.59
3 dB bandwidth of open circuit voltage transfer gain (V_X/V_Y)	MHz	116	232	206
Input current range (I_X)	μA	−300 to 300	−300 to 300	−300 to 300
Current offset	nA	1.5	0.165	−0.304
3 dB bandwidth of current transfer gain (I_Z/I_X)	MHz	195	180	230
THD for a 10 MHz, 1 Vp-p sinusoidal signal at V_Y		0.5%	0.15%	0.3%
Power dissipation	mW	5	8.8	1.9
Number of transistors		22	32	24

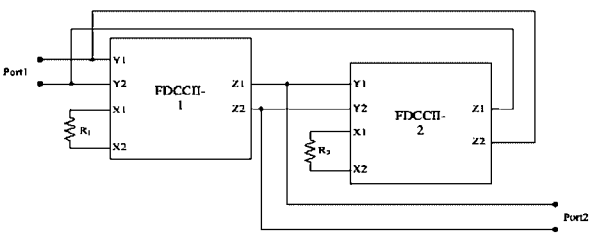

Figure 9. The proposed floating gyrator.

The transmission matrix of the proposed gyrator is given by

$$T = \begin{pmatrix} 0 & -R_1 \\ -\dfrac{1}{R_2} & 0 \end{pmatrix} \tag{17}$$

If port 2 of the gyrator is terminated by a capacitor C, a floating inductor, of inductance $L = C R_1 R_2$ is realizable at port 1.

As a design example, a second-order low-pass filter is simulated using this floating inductor and the simulation results are compared with the ideal response when using an ideal floating inductor. The FDVCCII- used in simulations is the one given in Figure 4. The low-pass filter component values are chosen to achieve $\omega_o = 50$ Mrad/s and maximally flat response. Simulations are shown in Figure 10.

5. CONCLUSIONS

Three new CMOS realizations for the FDVCCII- have been presented. The first two realizations are based on using differential amplifiers for the input stage and FCSs for the output stage of

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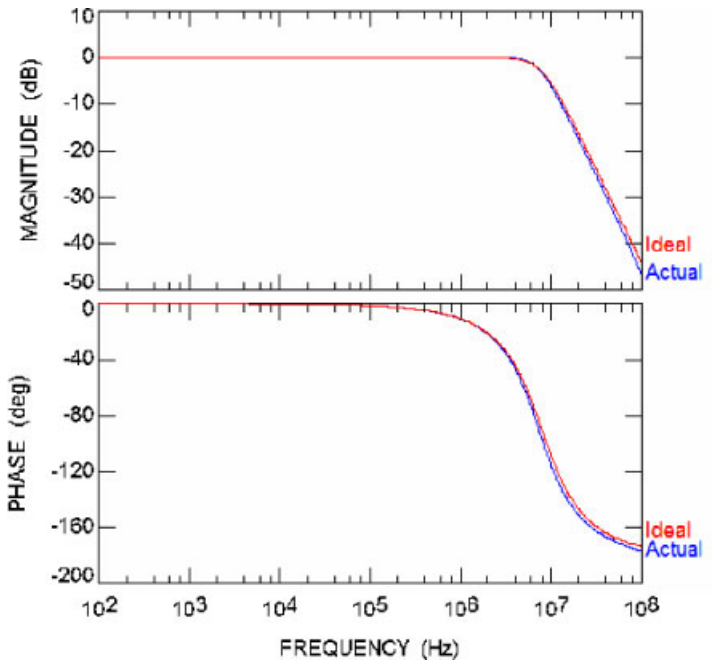

Figure 10. AC response of the low-pass filter compared with the ideal curves.

the FDVCCII-, respectively. The third realization is totally based on using the FCSs for both the input and output stages. Spice simulations to demonstrate circuit performance are given. A floating gyrator using the FDVCCII- is also included and is used in realizing a floating inductor.

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