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LETTER

A CMOS differential difference operational mirrored amplifier

Ahmed Soltan[a], Ahmed M. Soliman[b,*]

[a] *Electronics and Communications Engineering Department, University of Fayoom, Egypt*
[b] *Electronics and Communications Engineering Department, Faculty of Engineering, Cairo University, Egypt*

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Abstract

Design of a high-performance differential difference operational mirrored amplifier is presented. The proposed circuit is useful for continuous-time analog signal processing. The circuit is developed using folded cascode amplifier and the floating current source. Several applications including grounded resistor, voltage amplifier, grounded inductor and oscillator circuit are presented. Simulation results for the DDOMA circuit and its applications are given.

Keywords: Operational mirrored amplifier; Grounded resistor; Integrator; Simulated inductor; Oscillator

1. Introduction

Analog circuit design using the current mode approach has recently gained considerable attention. This stems from its inherent advantages of wide bandwidth, high slew rate, low-power consumption and simple circuitry.

One of the standard techniques to extend the dynamic range of analog blocks is to use fully differential (FD) signal processing [1,2]. It can extend the dynamic range over order of magnitude through the cancellation of the even harmonics, as well as the suppression of all undesirable signals generated by analog or digital blocks in mixed mode circuits.

The purpose of this paper is to introduce a differential difference operational mirrored amplifier (DDOMA). The proposed block diagram is derived from that of the single ended operational mirrored amplifier (OMA). The OMA is a general purpose current mode building block and basically a very high-gain transconductance scheme with identical output currents [3–5].

In this paper, CMOS realization of the proposed DDOMA is given in Section 2. Specific DDOMA-based applications such as MOS grounded resistor, voltage-to-current converter, differential voltage amplifier and simulated grounded inductor are introduced in Section 3. Simulation results using PSPICE for the DDOMA circuit and its applications that verify the analytical results are also provided after each application.

For all circuits examined in this paper, the supply voltages are ± 1.5 V. PSPICE simulations were carried out with model parameters of 0.25 μm level 3 CMOS process provided by MOSIS.

2. Proposed design

The OMA comprises a nullator ($V_1 = 0$, $I_1 = 0$) at one port and a current mirror at the other port with arbitrary voltage as illustrated in Fig. 1(a). According to the definition of the OMA, an ideal OMA symbolically shown in Fig. 1(b) exhibits these terminal characteristics: $I_1 = I_2 = 0$, $V_1 = V_2$ and $I_{o1} = I_{o2}$. According to the OMA definition, its differential

* Corresponding author.
E-mail address: asoliman@ieee.org (A.M. Soliman).

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difference version with its symbol shown in Fig. 2(a) is a six-terminal device that can be characterized by the following equations:

$$I_{1P} = I_{1n} = I_{2P} = I_{2n} = 0 \quad (1)$$

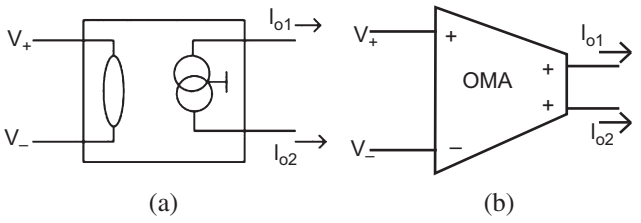


Fig. 1. (a) Pathological element representation of the OMA. (b) Symbol of the OMA.

$$V_{1d} = V_{1P} - V_{1n} = V_{2d} = V_{2P} - V_{2n} \quad (2)$$

$$I_{o1} = I_{o2} \quad (3)$$

The block diagram and the CMOS realization of the proposed DDOMA are shown in Fig. 2(b) and (c), respectively. As shown in the block diagram, the input stage of the proposed design consists of two differential pairs with active load M1–M8. The two differential pairs convert the two differential voltages into two currents.

The output currents of the input stage are subtracted and converted into a voltage with a high gain using the self-biased complementary folded cascode (SB-CFC) amplifier M9–M16. The folded cascode (FC) [6] amplifier is used because it gives wide bandwidth and fast settling operation.

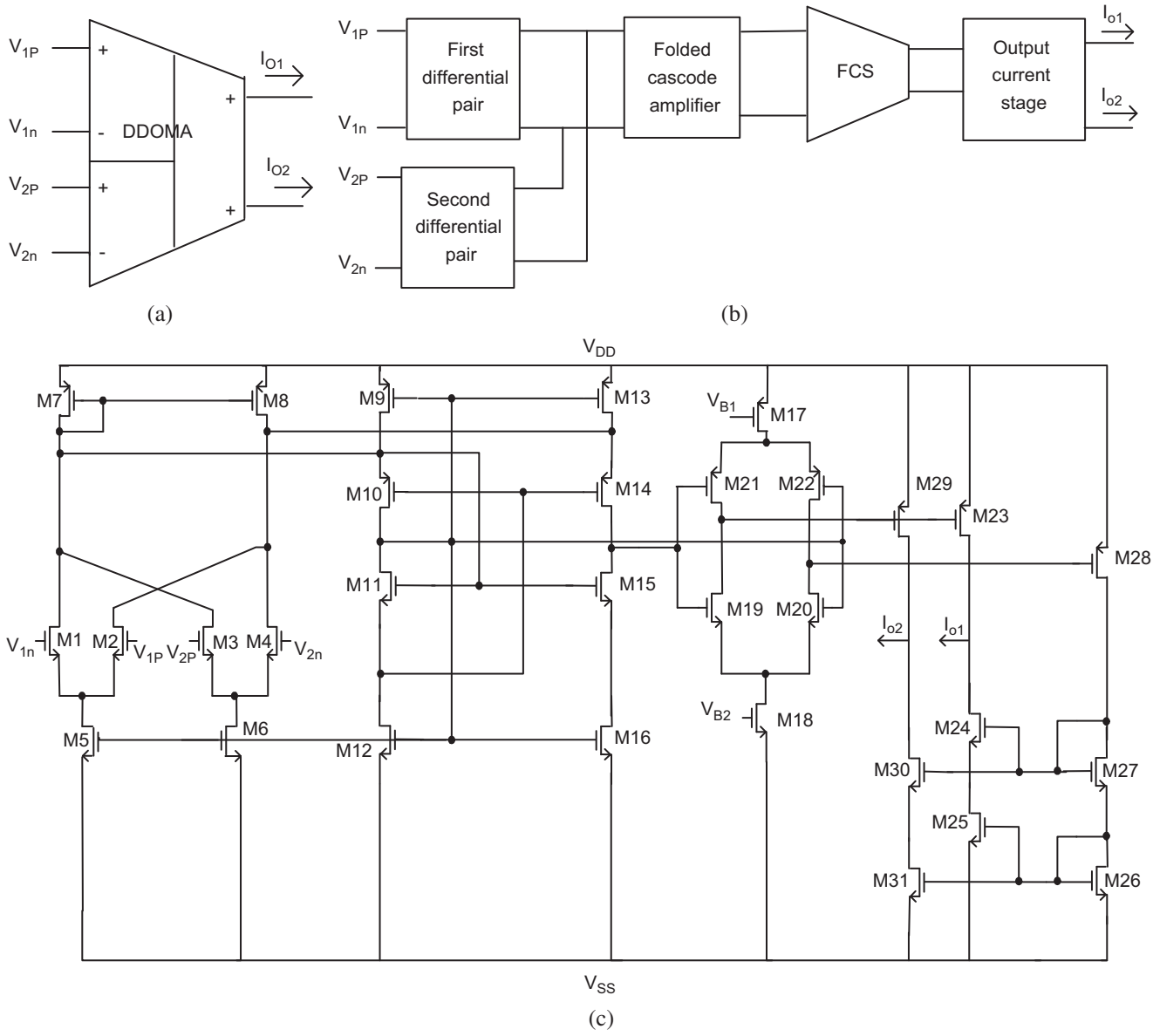
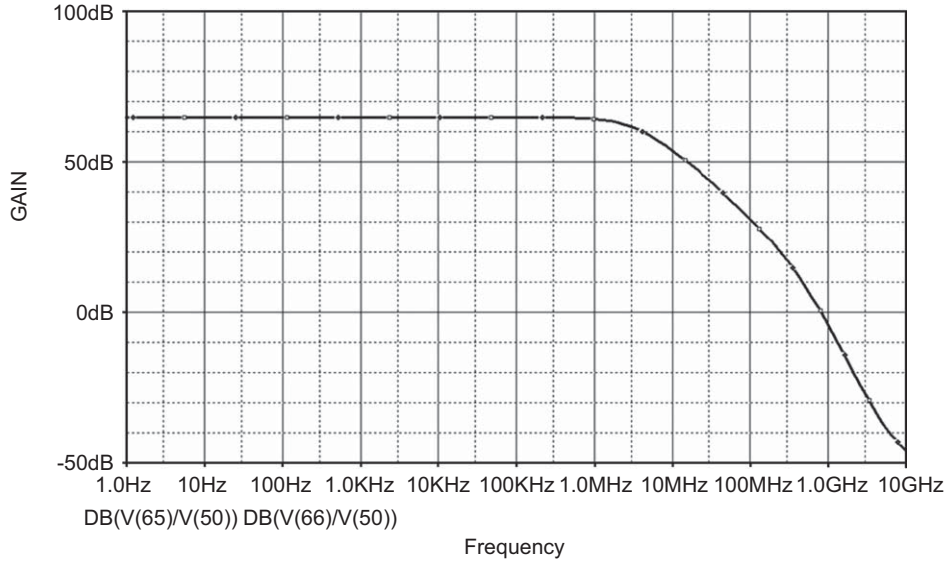
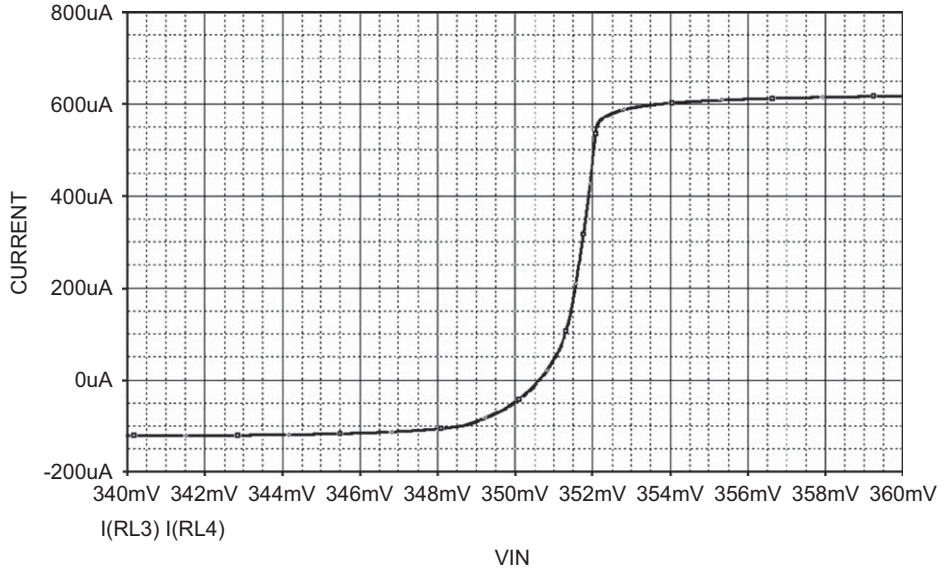


Fig. 2. (a) Symbol of the DDOMA. (b) The block diagram of the proposed DDOMA. (c) The proposed DDOMA CMOS realization.



(a)



(b)

Fig. 3. (a) The gain of the proposed DDOMA. (b) The DDOMA input voltage range.

Table 1. Transistor aspect ratios for the proposed DDOMA circuit

Transistor	Aspect ratio W/L
M1–M4	170/0.25
M5, M6	155/0.25
M7, M8	250/0.25
M9, M10	35/1.25
M11, M12	20/1.25
M13, M14	65/1.25
M15, M16	60/1.25
M17–M22	50.5/0.25
M23, M29	300/0.5
M24–M27, M30, M31	20/5
M28	16/8

Table 2. A summary of the simulation results for the DDOMA

Parameter	Simulation results
DC power dissipation	148 mW
Gain	64 Db
Input range	350–353 mV
Unity gain frequency	820 MHz
3-dB bandwidth	3 MHz
THD for a sinusoid of 30 kHz	72.3%
Noise level	$0.4\,\text{nv}/\sqrt{\text{Hz}}$

But the FC amplifier uses large number of external bias voltage, so the SB-CFC [7] is used, which does not need any external bias voltage.

The amplified voltage is converted into two balanced currents I_{o1} and I_{o2} by using floating current source (FCS) [8–10] M17–M22 and a current output stage M23–M31 to provide the required currents. The outputs of the circuit can be expressed as

$$I_{o1} = I_{o2} = G_m[(V_{1P} - V_{1n}) - (V_{2P} - V_{2n})] \quad (4)$$

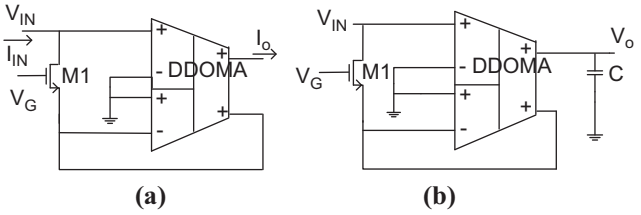


Fig. 4. (a) DDOMA-based grounded resistor. (b) Integrator using the grounded resistor.

$$G_m = (g_{m4} + g_{m2})[r_{d3}//r_{d1}//r_{d7}] \times [r_{d15}r_{d16}g_{m15}//r_{d14}r_{d13}g_{m14}] \times (g_{m19} + g_{m21})(r_{d20}//r_{d22})g_{m28} \quad (5)$$

where G_m is the open loop transconductance. Analogous to the traditional op-amp, when negative feedback is applied the differential voltage of the two input ports become equal.

$$V_{1P} - V_{1n} = V_{2P} - V_{2n} \quad \text{as } G_m \longrightarrow \infty \quad (6)$$

As the finite open loop transconductance G_m decreases, the difference between the two differential voltages increases. Therefore, the open loop transconductance is required to be as large as possible in order to improve the performance.

The open loop transconductance of the proposed DDOMA is shown in Fig. 3. It is obtained using the PSPICE

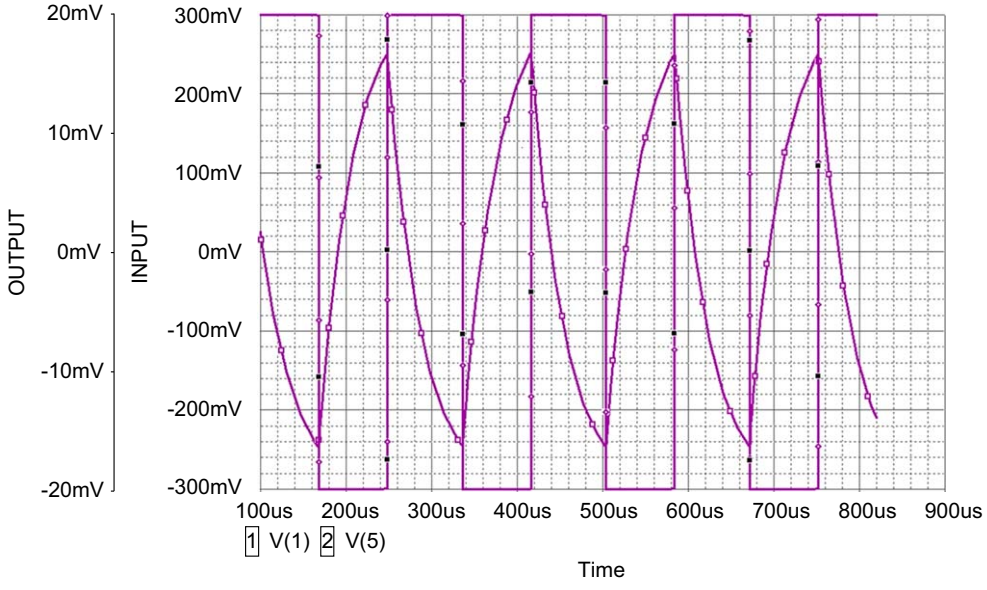


Fig. 5. (a) The integrator output. (b) The voltage-to-current converter output.

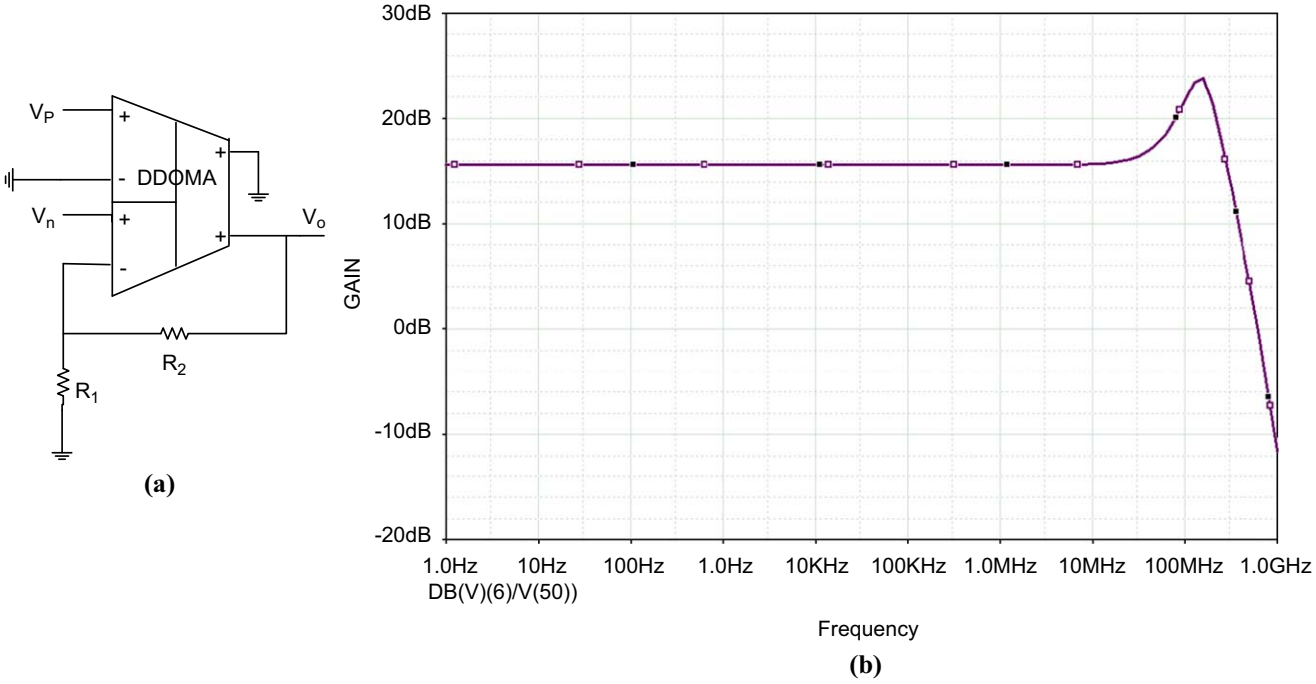


Fig. 6. (a) The differential voltage amplifier using DDOMA. (b) The gain of the voltage amplifier.

simulation with the transistor aspect ratios given in Table 1, supply voltage of $\pm 1.5\,\mathrm{V}$, $V_{B1} = 0.5\,\mathrm{V}$ and $V_{B2} = -0.5\,\mathrm{V}$. Other simulation results are given in Table 2.

3. Design examples

The following sub-sections demonstrate the design of several fundamental applications based on the proposed DDOMA. First the design of grounded resistance and integrator are given. Second a differential voltage amplifier is presented. Finally, a simulated grounded inductor is presented. The PSPICE simulation results are given to verify the concepts.

3.1. DDOMA-based grounded resistor

The DDOMA-based grounded resistor is shown in Fig. 4(a). The input current of the circuit equals the linearized drain current of the MOS transistor, which is given by

$$I_{IN} = 2K(V_G - V_T)V_{IN} \quad \text{for } V_G \geqslant |V_{IN}| + V_T \tag{7}$$

$$K = \mu_n C_{ox}\left(\frac{W}{L}\right)_n$$

where μ_n is the electron mobility, C_{ox} is the gate oxide capacitance, $(W/L)_n$ is the aspect ratio of the NMOS transistor.

Therefore, the circuit is equivalent to a voltage controlled grounded resistor with a magnitude given by

$$R = \frac{1}{2K(V_G - V_T)} \tag{8}$$

An inverting integrator using the grounded resistor can be realized as shown in Fig. 4(b), and the output voltage is given by

$$V_O = -\frac{2K(V_G - V_T)}{sC}V_{IN} \tag{9}$$

The circuit shown in Fig. 4(a) also realizes an inverting voltage-to-current converter by using the extra output terminal of the DDOMA. The output current is given by

$$I_O = -2K(V_G - V_T)V_{IN} \tag{10}$$

PSPICE simulation results of the integrator and the voltage-to-current converter is shown in Fig. 5(a) and (b), respectively.

3.2. Differential voltage amplifier

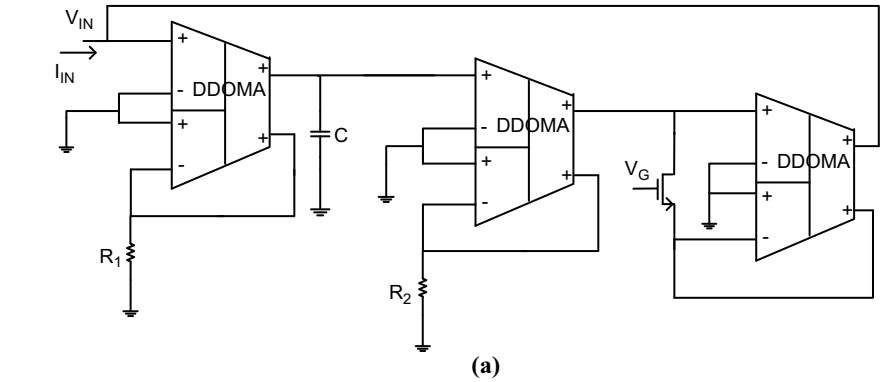
A differential voltage amplifier can be realized as shown in Fig. 6(a) with the output voltage given by

$$V_O = -(V_P - V_n)\left(1 + \frac{R_2}{R_1}\right) \tag{11}$$

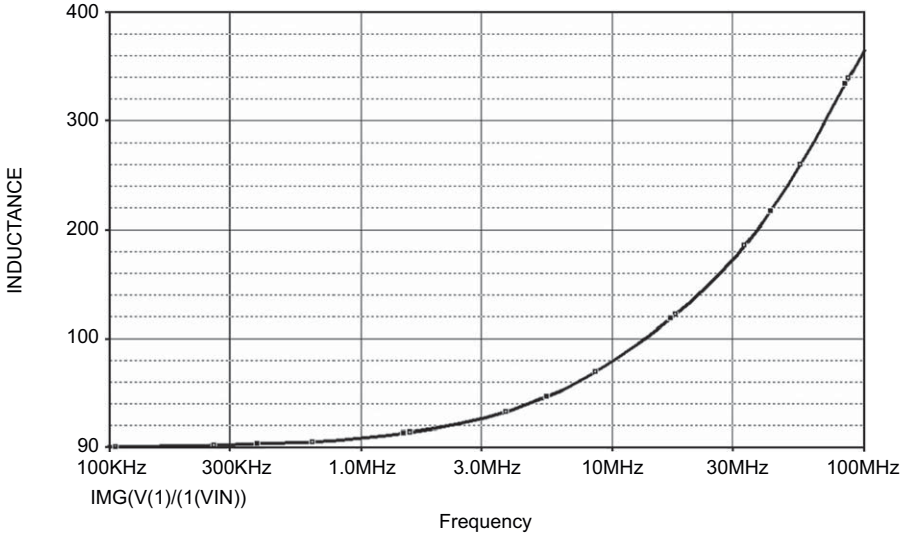
The simulation results of the amplifier using PSPICE is shown in Fig. 6(b). As shown in Fig. 6(b), the amplifier can work to a very wide bandwidth as it reaches to 300 MHz.

3.3. DDOMA simulated inductor

Simulated inductors employing active elements [11] are widely used in various applications. A simulated inductor



(a)



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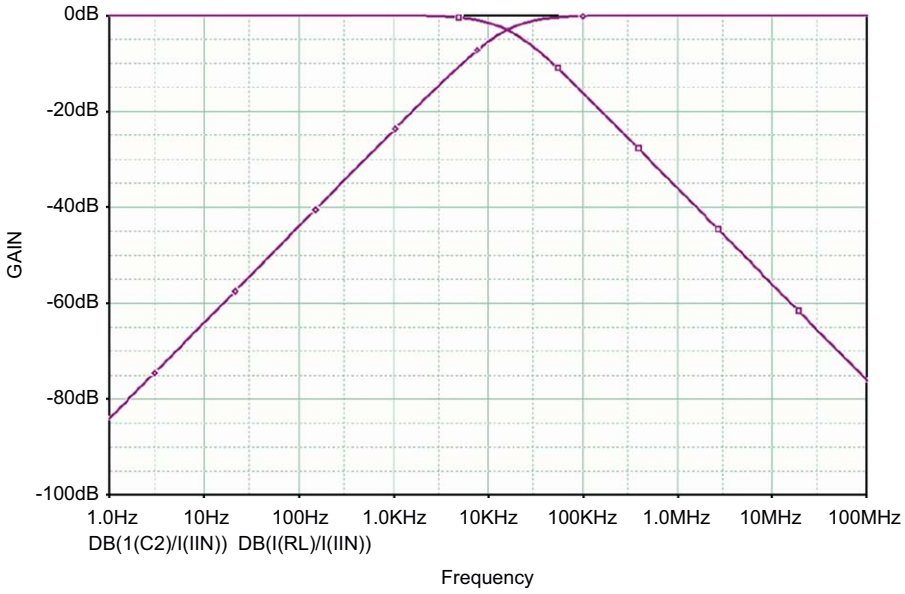

(c)

Fig. 7. (a) The simulated grounded inductor using the DDOMA. (b) The input impedance of the inductor. (c) Low-pass and high-pass filter response using the proposed inductor.

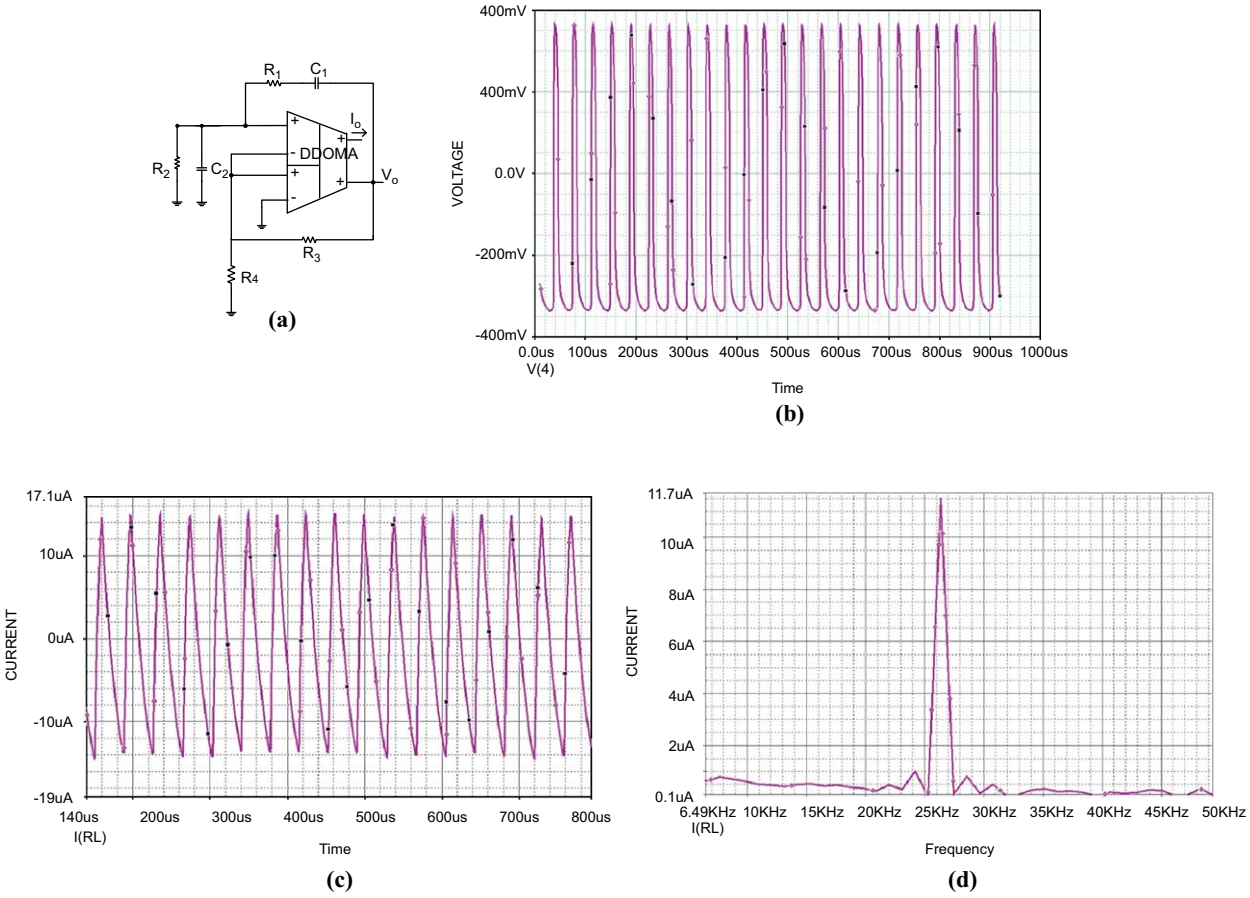

Fig. 8. (a) The oscillator circuit using the DDOMA. (b) The voltage wave form of the oscillator. (c) The current wave form of the oscillator. (d) The frequency spectrum of the osillator.

can be realized by using three DDOMA, one floating capacitor and two floating resistors as shown in Fig. 7(a). The simulated inductance of the simulated inductor is given by

$$L = CR_1R_2 \tag{12}$$

PSPICE simulation shown in Fig. 7(b) is done to verify that the input impedance of the circuit of Fig. 7(a) behaves as an inductor.

As a design example, a second-order low pass and high-pass filter is simulated using the proposed inductor. The simulation results of the filter are shown in Fig. 7(c). The filter component values are chosen to a achieve $f_o = 25\,\text{kHz}$.

3.4. DDOMA-based oscillator

Different oscillator circuits are introduced in [11–14]. New proposed oscillator circuit employing one DDOMA, two resistors and two capacitors is shown in Fig. 8(a). The condition of oscillation and the radian frequency are given by

$$\frac{K}{2} = 1 + \frac{C_2}{C_1} + \frac{R_1}{R_2} \tag{13}$$

$$\omega_o = \frac{1}{\sqrt{C_1C_2R_1R_2}} \tag{14}$$

where K is given by

$$K = 1 + \frac{R_3}{R_4} \tag{15}$$

This oscillator circuit has both voltage output and current output as shown in Fig. 8(a).

PSPICE simulations of the oscillator was performed, taking $C_1 = C_2 = 0.5\,\text{nF}$, $R_1 = 5\,\text{k}\Omega$, $R_2 = 20\,\text{k}\Omega$, $R_3 = 12\,\text{k}\Omega$ and $R_4 = 4\,\text{k}\Omega$. To start oscillation, R_3 was increased to $12.2\,\text{k}\Omega$. Fig. 8(b) and (c) represents the output voltage and current waveforms, respectively, and Fig. 8(d) represents the frequency spectrum, from which it is seen that $f_o = 26.3\,\text{kHz}$.

4. Conclusion

In this paper, the design of wide range and low-power DDOMA has been presented. The DDOMA is realized using the self-biased complementary folded cascode amplifier because it gives a wide bandwidth in the operation. Design

examples including grounded resistance, integrator, differential amplifier, grounded inductor and DDOMA-based oscillator are given. PSPICE simulation results for all applications are given to confirm the analytical results.

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Ahmed Soltan El-sheekh was born in Cairo Egypt, on July 22, 1982. He received his B.Sc. degrees in Electronics and Communications Engineering from Cairo University Fayoum branch, Fayoum, Egypt in 2004. He is currently working as a Teacher Assistant in Department of Electronics and Communications Engineering, Fayoum University since his graduation. His research interests include analog circuits with particular emphasis on current-mode approach and RF power amplifers and VCO.

Ahmed M. Soliman was born in Cairo Egypt, on November 22, 1943. He received his B.Sc. degree with honors from Cairo University, Cairo, Egypt, in 1964, the M.S. and Ph.D. degrees from the University of Pittsburgh, Pittsburgh, PA, USA, in 1967 and 1970, respectively, all in Electrical Engineering.

He is currently Professor in Electronics and Communications Engineering Department, Cairo University, Egypt.

From September 1997 to September 2003, Dr. Soliman served as Professor and Chairman of Electronics and Communications Engineering Department, Cairo University, Egypt.

From 1985 to 1987, Dr. Soliman served as Professor and Chairman of the Electrical Engineering Department, United Arab Emirates University, and from 1987 to 1991 he was the Associate Dean of Engineering at the same University.

He has held visiting academic appointments at San Francisco State University, Florida Atlantic University and the American University in Cairo.

He was a visiting scholar at Bochum University, Germany (Summer 1985) and with the Technical University of Wien, Austria (Summer 1987).

In 1977, Dr. Soliman was decorated with the First Class Science Medal, from the President of Egypt, for his services to the field of Engineering and Engineering Education.

Dr. Soliman is a Member of the Editorial Board of the IEE Proceedings Circuits, Devices and Systems.

Dr. Soliman is a Member of the Editorial Board of Analog Integrated Circuits and Signal Processing.

Dr. Soliman served as Associate Editor of the IEEE Transactions on Circuits and Systems I (Analog Circuits and Filters) from December 2001 to December 2003 and is Associate Editor of the Journal of Circuits, Systems and Signal Processing from January 2004 to till now.