ured instead of 25.2GHz when simulated). The results are presented in Fig. 5.

When the parasitic patches operate, the bandwidth is increased from 400 for a single resonator (1.6%) to 640MHz for an array antenna (2.7%). The adaptation at the resonant frequency ($S11$ = −15dB at 25.7GHz) is not good enough to obtain the expected 1.2GHz bandwidth.

The gain of the array antenna is 3dB at the resonant frequency instead of 5dB as expected. This difference between the simulated and measured results can be explained by a mismatch of the antenna.

Conclusion: We have fabricated a compact monolithic photolithography antenna with a widened bandwidth. The discrepancies between the simulated and measured values of the gain and bandwith can be attributed to rather incomplete knowledge of the losses in the dielectrics. These points have to be investigated further.

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Low-power CMOS current conveyor

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A novel second-generation CMOS current conveyor based on a new adaptive biasing technique is proposed. It is shown that the use of this circuit offers an excellent performance and leads to a significant reduction in the standby power dissipation. PSPICE simulation results assuming 0.5μm CMOS process are also given.

Introduction: Although lower supply voltage directly translates to lower power consumption in digital circuits, a similar conclusion cannot be drawn for analogue circuits. Low-power analogue design, therefore, raises its own challenge [1 – 7]. Owing to economic constraints, the standard CMOS technology is suitable for use in many applications. Recently, analogue CMOS current-mode circuits have received a great deal of interest because they can operate under low voltage supplies since the current-mode substitutes current swings for voltage swings in the signal propagation [1 – 3]. The second-generation current conveyor (CCII) is the most versatile building block in current-mode signal processing [1, 2]. Many realisations of the CCII in the literature based on a feedback-stabilised voltage follower have been developed in order to obtain accurate voltage-following action between node Y and node X [4 – 6]. In these realisations, differential amplifiers with high current tails are required to obtain high open-loop gain. This leads to high power consumption in addition to a slew rate limited performance. In this Letter, a novel CMOS realisation based on an adaptively biased differential pair structure is introduced.

Circuit description: Consider the circuit shown in Fig. 1. In this circuit, which is the class AB version of that reported in [4], a negative feedback is applied on two long tail differential pairs (LTP) in such a way as to force them to follow the same value of current driven from the node X. The local feedback actions on the drains of M2 and M3 lead to an exact voltage following with a negligible DC offset and a small input resistance [4]. A sufficiently high current source value I_B should be chosen in order not to limit the maximum current driven from node X.

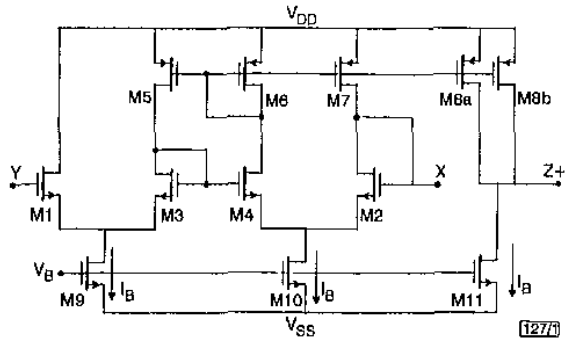

Fig. 1 *Circuit configuration of class AB long tail-based CCII*

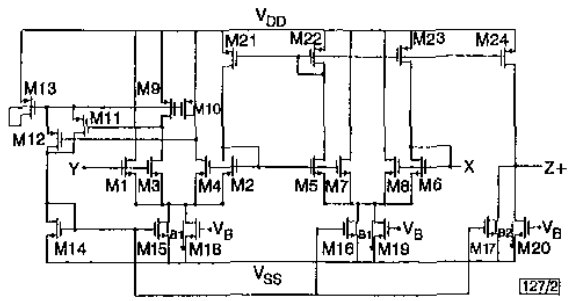

Fig. 2 *Circuit configuration of proposed CCII*

Consider the circuit shown in Fig. 2. Transistors M1–M2 and M5–M6 have the same role as in the circuit shown in Fig. 1. To control the value of the current tails of the two LTP structures, an adaptive biasing action is effected by means of transistors M3 - M4, the high-speed current-mode maximum sub-circuit M9–M13 (reported in [7]) and the current mirrors M14–M17. Consequently, the larger the current driven from node X, the higher the biasing current for the two LTPs. Standby current sources (M18–M20) are needed to prevent the LTP structures from turning off, thus avoiding cross-over distortion and frequency response limitation. It is noted that, to obtain low power consumption, the aspect ratios of transistors M3–M4 and M7–M8 are small compared with those for M1–M2 and M5–M6. Also, the aspect ratios of all the remaining transistors are optimised as shown in Table 1. The current at node X is reproduced at node Z+ through current mirrors M17, M20 and M24.

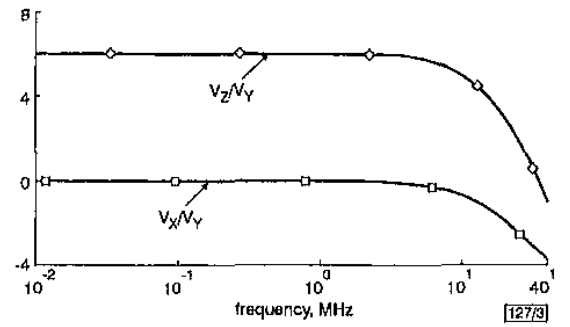

Fig. 3 *Frequency characteristics of CCII*

□ *DB* (*V*(*x*))
◇ *DB* (*V*(*cc*))

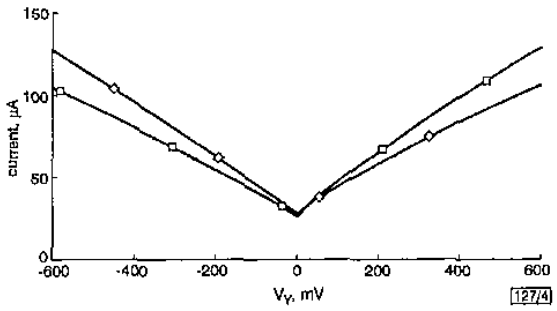

Fig. 4 *Current driven from supplies to CCII*

□ *I* (positive supply)
◇ *I* (negative supply)

Table 1: W/L of transistors of circuit shown in Fig. 2

Transistor	Aspect ratio
M1–M2, M5–M6	10/1
M3–M4, M7–M8	2/1
M9–M10	11.5/2.5
M11–M12	1/0.5
M13	10/2.5
M14	6/1.5
M15–M16	72/1.5
M17	60/1.5
M18–M19	6/1.5
M20	5/1.5
M21–M23	11.5/2.5
M24	23/2.5

PSPICE simulations: The performances of the CCII shown in Fig. 2 are simulated using PSPICE. Transistor aspect ratios are given in Table 1 and a 0.5μm MIETEC CMOS process is assumed. The supply voltages are $V_{DD} = -V_{SS} = 1.5$V, and I_{B1} is set to 6μA. Table 2 shows a summary of the results of the simulations.

Table 2: Summary of simulation results

THD	50dB
Input resistance R_x	2Ω
Open-loop gain	42dB
3dB frequency (voltage amplifier topology)	30MHz
Standby current	32μA
Voltage offset (from Y to X)	0.05mV
Current offset (from X to Z+)	0.8μA

Fig. 3 shows the voltage transfer characteristics from node Y to node X and to node Z+ when node X is terminated by $R_x = 40$kΩ and $R_z = 80$kΩ. V_Y is set to 0.5Vp-p.

Fig. 4 shows the current driven from the supplies when the voltage V_Y is scanned from -0.6V to 0.6V with the same R_x and R_z. It is clear that, when node Y is at ground, the standby power consumption is very low.

Conclusion: In this Letter, the novel realisation of a CCII has been introduced. Simulation results show that the circuit exhibits excellent performance while consuming low standby power, which makes it suitable for low-power analogue signal processing.

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Realisation of exponential V-I converter using composite NMOS transistors

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A CMOS voltage-to-current converter with exponential characteristics is presented. The Taylor's series expansion is used for realising the exponential function. In a 0.35μm CMOS process, the HSPICE simulation results show a 15dB linear range with a linearity error of < ±0.5dB. The total power consumption is < 0.8mW with ±1.5V supply voltage. The circuit can be used in the design of a variable gain amplifier (VGA).

Introduction: Since there is no intrinsic logarithmic MOS device operating in the saturation region for CMOS technologies, one method to generate the exponential characteristics is by use of a 'pseudo-exponential' generator [1, 2]. Alternatively, the Taylor's series expansion can also be used for implementation of the exponential [3]. According to the Taylor's series expansion, a general exponential function can be expressed as

$$\exp(ax) \simeq 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 + \frac{a^3}{3!}x^3 + \cdots + \frac{a^n}{n!}x^n + \cdots \quad (1)$$

where a is the coefficient and x is the independent variable; if $|ax| \ll 1$, the higher order terms of eqn. 1 can be neglected and the final approximation equation can be given as [3]

$$\exp(ax) \simeq 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 \quad (2)$$

Eqn. 2 can be implemented by the composition of a V-I squarer circuit, a linear V-I converter and a constant bias current which are equivalent to the second-order, the first-order and the zero-order terms in eqn. 2 [3]. In this Letter, a simple and universal approach is presented to realise eqn. 2. Simulation results will be given to verify the validity of the approach.

Circuit implementation: Consider the composite NMOS transistor [4] shown in Fig. 1. Assuming that transistors M1 and M2 are identical and that both of them operate in the saturation region without body effects, the following equation applies:

$$Id1 + Id2 = \frac{Kn}{2}(Vin - Vx - Vtn)^2 + \frac{Kn}{2}(Vx - Vc - Vtn)^2 \quad (3)$$

where $Id1$ and $Id2$ are the drain currents of transistors M1 and M2, respectively, $Kn = \mu_n Cox$ is the process parameter and Vtn is the threshold voltage. According to eqn. 3, if $Vx = Vc/2$, then eqn. 3 can be rewritten as

$$Id1 + Id2 = Kn\left(\frac{-Vc}{2} - Vtn\right)^2\left(1 + \frac{Vin}{\left(\frac{-Vc}{2} - Vtn\right)} + \frac{Vin^2}{2\left(\frac{-Vc}{2} - Vtn\right)^2}\right) \quad (4)$$