

ON THE DVCC AND THE BOCCII AS ADJOINT ELEMENTS

AHMED M. SOLIMAN

*Electronics and Communications Engineering Department,
Faculty of Engineering Cairo University, Egypt
asoliman@ieee.org*

Revised 12 March 2009

The Differential Voltage Current Conveyor (DVCC) with its two polarities namely DVCC⁻ and DVCC⁺ are reviewed together with their pathological element representations. Their two adjoint building blocks are the Balanced Output Current Conveyor (BOCCII) and the Balanced Output Inverting Current Conveyor (BOICCCII) are also discussed with their pathological element representations. The universal CMOS circuit realizing these four building blocks is also included.

The Nodal Admittance Matrix (NAM) stamp for the DVCC⁻, DVCC⁺, BOCCII and BOICCCII are also given. Among the four basic building blocks considered the DVCC⁻ is the only floating building block.

Examples are given showing that some of the reported filters are related to each other by the adjoint network theorem.

Keywords: Differential voltage current conveyor; balanced output current conveyor; inverting current conveyor.

1. Introduction

The reciprocity theorem introduced in Ref. 1 defines a circuit as reciprocal if the same transfer function is obtained when the input and output are interchanged. The scope of the reciprocity theorem was extended in Ref. 2 by defining the concept of inter-reciprocity. An inter-reciprocal circuit is known as the adjoint of the original circuit. The properties of the adjoint circuit can therefore be inferred from the properties of the original circuit without requiring any further analysis.^{3,4}

Recently it was shown that all the properties are preserved to the adjoint circuit except one important property, namely the floating status.⁵

In this paper the Differential Voltage Current Conveyor (DVCC) with its two polarities, namely DVCC⁻ and DVCC⁺, are reviewed together with their pathological element representations. Their two adjoint building blocks are the Balanced Output Current Conveyor (BOCCII) and the Balanced Output Inverting Current Conveyor (BOICCCII) are also reviewed with their pathological element representations. The universal CMOS circuit realizing all of these four building blocks is included.

The Nodal Admittance Matrix (NAM) stamp for the DVCC-, DVCC+, BOCCII and BOICCCII are also given. Among the four basic building blocks considered, the DVCC- is the only floating building block.

Examples are given showing that some of the reported filters are related to each other by the adjoint network theorem.

2. The DVCC- and the BOCCII as Adjoint Elements

The Differential Voltage Current Conveyor with a Z- output terminal (DVCC-) is shown symbolically in Fig. 1(a) and is defined by:⁶

$$\begin{bmatrix} V_X \\ I_{Y_1} \\ I_{Y_2} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y_1} \\ V_{Y_2} \\ V_{Z-} \end{bmatrix}. \tag{1}$$

With terminal Y₂ grounded, the DVCC- reduces to the CCII- as a special case.⁷ Also with terminal Y₁ grounded, the DVCC- reduces to the ICCII- as a special case.⁸

The pathological element representation of the DVCC- is shown in Fig. 1(b) which includes two voltage mirrors (VM)⁹ and two norators.

A dummy grounded norator is added at the reference terminal of the VMs, to form a pair with one of the VMs; meanwhile, the other VM forms a pair with the norator connected between terminals X and Z-.

The Nodal Admittance Matrix (NAM)¹⁰⁻¹³ representation of the DVCC- can be obtained as:

$$\begin{matrix} & X & Y_1 & Y_2 \\ X & \left[\begin{matrix} \infty_i & -\infty_i & \infty_i \\ -\infty_i & \infty_i & -\infty_i \end{matrix} \right] & & \\ Z- & & & \end{matrix}. \tag{2}$$

From the DVCC- definition Eq. (1) or the NAM Eq. (2) it is seen that the DVCC- is a floating building block. It is the only building block among the four basic blocks considered in this paper which has this floating property.⁵

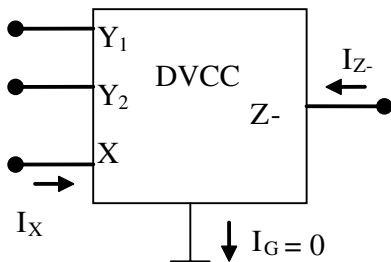


Fig. 1(a). Symbol of the floating four-port DVCC-.

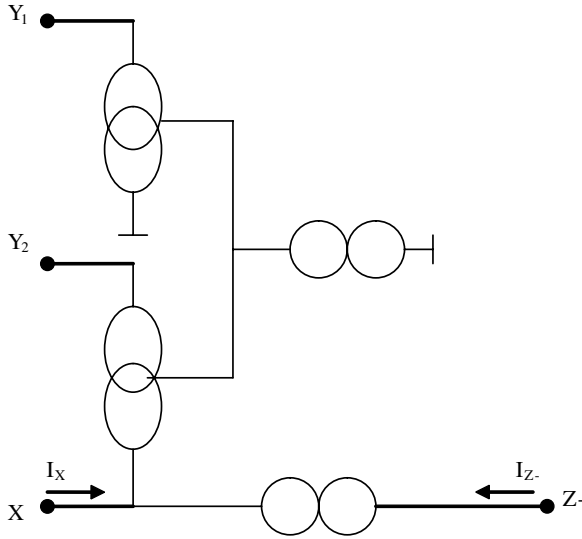


Fig. 1(b). Pathological element representation of the DVCC-.

With Y_2 grounded the NAM stamp of the CCII- is obtained as a special case and is given by:

$$\begin{matrix} & X & Y \\ X & \left[\begin{array}{cc} \infty_i & -\infty_i \\ -\infty_i & \infty_i \end{array} \right] \\ Z- & & \end{matrix} \quad (3)$$

Also with Y_1 grounded the NAM stamp of the ICCII- is obtained as a special case and is given by:

$$\begin{matrix} & X & Y \\ X & \left[\begin{array}{cc} \infty_i & \infty_i \\ -\infty_i & -\infty_i \end{array} \right] \\ Z- & & \end{matrix} \quad (4)$$

It is seen that both of the CCII- and ICCII- are floating building blocks.

The Balanced Output Current Conveyor (BOCCII) is shown symbolically in Fig. 2(a) and is defined by:¹⁴

$$\begin{bmatrix} V_X \\ I_Y \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (5)$$

The pathological element representation of the BOCCII is shown in Fig. 2(b)¹³ which includes two pathological current mirrors (CM)⁹ and two nullators. The grounded nullator connected at the common terminal of the two CMs is a dummy nullator to equate the number of nullators and CMs.¹³

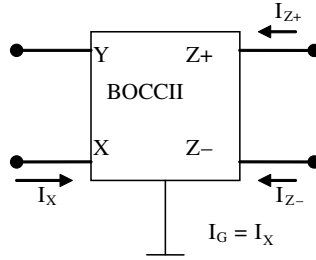


Fig. 2(a). Symbol of the balanced output CCII.

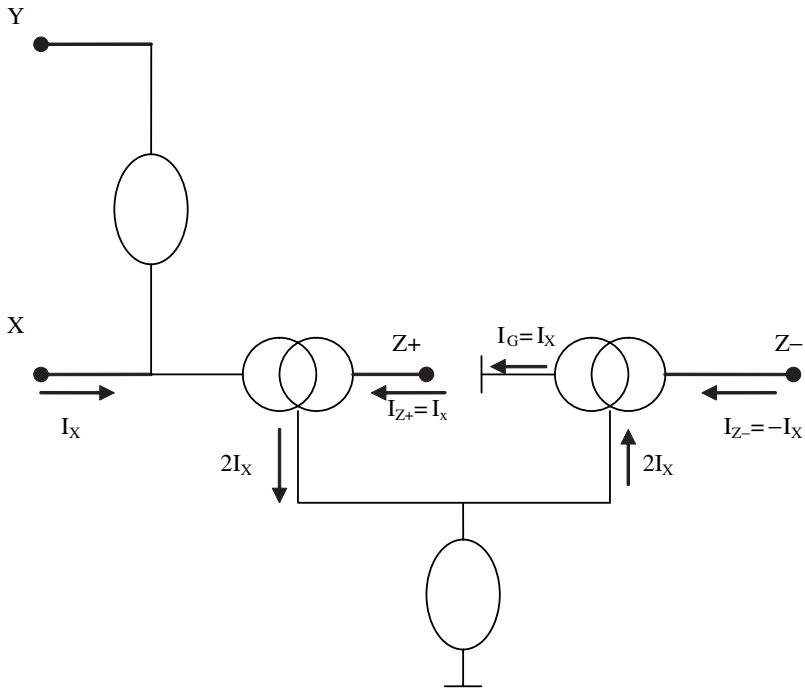


Fig. 2(b). Pathological element representation of the BOCCII.

The Nodal Admittance Matrix (NAM) representation of the BOCCII is obtained as:

$$\begin{matrix} & X & Y \\ X & \left[\begin{array}{cc} \infty_i & -\infty_i \\ -\infty_i & \infty_i \end{array} \right] \\ Z- & & \\ Z+ & & \end{matrix} \quad (6)$$

The above NAM representation is the transpose of the NAM of the DVCC— given by Eq. (2) since they are adjoint to each other. The BOCCII however is a non-floating building block and the ground current equals to I_X .

It is also seen that the NAM stamp of the CCII- is obtainable from the above equation with $Z+$ set to zero thus eliminating third row.

3. The DVCC+ and the BOICCCII as Adjoint Elements

The Differential Voltage Current Conveyor with a $Z+$ output terminal (DVCC+) is shown symbolically in Fig. 3(a) and is defined by:^{6,15}

$$\begin{bmatrix} V_X \\ I_{Y_1} \\ I_{Y_2} \\ I_{Z+} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y_1} \\ V_{Y_2} \\ V_{Z+} \end{bmatrix}. \tag{7}$$

With terminal Y_2 grounded, the DVCC+ reduces to the CCII+ as a special case.⁷ Also with terminal Y_1 grounded, the DVCC+ reduces to the ICCII+ as a special case.⁸

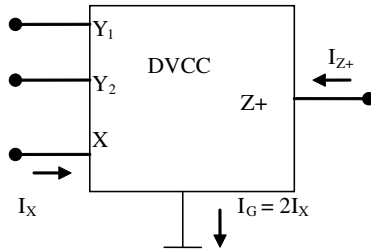


Fig. 3(a). Symbol of the four-port DVCC+.

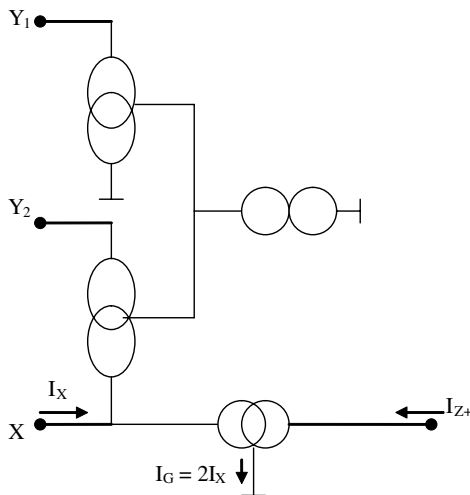


Fig. 3(b). Pathological element representation of the DVCC+.

The pathological element representation of the DVCC+ is shown in Fig. 3(b) which includes two VMs, a CM and a dummy norator to form a pair with one of the VMs while the other VM forms a pair with the CM connected between the X and Z+.

The Nodal Admittance Matrix (NAM)¹⁰⁻¹³ representation of the DVCC+ can be obtained as:

$$\begin{matrix} & X & Y_1 & Y_2 \\ X & \left[\begin{matrix} \infty_i & -\infty_i & \infty_i \end{matrix} \right] \\ Z+ & \left[\begin{matrix} \infty_i & -\infty_i & \infty_i \end{matrix} \right] \end{matrix} \cdot \tag{8}$$

From the DVCC+ definition Eq. (7) or the NAM Eq. (8) it is seen that the DVCC+ is a non-floating building block and the ground current equals to $2I_X$.

With Y_2 grounded the NAM stamp of the CCII+ is obtained as a special case and is given by:

$$\begin{matrix} & X & Y \\ X & \left[\begin{matrix} \infty_i & -\infty_i \end{matrix} \right] \\ Z+ & \left[\begin{matrix} \infty_i & -\infty_i \end{matrix} \right] \end{matrix} \cdot \tag{9}$$

Also with Y_1 grounded the NAM stamp of the ICCII+ is obtained as a special case and is given by:

$$\begin{matrix} & X & Y \\ X & \left[\begin{matrix} \infty_i & \infty_i \end{matrix} \right] \\ Z+ & \left[\begin{matrix} \infty_i & \infty_i \end{matrix} \right] \end{matrix} \cdot \tag{10}$$

It is seen that both of the CCII+ and ICCII+ are also non-floating building blocks and in both cases the ground current equals to $2I_X$.

The Balanced Output Inverting Current Conveyor (BOICCCII) is shown symbolically in Fig. 4(a) and is defined by:¹⁶

$$\begin{bmatrix} V_X \\ I_Y \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \tag{11}$$

The pathological element representation of the BOICCCII is shown in Fig. 4(b) which includes a VM, two CMs and a dummy grounded nullator connected at the common terminal of the two CMs.

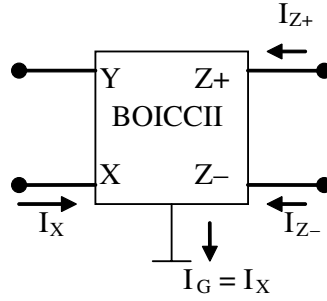


Fig. 4(a). Symbol of the balanced output ICCII.

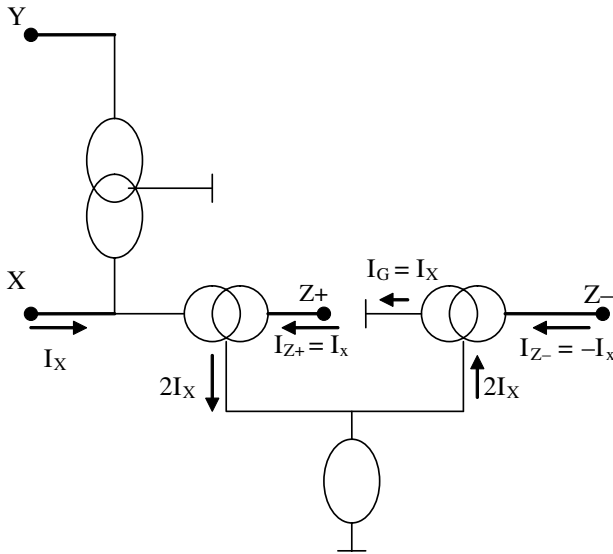


Fig. 4(b). Pathological element representation of the BOICCCII.

The Nodal Admittance Matrix (NAM) representation of the BOICCCII is obtained as:

$$\begin{matrix} & X & Y \\ \begin{matrix} X \\ Z- \\ Z+ \end{matrix} & \begin{bmatrix} \infty_i & \infty_i \\ -\infty_i & -\infty_i \\ \infty_i & \infty_i \end{bmatrix} & \end{matrix} \quad (12)$$

The above NAM representation is the transpose of the NAM of the DVCC+ given by Eq. (8) since they are adjoint to each other. The BOICCCII is a non-floating building block and the ground current equals to I_X .

It is seen that the NAM stamp of the ICCII- is obtainable from the above equation with $Z+$ set to zero thus eliminating third row resulting in Eq. (4). It is

also seen that the NAM stamp of the ICCII+ is obtainable from the above equation with $Z-$ set to zero thus eliminating second row resulting in Eq. (10).

4. The Universal CMOS Building Block

Figure 5 represents the CMOS universal building block^{6,15} with the aspect ratios shown in Table 1 based on the $0.5\ \mu\text{m}$ CMOS model from MOSIS. $V_{DD} = 1.5\ \text{V}$, $V_{SS} = -1.5\ \text{V}$ and $V_{B1} = -0.52\ \text{V}$ and $V_{B2} = 0.32\ \text{V}$.

The circuit realizes the DVCC- by connecting $Z+$ to ground, and the circuit realizes the DVCC+ by connecting $Z-$ to ground.

The BOCCII is realizable by setting Y_2 to ground and the BOICCCII is realizable by setting Y_1 to ground.

Simulations are carried out for the four building blocks as special cases from the universal CMOS circuit.

Figure 6(a) represents the magnitude and phase characteristics of the currents in R_X and in R_{Z-} of the DVCC- with $V_{Y1} = 2\ \text{V}$ and $V_{Y2} = 1\ \text{V}$. Terminals X and $Z-$ are connected to resistors of $1\ \text{k}\Omega$.

Figure 6(b) represents the magnitude and phase characteristics of the currents in R_X and in R_{Z+} of the DVCC+ with $V_{Y1} = 2\ \text{V}$ and $V_{Y2} = 1\ \text{V}$. Terminals X and $Z+$ are connected to resistors of $1\ \text{k}\Omega$.

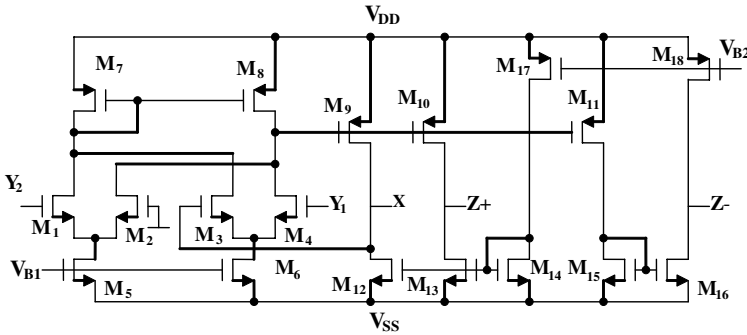


Fig. 5. Universal CMOS circuit realizing DVCC, BOCCII and BOICCCII.

Table 1. Transistor aspect ratios of the universal CMOS circuit shown in Fig. 5.

	$W(\mu\text{m})/L(\mu\text{m})$
NMOS transistors	
M_1, M_2, M_3, M_4	2.5/1
M_5, M_6	8/1
$M_{12}, M_{13}, M_{14}, M_{15}, M_{16}$	20/2.5
PMOS transistors	
M_7, M_8	10/1
$M_9, M_{10}, M_{11}, M_{17}, M_{18}$	40/2

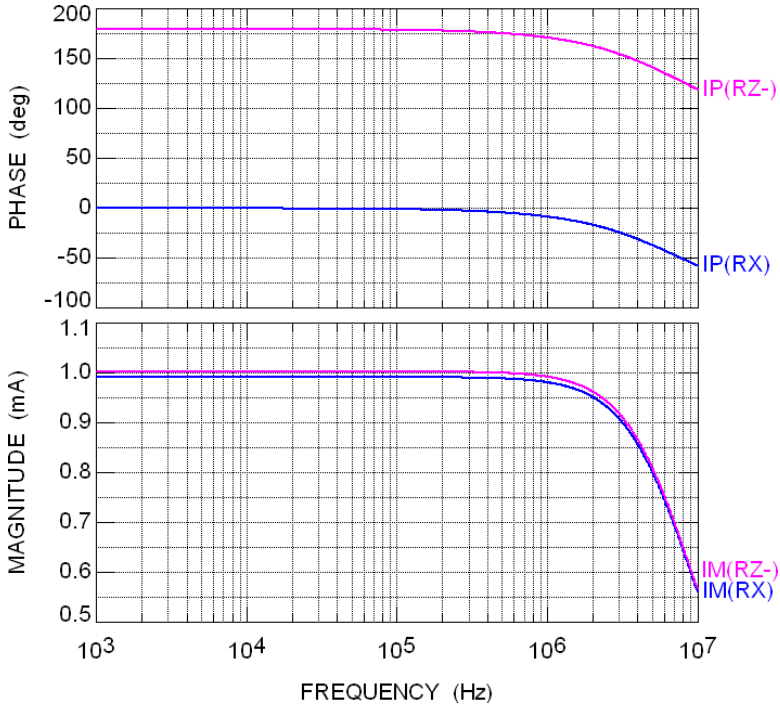


Fig. 6(a). Magnitude and phases responses of the DVCC.

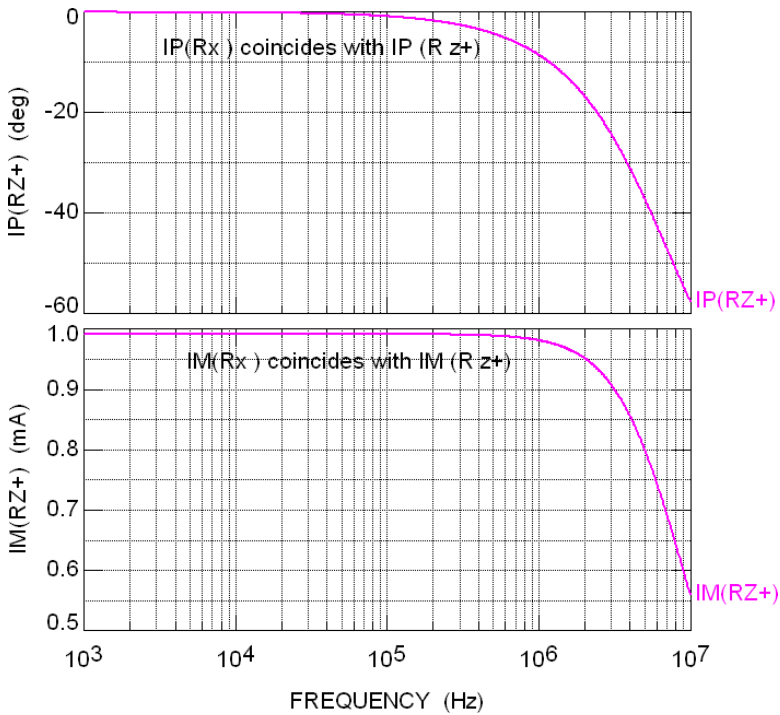


Fig. 6(b). Magnitude and phases responses of the DVCC+.

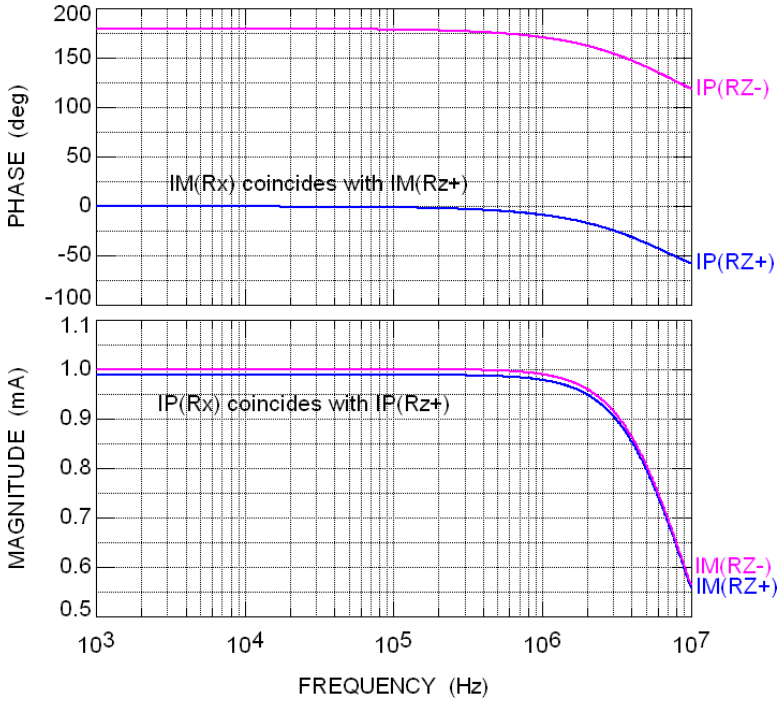


Fig. 6(c). Magnitude and phases responses of the BOCCII.

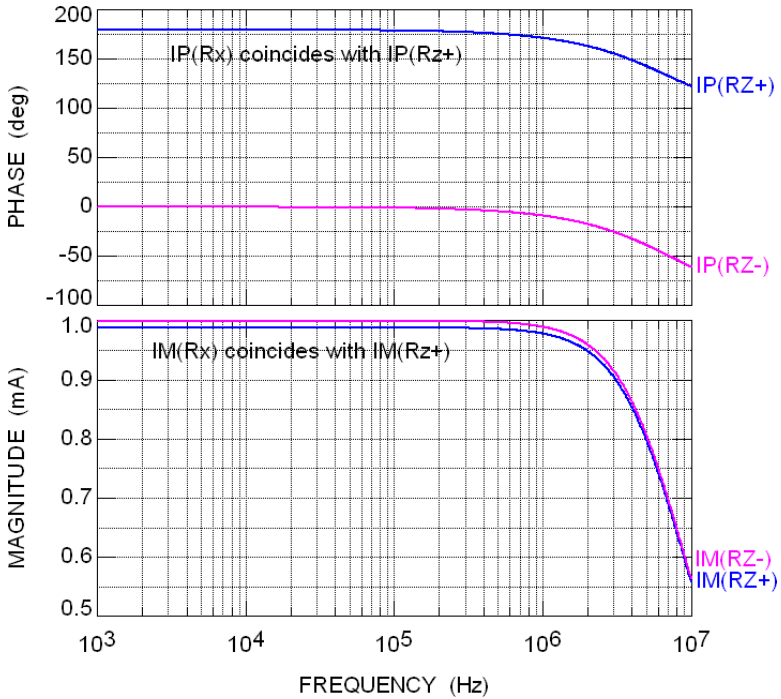


Fig. 6(d). Magnitude and phases responses of the BOICCCII.

Figure 6(c) represents the magnitude and phase characteristics of the currents in R_X , in R_{Z+} and in R_{Z-} of the BOCCII with $V_Y = 1\text{ V}$. Terminals X , $Z+$ and $Z-$ are connected to resistors of $1\text{ k}\Omega$.

Figure 6(d) represents the magnitude and phase characteristics of the currents in R_X , in R_{Z+} and in R_{Z-} of the BOICCCII with $V_Y = 1\text{ V}$. Terminals X , $Z+$ and $Z-$ are connected to resistors of $1\text{ k}\Omega$.

In all the above simulations the resistor connected to port X is taken slightly less than $1\text{ k}\Omega$ in order to account for the parasitic resistance R_X .

5. Examples

In this section the importance of the adjoint network theorem in generating new circuits as well as in discovering that some circuits that have been reported as new are related to well known circuits by the adjoint transformation.

5.1. Example 1

The first example taken is based on the current mode filter introduced in Ref. 17 which uses three BOCCII one of them acts as a current follower to provide the desirable low input impedance. The band-pass low-pass current mode filter given in Fig. 4(a) realization 3 in Table 2 of Ref. 18 and shown in Fig. 7(a) is based on the current mode filter in Ref. 17 after removing the first stage. The circuit uses two BOCCII, three grounded resistors and two grounded capacitors.

$$\frac{I_{BP}}{I_i} = \frac{-sC_2R_2}{s^2C_1C_2R_1R_2 + \frac{sC_2R_1R_2}{R} + 1}, \tag{13}$$

$$\frac{I_{LP}}{I_i} = \frac{1}{s^2C_1C_2R_1R_2 + \frac{sC_2R_1R_2}{R} + 1}. \tag{14}$$

The radian frequency ω_0 and Q are given by:

$$\omega_0 = \frac{1}{\sqrt{C_1C_2R_1R_2}}, \quad Q = R\sqrt{\frac{C_1}{C_2R_1R_2}}. \tag{15}$$

The resistor R controls Q without affecting ω_0 .

This circuit has one input current and two output currents, and when the adjoint transformation is applied in the classical way a two inputs one output voltage mode circuit is obtained. In the following the adjoint transformation is applied to the circuit of Fig. 7(a) in the non-classical way considering that it has only one band-pass output.

Replacing the two BOCCII by their adjoint blocks namely two DVCC-, the voltage mode circuit of Fig. 7(b) is obtained. The band-pass voltage transfer function is given by:

$$\frac{V_{BP}}{V_i} = \frac{-sC_2R_2}{s^2C_1C_2R_1R_2 + \frac{sC_2R_1R_2}{R} + 1}. \tag{16}$$

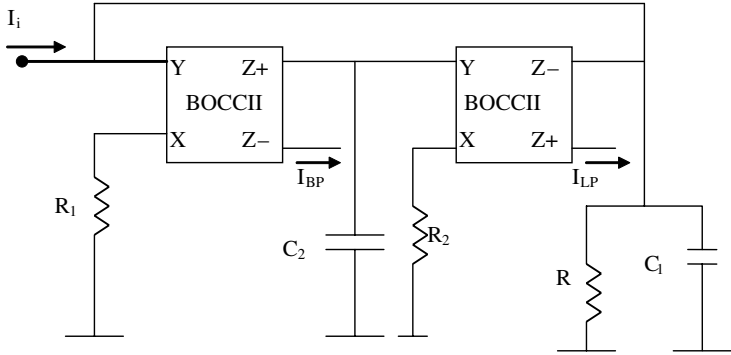


Fig. 7(a). Grounded R, C current mode circuit using BOCCII.¹⁸

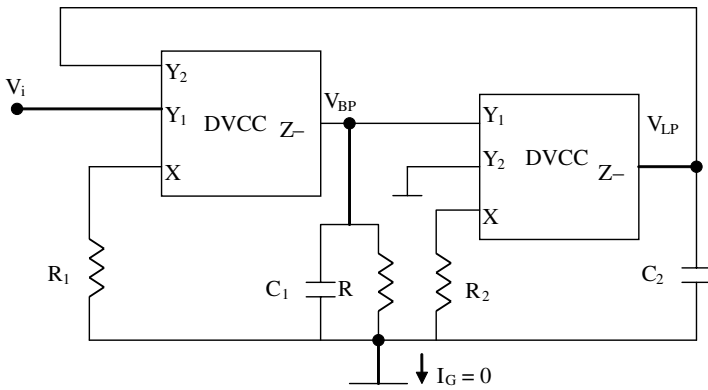


Fig. 7(b). Voltage mode Tow-Thomas circuit using DVCCII-.

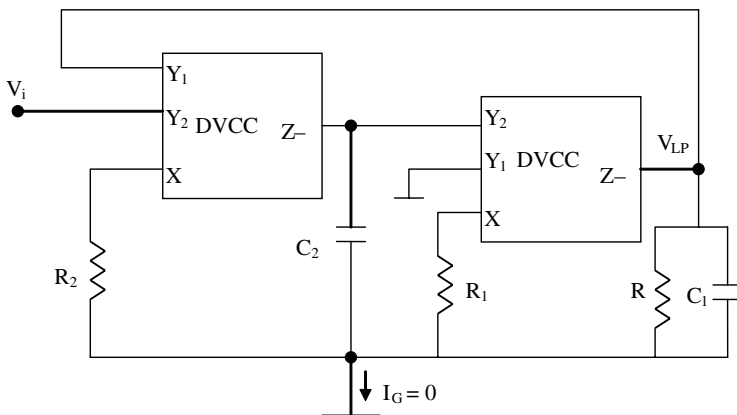


Fig. 7(c). Voltage mode low-pass filter derived as adjoint of Fig. 7(a).

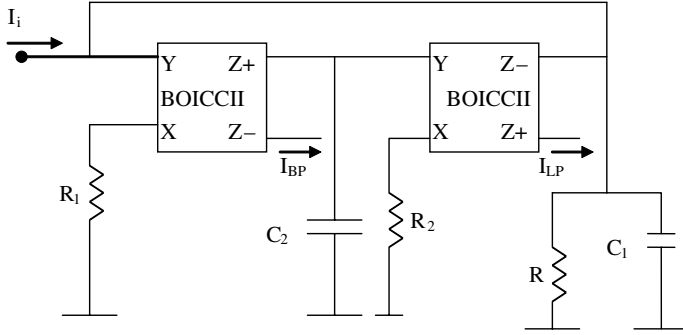


Fig. 8(a). Grounded R, C current mode circuit using BOICCH.¹⁶

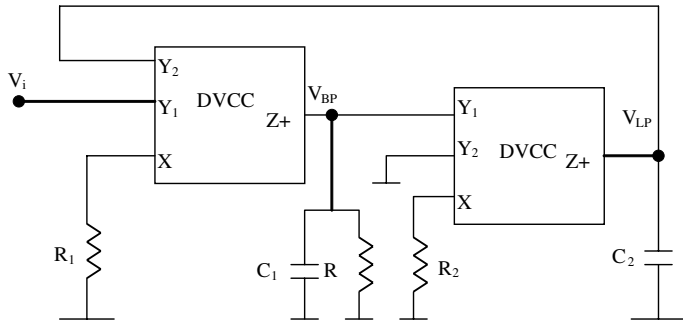


Fig. 8(b). Voltage mode Tow-Thomas circuit using DVCCII+.¹⁵

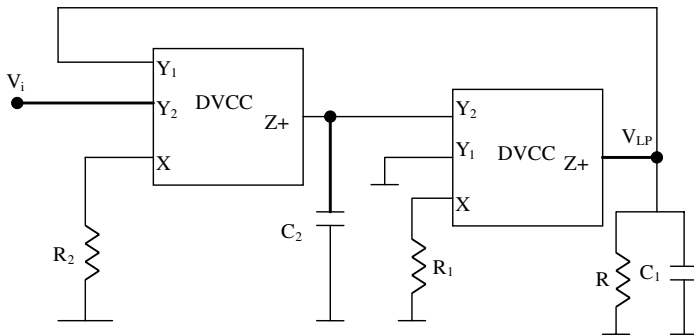


Fig. 8(c). Voltage mode low-pass filter derived as adjoint of Fig. 8(a).

Since the second stage realizes an inverting integrator, the voltage at the $Z-$ of the second stage is a noninverting low-pass response with a transfer function:

$$\frac{V_{LP}}{V_i} = \frac{1}{s^2 C_1 C_2 R_1 R_2 + \frac{s C_2 R_1 R_2}{R} + 1}. \quad (17)$$

Equation (15) applies to this Tow-Thomas voltage mode circuit.^{19,20} It is interesting to notice that although the original circuit of Fig. 7(a) has a nonzero grounded current I_G , the transformed circuit of Fig. 7(b) has $I_G = 0$.

Next the adjoint transformation is applied to the circuit of Fig. 7(a) in the non-classical way considering that it has only one low-pass output. Replacing the two BOCCII by their adjoint blocks, namely two DVCC–, the voltage mode circuit of Fig. 7(c) is obtained. The low-pass voltage transfer function is the same as given by Eq. (17). This transformed low-pass circuit of Fig. 7(c) has also a floating nature since $I_G = 0$.

5.2. Example 2

The second example is based on the current mode filter using two BOICCCII and introduced in Ref. 16. The circuit equations are the same as given by Eqs. (13) to (15) except the band-pass response is noninverting.

In the following the adjoint transformation is applied to the circuit of Fig. 8(a) in the non-classical way by considering that it has only one band-pass output. Replacing the two BOICCCII by their adjoint blocks, namely two DVCC+, the voltage mode circuit of Fig. 8(b) is obtained. Since the second stage realizes a noninverting integrator, the voltage at the $Z+$ of the second stage is a noninverting low-pass response. This circuit was introduced in Ref. 15 and it represents the well known Tow-Thomas circuit Refs. 19, 20 using the DVCC+ as basic building blocks.

Next the adjoint transformation is applied to the circuit of Fig. 8(a) in the non-classical way considering that it has only one low-pass output. Replacing the two BOICCCII by their adjoint blocks, namely two DVCC+, the voltage mode circuit of Fig. 8(c) is obtained. The low-pass voltage transfer function is the same as given by Eq. (17). This transformed low-pass circuit of Fig. 8(c) has also a non-floating nature since I_G is not zero.

6. Conclusions

A review of the Differential Voltage Current Conveyor (DVCC) with its two polarities namely DVCC– and DVCC+ are given together with their pathological element representations. Their two adjoint building blocks are the Balanced Output Current Conveyor (BOCCII), and the Balanced Output Inverting Current Conveyor (BOICCCII), they are also discussed with their pathological element representations. The universal CMOS circuit realizing these four building blocks is also included.

The Nodal Admittance Matrix (NAM) stamp for the DVCC–, DVCC+, BOCCII and BOICCCII are also given. Among the four basic building blocks considered, the DVCC– is the only floating building block.

Examples are given showing that some of the reported filters are related to each other by the adjoint network theorem. The six filters considered in this paper have the advantage that the parasitic elements, namely R_X and C_Z , can be easily compensated by subtracting their values from the proper resistance connected to

port X and the proper capacitance connected to port Z . Among the six filter circuits given in this paper in Figs. 7 and 8, only the circuits of Figs. 7(b) and 7(c) have a floating property.

It is worth noting that very recently, alternative modeling of the BOCCII has been described in Refs. 21 and 22. The BOCCII is modeled using one nullator, one norator and two current controlled current sources (CCCS).²¹ Its adjoint circuit, namely the DVCC–, is also represented in Ref. 21 using one nullator, one norator and two voltage controlled voltage sources (VCVS) and generalized to multiple inputs and defined as multiple input differential current conveyor (MIDCC). The representation given in Ref. 21 is for MIDCC– and no realization was given for MIDCC+ which implies that no representation for the DVCC+ was given in Ref. 21. The BOCCII is modeled using four nullators, four norators and five grounded resistors.²² Although the well known representation of the ICCII–⁸ using two nullators, two norators and two grounded resistors is described in Ref. 22, no nullator norator representations for the BOICCCII is given in Ref. 21 or in Ref. 22.

References

1. B. D. H. Tellegen, A general network theorem with applications, *Philips Res. Rep.* **7** (1952) 259–269.
2. L. J. Bordewijk, Inter-reciprocity applied to electrical networks, *Appl. Sci. Res.* **B-6** (1956) 1–74.
3. S. W. Director and R. A. Rohrer, The generalized adjoint network and network sensitivities, *IEEE Trans. Circuit Theor.* **16** (1969) 318–323.
4. B. B. Bhattacharyya and M. N. S. Swamy, Network transposition and its application in synthesis, *IEEE Trans. Circuit Theor.* **18** (1971) 394–397.
5. A. M. Soliman, Adjoint network theorem and floating elements in the NAM, *J. Circuits Syst. Comput.* **18** (2009) 597–616.
6. H. O. Elwan and A. M. Soliman, Novel CMOS differential voltage current conveyor and its applications, *IEE Proc. Circuits Dev. Syst.* **144** (1997) 195–200.
7. A. S. Sedra and K. C. Smith, A second generation current conveyor and its applications, *IEEE Trans. Circuit Theor.* **17** (1970) 132–134.
8. I. A. Awad and A. M. Soliman, Inverting second generation current conveyors: The missing building blocks, CMOS realizations and applications, *Int. J. Electron.* **86** (1999) 413–432.
9. I. A. Awad and A. M. Soliman, On the voltage mirrors and the current mirrors, *Anal. Integr. Circuits Signal Process.* **32** (2002) 79–81.
10. D. G. Haigh, T. J. W. Clarke and P. M. Radmore, Symbolic framework for linear active circuits based on port equivalence using limit variables, *IEEE Trans. Circuits Syst. I* **53** (2006) 2011–2024.
11. D. G. Haigh and P. M. Radmore, Admittance matrix models for the nullor using limit variables and their application to circuit design, *IEEE Trans. Circuits Syst. I* **53** (2006) 2214–2223.
12. R. A. Saad and A. M. Soliman, Use of mirror elements in the active device synthesis by admittance matrix expansion, *IEEE Trans. Circuits Syst. I* **55** (2008) 2726–2735.
13. R. A. Saad and A. M. Soliman, A new approach for using the pathological mirror elements in the ideal representation of active devices, *Int. J. Circuit Theor. Appl.*, Online DOI: 10.1002/cta.534, 2008.

14. H. O. Elwan and A. M. Soliman, A novel CMOS current conveyor realization with an electronically tunable current mode filter suitable for VLSI, *IEEE Trans. Circuits Syst. II* **43** (1996) 663–670.
15. W. Chiu, S. I. Liu, H. W. Tsao and J. J. Chen, CMOS differential difference current conveyors and their applications, *IEE Proc. Circuits Dev. Syst.* **143** (1996) 91–96.
16. A. M. Soliman, New grounded capacitor current mode band-pass low-pass filters using two balanced output ICCII, *J. Active Passive Electron. Dev.* **3** (2008) 175–184.
17. A. M. Soliman, Current mode universal filter, *Electron. Lett.* **31** (1995) 1420–1421.
18. A. M. Soliman, New current mode filters using current conveyors, *Int. J. Electron. Commun. (AEU)* **51** (1997) 275–278.
19. J. Tow, A step by step active filter design, *IEEE Spec.* **6** (1969) 64–68.
20. L. Thomas, The Biquad: Part I — Some practical design considerations, *IEEE Trans. Circuit Theor.* **CT-18** (1971) 350–357.
21. J. W. Horng, C. L. Hou and C. M. Chang, Multi-input differential current conveyor, CMOS realization and application, *IET Circuits Dev. Syst.* **2** (2008) 469–475.
22. E. Tlelo-Cuautle, C. Sanchez-Lopez and D. Moro-Frías, Symbolic analysis of (MO)(I)CCI(II)(III)-based analog circuits, *Int. J. Circuit Theor. Appl.* Online DOI: 10.1002/cta.582, 2009.