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CMOS voltage controlled floating resistor

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A new CMOS floating linear resistor circuit with a wide linearity range is proposed. The circuit employs 14 transistors all operating in the saturation region. A modified circuit which employs one more transistor, such that it is threshold voltage independent, is also given. PSPICE simulations taking into account the second order effects due to the channel length modulation and mobility degradation are given.

1. Introduction

MOS technology is inherently capable of realizing excellent quality capacitors and op.-amps; however, resistors of practical values in MOS technology suffer from nonlinearities and high temperature coefficients. Extensive research has been proposed for replacing the resistors in analogue circuit applications by MOS transistors, such that the circuit is fully integrated (Ismail 1985, Sakurai *et al.* 1992, Kobayashi *et al.* 1991, Van der Plas 1991, Kwan and Martin 1991). Banu and Tsividis (1982) proposed a CMOS floating resistor based on transistors operating in the triode region that employ ten transistors. The low MOS transconductance and the distributed channel capacitance in the triode region may limit the frequency response. Recently, Singh *et al.* (1989) proposed a floating resistor for CMOS technology using 36 transistors operating in the saturation region, and Sakurai and Ismail (1992) proposed an elegant CMOS square-law floating resistor using 20 transistors. The objective of this paper is to propose a new voltage-controlled CMOS floating resistor using only 15 transistors.

2. The MOS resistor circuit

The MOS floating resistor circuit is shown in Fig. 1. The nodes X and Y are the two terminals of the resistor. The matched transistors M1 and M2 are the basic transistors forming the two ports of the resistor. Transistors M3, M4, M5 and M6 form the biasing circuit for M1 and M2. The remaining transistors perform the current transfer to the two ports of the resistor. All the transistors are assumed to be operating in the saturation region with their sources connected to the substrate/bulk. The MOS drain current in the saturation region is given by

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2 \tag{1}$$

where

$$K = \mu C_{ox}(W/L) \tag{2}$$

W/L = the transistor aspect ratio

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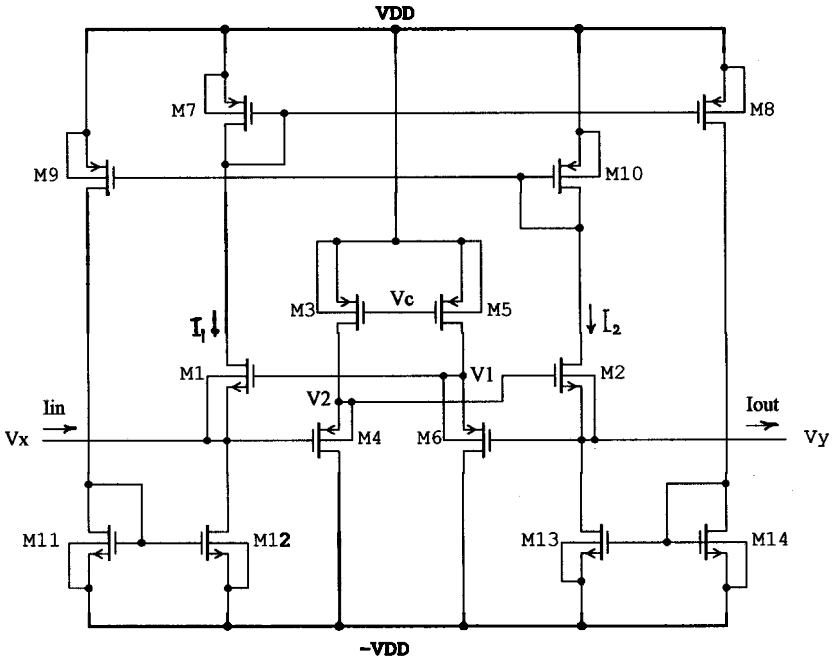


Figure 1. CMOS floating resistor circuit.

C_{ox} = the gate-oxide capacitance per unit area
μ = the electron mobility
V_T = the threshold voltage (assumed equal for all MOS transistors)

From Fig. 1

$$I_{in} = I_{out} = I_2 - I_1 \tag{3}$$

$$I_1 = \frac{K}{2}(V_1 - V_x - V_T)^2 \tag{4}$$

$$I_2 = \frac{K}{2}(V_2 - V_y - V_T)^2 \tag{5}$$

Therefore

$$I_{in} = I_{out} = \frac{K}{2}(V_1 + V_2 - V_x - V_y - 2V_T)(V_2 - V_1 + V_x - V_y) \tag{6}$$

From the biasing circuit realized by the two matched transistors M3 and M4, one obtains

$$I_3 = I_4 \tag{7}$$

Therefore

$$\frac{K}{2}(V_C - V_{DD} - V_{Tp})^2 = \frac{K}{2}(V_x - V_2 - V_{Tp})^2 \tag{8}$$

Hence

$$V_2 = V_x - V_C + V_{DD} \tag{9}$$

Similarly, from the biasing circuit realized by the matched transistors M5, M6 one obtains

$$V_1 = V_y - V_C + V_{DD} \tag{10}$$

From (9), (10) and (6) one gets

$$I_{in} = I_{out} = 2K(V_{DD} - V_C - V_T)(V_x - V_y) \tag{11}$$

Therefore, the MOS circuit simulates a floating resistor between the nodes X and Y and its value is controlled by V_C and is given by

$$R = \frac{V_x - V_y}{I_{in}} = \frac{V_x - V_y}{I_{out}} = \frac{1}{2K(V_{DD} - V_C - V_T)} \tag{12}$$

It should be noted that the resistor value depends on V_T, which is a process dependent parameter.

Figure 2 represents a modified MOS resistor circuit in which only one transistor M15 is added that shifts V_C (control voltage) by the amount V_T before it is applied to the biasing circuit, therefore the biasing voltages V_1 and V_2 are modified to

$$V_1 = V_y - V_C + V_T + V_{DD} \tag{12}$$

$$V_2 = V_x - V_C + V_T + V_{DD} \tag{13}$$

From (12) and (13) in (6), one gets

$$I_{in} = I_{out} = 2K(V_{DD} - V_C)(V_x - V_y) \tag{14}$$

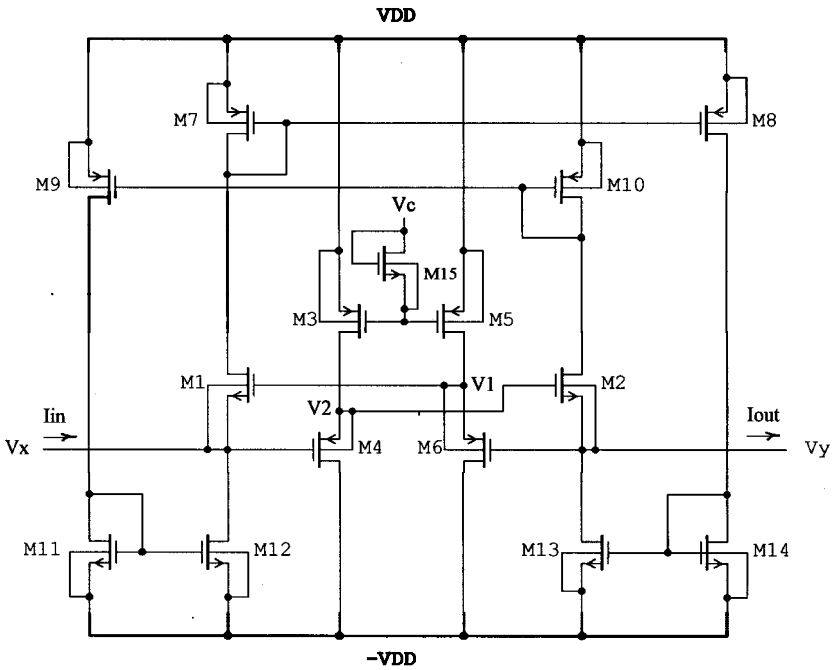


Figure 2. Modified CMOS floating resistor circuit.

Therefore

$$R = \frac{V_x - V_y}{I_{in}} = \frac{V_x - V_y}{I_{out}} = \frac{1}{2K(V_{DD} - V_C)} \tag{15}$$

It is seen that the magnitude of the resistor is controlled by V_C and is independent of V_T.

3. Simulation results

PSPICE simulations were carried out with the transistors' aspect ratios as given in Table 1 and with the supply voltages = ±3·3 V. The PSPICE model parameters for the NMOS and PMOS transistors are listed in Table 2.

Figure 3 (*b*) represents the magnitude response of the maximally flat magnitude Sallen and Key lowpass filter shown in Fig. 3 (*a*), where the values of the capacitors are C_1 = 1·414 nF and C_2 = 0·707 nF. The two floating resistors are implemented using the MOS resistor circuit shown in Fig. 2. The resistor magnitudes are controlled by the control voltage V_C, which is scanned from 2·17 V to 2·67 V. The THD is less than 0·28% for a 1 kHz 1 Volt peak-to-peak sinusoidal input. The power consumption of each of the MOS resistors is less than 0·5 mW.

MOS transistor	Aspect ratio (W/L)
M1, M2	24/10
M3, M4, M5, M6	4/4
M7, M8, M9, M10	60/18
M11, M12, M13, M14	60/18
M15	4/4

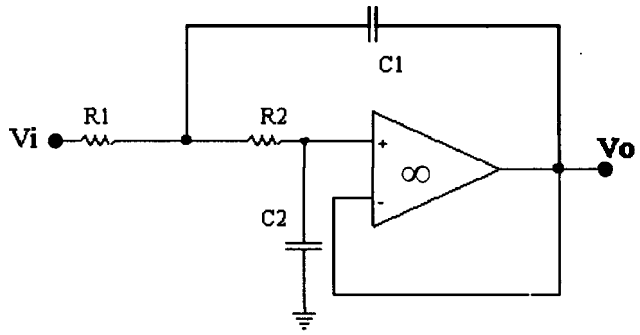
Table 1. Transistor aspect ratios.

Model parameters set for 2 μm CMOS Technology (obtained through MOSIS)

.MODEL NMOS NMOS LEVEL = 2 LD= 0·225112U TOX= 405·000001E-10
NSUB= 2·256421E+ 15 VTO= 0·77227 KP= 4·954000E-05 GAMMA= 1·0151 PHI= 0·6
UO= 581 UEXP= 0·217142 UCRIT= 115146 DELTA= 1·360440 VMAX= 68535·3
XJ= 0·250000U NFS= 2·85E+ 12 NEFF= 1 NSS= 1·000000E+ 10 TPG= 1·000000
RSH= 27·020000 CGDO= 2·873845E-10 CGSO= 2·880845E-10 CGBO= 3·840832E-10
CJ= 4·100000E-04 MJ= 0·4650 CJSW= 4·803300E-10 MJSW= 0·351 PB= 0·800000

MODEL PMOS PMOS LEVEL= 2 LD= 0·177432U TOX= 405·000001E-10
NSUB= 3·956006E+ 15 VTO= - 0·74078 KP= 2·526000E-05 GAMMA= 0·4251 PHI= 0·6
UO= 299·253 UEXP= 0·1933 UCRIT= 5462·67 DELTA = 0·91285 VMAX= 29720·9
XJ= 0·250000U NFS= 1·00E+ 11 NEFF= 1 NSS= 1·000000E+ 10 TPG= - 1·000000
RSH= 107·40000 CGDO= 2·262940E-10 CGSO= 2·268940E-10 CGBO= 3·471103E-10
CJ= 1·898000E-04 MJ= 0·439556 CJSW= 2·267600E-10 MJSW= 0·207266 PB= 0·700000

Table 2. PSPICE model parameters for the NMOS and PMOS transistors.



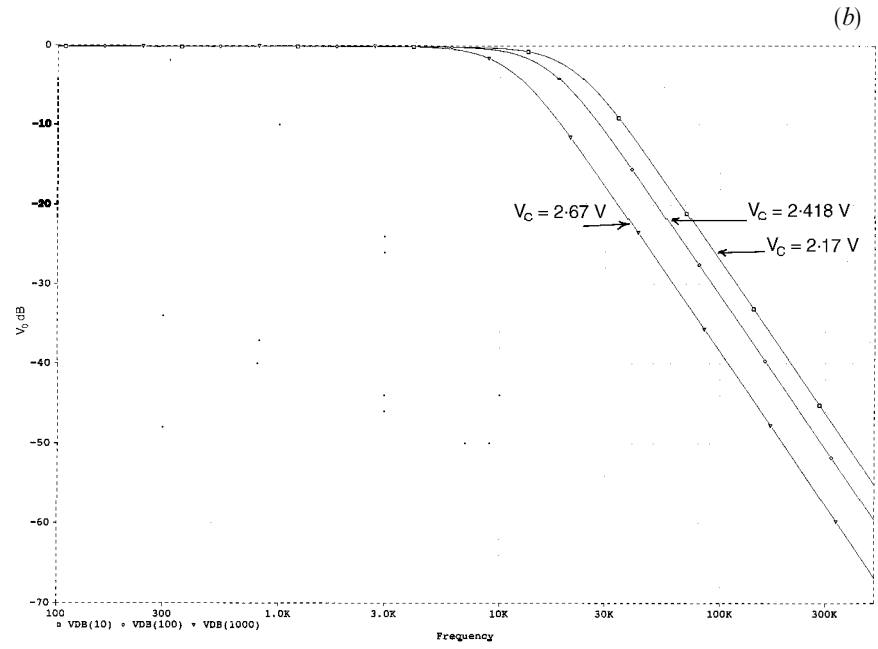


Figure 3. (*a*) The Sallen–Key lowpass filter. (*b*) The magnitude response of the Sallen–Key filter with V_C as a parameter.

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