3D-NOCET: A Tool for Implementing 3D-NoCs based on the Direct-Elevator Algorithm

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***Abstract*—In this paper, a new tool is proposed to provide a solution for the implementation of generic 3D Network-on-Chips (NoCs) to serve different applications. The proposed tool denoted by 3D-NOCET, is based on the 3D Direct-Elevator routing algorithm. The 3D-NOCET tool allows the user to create different combinations of 3D-NoCs based on the 2D-routing topology, number of tiers and number of routers per each tier through a fully automated process. That opens the door to perform future experimental evaluations for the different 3D-NoC structures.**

The future experimental evaluations and the performance comparative analyses help to find the optimal network configuration for different applications, specifically the 3D-NoC based Field Programmable Gate Arrays (FPGA).

***Index Terms*—3D technology, NoC, 3D NoC, 3D NoC tool.**

I. Introduction

Three-Dimensional technology which stacks multiple levels of devices, offers a dramatic enhancement in the system performance and functionality [1]. The 3D integration also combines the benefits from the System-on-Chip (SoC) which adds all system components into a single chip and the System-in-Package (SiP) which assimilates to intergarte non-silicon parts to the chip [2]. Also, it opens many opportunities to combine different components of microelectronics and micromechanicals in a single silicon die [3]. The demand for the 3D intergration technology increases due to the urgent need to reduce the length of interconnections and power consumption in the new advanced electronic products [4]. The 3D chips in the 3D technology are connected vertically with Through Silicon-Vias (TSV's) using four different stacking techniques: package stacking, die stacking, wafer stacking and device stacking [2] . Besides all the benefits of the 3D technology, it introduces new challenges in the power, the modeling of interconnects, the noise and the fabrication process [5]. In addition to the challenging considerations in the TSV's technology itself such as silicon cracking, high power density, heat generation and thremo-mechanical reliability [6] . On the other hand, Network-on-chip (NoC) offers flexiable, reliable and reconfigurable networks [7].

The advantages of the 3D new trend and NoCs are all combined in the 3D-NoCs providing a significant improvement and wide flexibility in the networking designs [8]. New 3D routing techniques have been developed and implemented to create and evaluate different combinations of 3D-NoCs. One of these techniques is the Elevator-First algorithm [9]. The Elevator First routing algorithm is a routing algorithm for partially vertically connected 3D-NoC which is deadlock and livelock free using two virtual channels. This algorithm is proved to be independent on the location and number of TSVs and the dimensions of the planar topologies. A 3D-NoC router is fully designed and impelmented to support the Elevator-First algorithm [10]. The Direct-Elevator algorithm can be considered as a special case from the Elevator-First algorithm that offers better communication latency [11]. The 3D-NOCET tool is based on the Direct-Elevator algorithm. It allows the user to create numerous synthesizble structures of the 3D-NoCs through a fully automated process by choosing the number of tiers, the number of routers per tier and the 2D routing topology.

This paper is organized as follows. In section II, various tools and simulators for 2D and 3D-NoCs are presented. In section III, An introduction to the 3D-NOCET tool is presented. In section IV, comparative performance study between different 3D-NoCs is detailed. Finally, Section V provides the conclusion of this work.

II. Related Work

Many tools and simulators have been created and developed to allow the researchers to find the best optimal NoC sturcture for different applications and also to perform experiments on different configurable NoCs. The authors of [12], developed a tool, CONNECT, which is a NoC generator to produce synthesizable 2D-NoCs with different dimensions, topology and number of virtual channels. In [13], a simulator developed in SystemC denoted by Noxim is presented. Noxim offers a configurable, flexible and open simulator to analyze the power and the performance of different NoCs. Authors in [14], proposed a modular SystemC based simulator denoted by NIRGAM, which allows the user to perform experiments with different NoC configurations and to analyze the performance according to the latency factor. In [15], the authors presented Booksim which is a cycle accurate simulator for NoCs, it offers a large number of configurable networks. These configurable networks vary in the topology, flow control, router architecture and routing algorithm aspects.

III. An Introduction to 3D-NOCET tool

The 3D-NOCET tool allows the user to create different configurable 3D-NoCs. An easy-to-use Graphical User Interface (GUI), allows the user to select the 2D routing topology, the number of tier in the 3D-NoC and the number of routers per tier. The tool then creates synthesizable SystemVerilog Register Transfer Logic (RTL) design files for the 3D-NoC through an automated infrastructure. Fig.1 shows the GUI of the tool, the user in this figure entered a 3D-NoC with the following configurations:

- Mesh topology for 2D routing topology.
- Four tiers in the 3D-NoC system.
- Four routers per each tier.

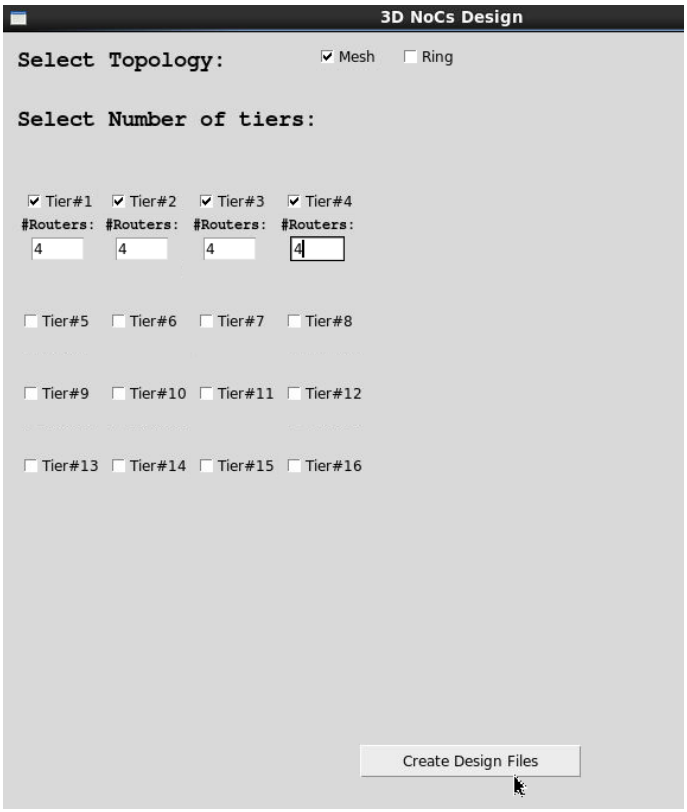

Fig. 1: The GUI of 3D-NOCET tool

The tool is implemented to support maximum number of tiers equals to 16, maximum number of routers per each tier equals to 255 and two 2D topologies, mesh and ring topologies. The tool mainly consists of the following components:

- Automation infrastructure to guarantee the flexilibty in creating different configurations of 3D-NoCs.
- The 3D router design that has been implemented to support mesh or ring as 2D topology and Direct-Elevator algorithm as the 3D routing mechanism.

All the Implemented 3D-NoCs have two vertical connections which act as the packet direct elevators to route the packets in the 3D dimension, also the 2D connections differ according to the 2D topology that gives two main categories of the implemented 3D-NoCs as shown in Fig.2 and Fig.3.

The tool has the flexibiity and reliability to create various structures of 3D-NoCs that paves the road to evaluate the performance for different structures and to find the optimal network configuration for many applications.

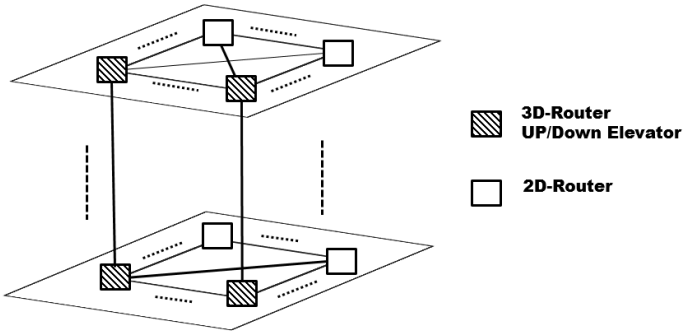

Fig. 2: The 3D-NoC in 2D Mesh Topology

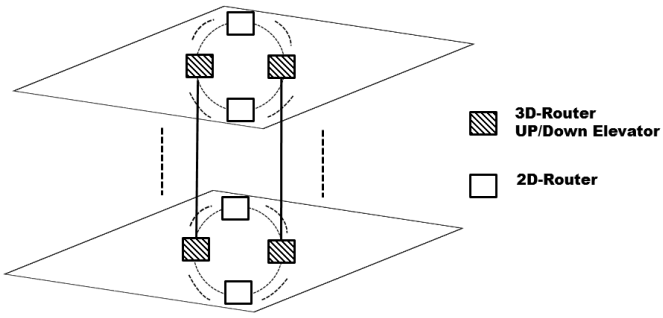

Fig. 3: The 3D-NoC in 2D Ring Topology

IV. Comparative and Performance Study on different Structures of 3D-NoCs

A study has been conducted in order to compare the performance of the different 3D-NoCs strucutres according to the area, power and latency aspects. All the 3D-NoCs are synthesized using Xilinx-Virtex7 technology and simulated using Questa simulation tool to guarantee an efficient and fair performance and comparison analysis. All designs are synthesized at a frequency of 100MHz. Also, the power is caluclated as the worst power can be consumed by the 3D-NoC and the latency is calculated according to the worst network path between two routers in clock cycles. The effect of the vertical network complexity, tier network complexity and 2D topology is measured on 3D-NoCs performance.

A. Vertical Network Complexity in 3D-NoCs

The vertical complexity measures the effect of increasing the number of tiers in the 3D-NoCs with mesh and ring planar topologies. The impact of the vertical complexity is measured through the latency, area and power factors.

Fig.4 shows the latency measured in clock cycles. The latency in the mesh topology increases linearly with the number of tiers, meanwhile it is the same if the number of routers per each tier doubled from four to eight as the routers in each tier

are connected in fully mesh topology. Also, the latency in the ring topology increases linearly with the number of tiers, but it increases while doubling the routers per each tier from four to eight as the routers are connected in a ring topology that lengthen the packet worst path in the network.

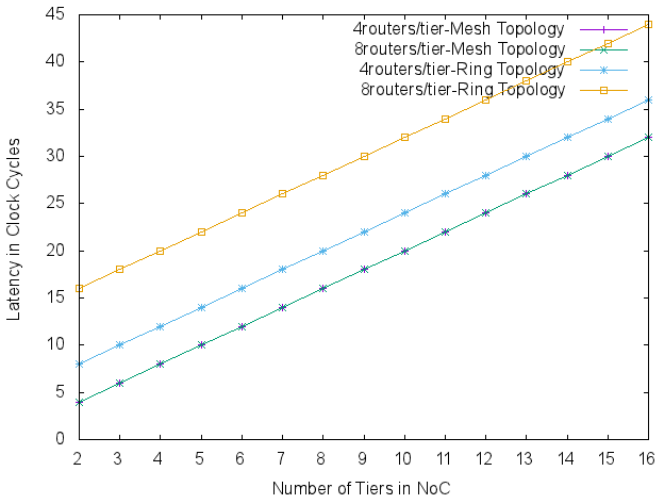

Fig. 4: Latency in Clock Cycles Vs. Number of Tiers in NoC

Fig.5 shows the power measured in Watts. The power in the mesh topology increases with the number of tiers in the 3D-NoC, also the power increases while doubling the number of routers in each tier from four to eight as the interconnections between the routers increase. On the other side, the power in the ring topology remains constant and small while increasing the number of tiers in the system and also doubling the number of routers per each tier as the increase of the interconnections is not that significant to change the power.

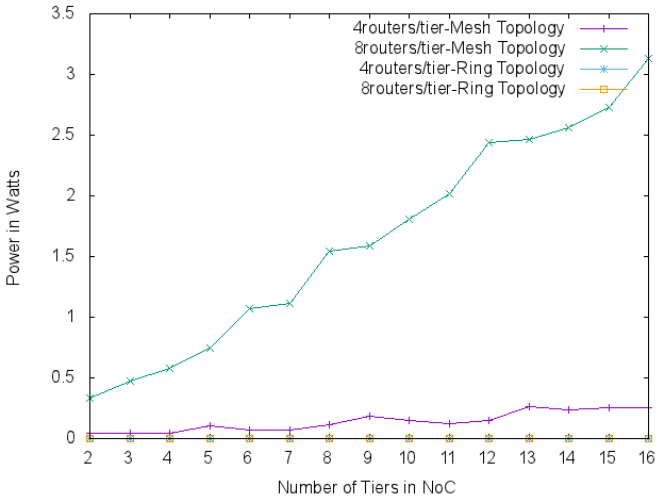

Fig. 5: Power in Watts Vs. Number of Tiers in NoC

Fig.6 and Fig.7 show the impact on the Lookup Tables(Luts) and the FlipFlops representing the area. While changing the number of tiers from the minimum to the maximum value. The area increases rapidly while doubling the number of routers in the mesh topology as the number of interconnections in the system grows exponentially with the increase of the number of routers to form the fully mesh network per each tier. On the other hand, the ring topology has moderate number of interconnections that reflects on the low rate of the increase in the area.

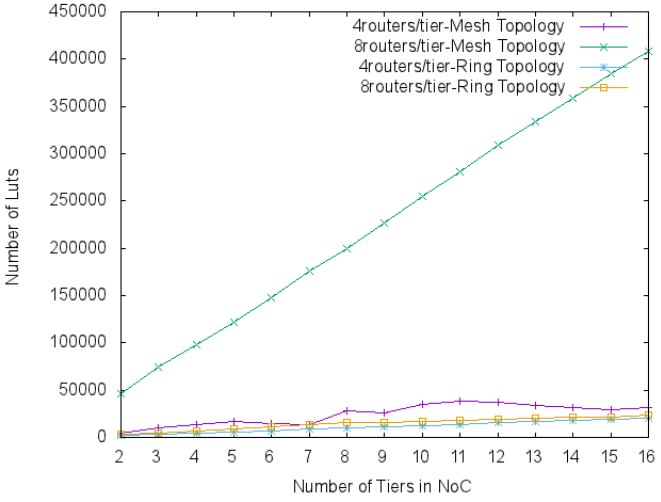

Fig. 6: Number of Luts Vs. Number of Tiers in NoC

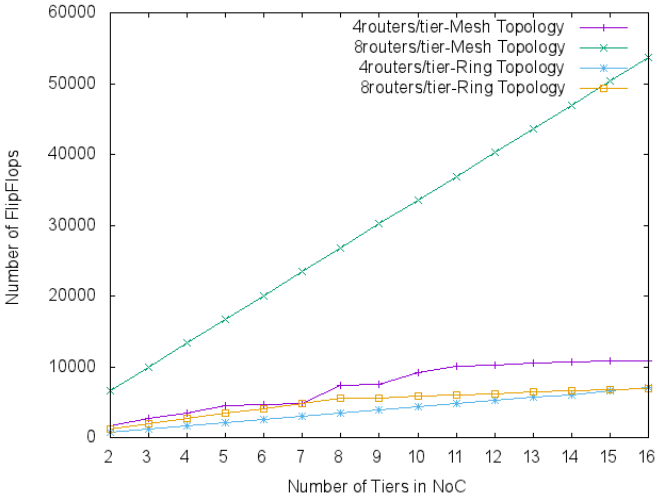

Fig. 7: Number of FlipFlops Vs. Number of Tiers in NoC

B. Tier Network Complexity in 3D-NoCs

The tier network complexity measures the effect of increasing the number of routers in each tier in the 3D-NoCs with mesh and ring planar topologies.

Fig.8 shows the latency while increasing the number of routers per each tier in the 3D-NoC. The latency of the routers connected in a fully planar mesh topology is constant and it doubles when doubling the number of tiers per the 3D-NoC system.

Meanwhile, it remains constant as the latency in mesh topology depends only on the number of vertical connections between tiers.

On the other side, the latency of the routers connected in ring planar topology increases linearly with the number of routers per tier in the 3D-NoC.

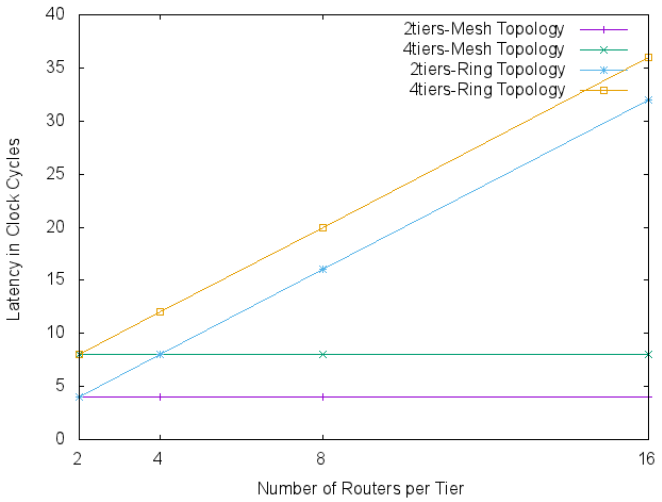

Fig. 8: Latency in Clock Cycles Vs. Number of Routers in Tier

Fig.9 shows the power while increasing the number of routers per each tier. The implementation of the 3D-NoC system in which the routers are connected in mesh topology in the planar level requires large logic to cover the fully mesh interconnections and the lookup table of each router, that reflects on the increase of the power while increasing the number of routers per each tier and also the number of tiers in the 3D-NoC. At the same time, the implementation of the 3D-NoC system in which the routers are connected in ring topology requires less interconnections and no lookup tables, that reflects on the low power consumption. That also clearly reflects on the area of the 3D-NoC represented in Luts and flipflops as shown in Fig.10 and Fig.11.

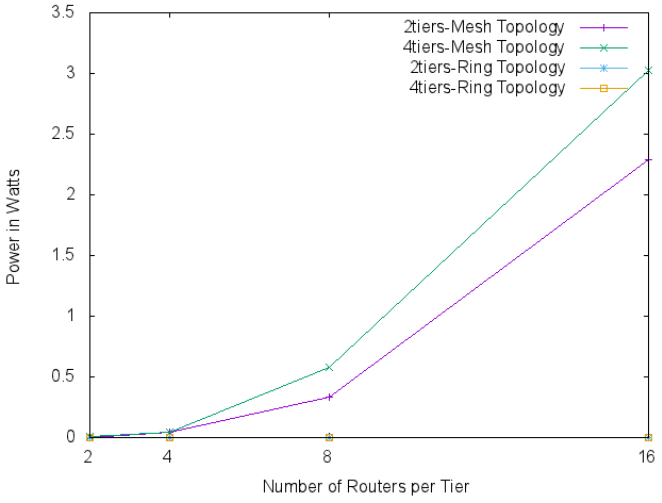

Fig. 9: Power in Watts Vs. Number of Routers in Tier

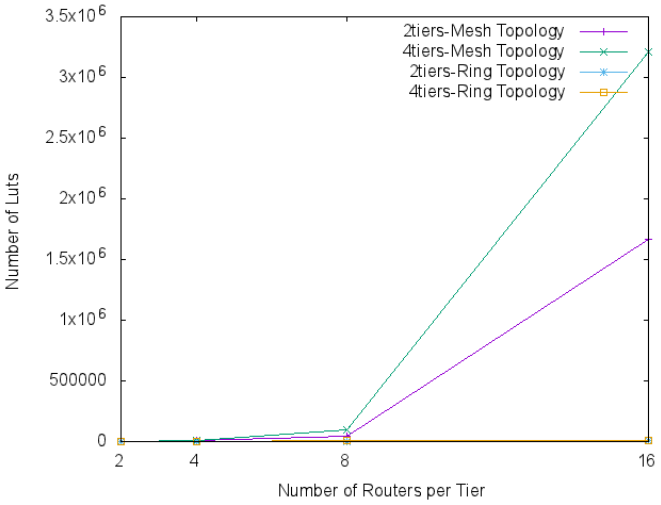

Fig. 10: Number of Luts Vs. Number of Routers in Tier

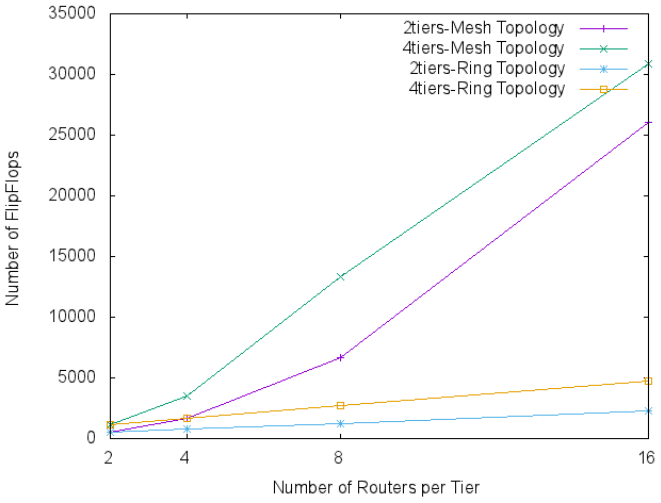

Fig. 11: Number of FlipFlops Vs. Number of Routers in Tier

V. Conclusion

The 3D-NOCET tool gives good insights about the different perfomance evaluations according to the main network factors which are the number of tiers, the number of routers per each tier and the planar topology in each tier. The fully mesh topology guarntees a faster 3D-NoC, but with a large area and power cost. Meanwhile, the ring topology offers a 3D-NoC with moderate area and power consumption, but a slower 3D-NoC compared to the mesh topology.

VI. Future Work

The 3D-NOCET tool offers a generic flexible solution to generate 3D-NoCs. To strengthen the flexibility and to allow the researchers to evaluate more and more 3D-NoCs, other planar topolgies can be supported in the router implementation such as star topology and torus topology. The tool also can be evaluated using other router implementations to study the impact of changing the router on the 3D-NoC system.

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