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Generation and classification of Kerwin–Huelsman–Newcomb circuits using the DVCC

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SUMMARY

New circuits realizing the Kerwin–Huelsman–Newcomb (KHN) and using three or four differential voltage current conveyor (DVCC) are generated from the basic KHN and inverted KHN block diagrams. The circuits are classified into two types, type A employs three DVCC and type B employs four DVCC. Each type includes four classes of circuits depending on the four possible integrator polarities. Each class can be realized by several circuits as will be demonstrated in the paper. All the eight possible sign combinations of the output voltages polarities are obtainable from the two types; four sign combinations from each type. The eight block diagrams are included to demonstrate the difference between each class of circuits. Spice simulation results demonstrating the practicality of the proposed filters are included. Copyright © 2008 John Wiley & Sons, Ltd.

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KEY WORDS: universal filters; differential voltage current conveyors; KHN circuit

1. INTRODUCTION

Analog integrated filters are basic building blocks in most electronic circuit applications. The state variable filter known in the literature as the Kerwin–Huelsman–Newcomb (KHN) filter [1] is a basic building block in many analog signal-processing applications. It provides the three basic filtering functions, namely the high-pass (HP), band-pass (BP) and low-pass (LP) responses. The circuit uses three operational amplifiers (Op Amps) as shown in Figure 1(a). Owing to the importance of this circuit, a brief review will be given here. The block diagram of the KHN circuit is shown in Figure 1(b), which consists of three stages, namely the summing stage and the two inverting integrators. The circuit equation for each stage is summarized in Table I and the three transfer functions polarities are given in Table II. The signal input of the KHN circuit is the non-inverting input terminal of the op amp as shown in Figure 1(a). It is also possible to inject the input signal

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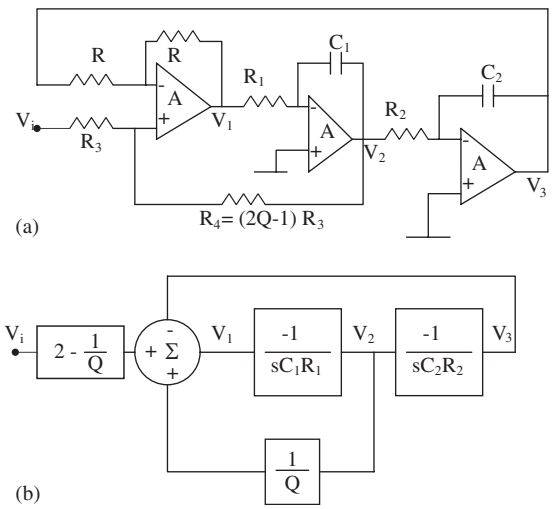

Figure 1. (a) The Kerwin–Huelsman–Newcomb (KHN) filter using three op amps [1] and (b) block diagram of the KHN circuit of (a).

Table I. Circuit equations of the three stages of KHN and inverted KHN.

Circuit	Summer stage	Integrator 1 $\frac{V_2}{V_1}$	Integrator 2 $\frac{V_3}{V_2}$
KHN Figure 1(a)	$V_1 = V_i\left[2-\frac{1}{Q}\right]+V_2\frac{1}{Q}-V_3$	$\frac{-1}{sC_1R_1}$	$\frac{-1}{sC_2R_2}$
Inverted KHN Figure 2(a)	$V_1 = -V_i+V_2\frac{1}{Q}-V_3$	$\frac{-1}{sC_1R_1}$	$\frac{-1}{sC_2R_2}$

Table II. The three output voltage polarities in KHN and inverted KHN.

Circuit	Polarity V_{HP}	Polarity V_{BP}	Polarity V_{LP}
KHN	+	−	+
Inverted KHN	−	+	−

to the inverting op amp terminal resulting in the inverted KHN filter shown in Figure 2(a) [2]. The inverted KHN circuit uses one resistor more than the classical KHN and it differs only in the summation stage. The block diagram of the inverted KHN is shown in Figure 2(b) and the circuit equations for each stage is given in Table I. The polarities of the three outputs are given in Table II and they are opposite to those of the classical KHN and is defined as the inverted KHN for this reason. Both KHN and the inverted KHN filters belong to the two integrator loop class of filters [3, 4]. Such filters suffer from the finite gain bandwidth of the op amp, which results in a pole Q enhancement thus limiting the frequency of operation of the filter [4–6]. The finite gain bandwidth effect on the filter performance has been studied [4] and methods of active compensation has been developed to improve the circuit operation [5, 6]. Universal filter structure that uses the three

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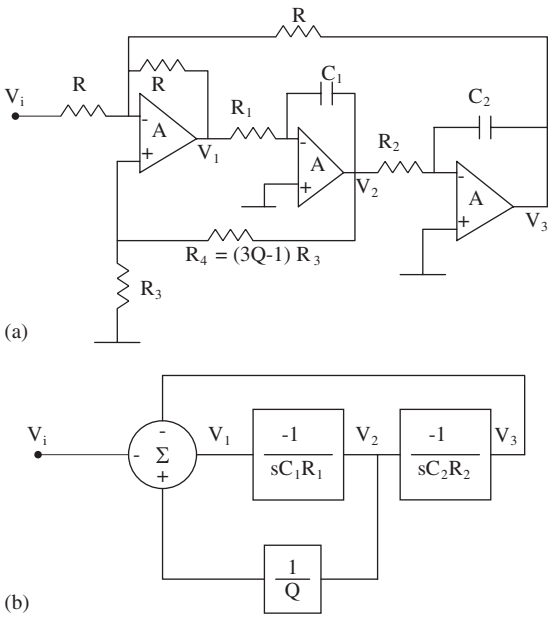

Figure 2. (a) The inverted polarity KHN filter using three op amps [2] and (b) block diagram of the inverted polarity KHN circuit of (a).

single ended op amps and MOS transistors has been introduced in the literature [7]. Other forms of MOS-C KHN filters using active devices other than the op amp have been also introduced in the literature [8]. The starting point in the MOS-C filter design is an active RC prototype [7]; therefore, it is necessary to develop new active RC filters using active devices that can operate at higher frequencies than the op amp.

The KHN circuit using current conveyors (CCII) [9] was introduced in [10] with a one to one correspondence to the three building blocks in the classical KHN resulting in circuits with four or three floating resistors. Shortly thereafter it was modified to have all grounded resistors and capacitors [11] and to provide all possible eight sign combinations of the three filter responses by changing the polarity of the Z terminal of the CCII [11]. Current mode two integrator loop filters using CCII was also introduced in the literature in [12].

Recently new type of universal voltage mode filter using the differential voltage current conveyor (DVCC) has been introduced in [13, 14]. The circuit reported in [13] employs two floating resistors and has no independent control on Q. The circuit reported in [14] is based on three input excitations and has no independent control on Q also.

The single output differential difference current conveyor has been introduced in [15]. The same circuit defined as DVCC with a balanced output has also been introduced independently in [16]. The DVCC is defined in [16] as a five port building block having

$$I_{Y_1} = I_{Y_2} = 0, \quad V_x = V_{Y_1} - V_{Y_2}, \quad I_{Z+} = I_x \quad \text{and} \quad I_{Z-} = -I_x \tag{1}$$

It is seen that the DVCC includes CCII+, CCII− and both types of inverting CCII (ICCII) as special cases [17–19].

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Active RC circuits of the Tow Thomas two integrator loop filter using the DVCC and the ICCII have been introduced in [15, 19], respectively.

In this paper several new circuits realizing the KHN and using three or four DVCC are generated from the basic KHN and inverted KHN block diagrams. The circuits are classified into two types, type A employs three DVCC and type B employs four DVCC. Each type includes four classes of circuits depending on the four possible integrator polarities. Each class can be realized by several circuits as will be demonstrated in the paper. All the eight possible sign combinations of the output voltages polarities are obtainable from the two types; four sign combinations from each type.

It is worth noting that the proposed KHN circuits using the DVCC employs three DVCC, two grounded capacitors and four grounded resistors, on the other hand, the KHN circuit using CCII reported in [11] employs five CCII, two grounded capacitors and six grounded resistors.

2. TYPE A—KHN CIRCUITS USING THREE DVCC

In this section the type A-KHN circuits using three DVCC are classified into four classes based on the two integrators polarities. Five equivalent circuits of the class I type A-circuits are shown in Figure 3.

Table III includes the three basic equations for the type A-KHN circuits. Solving the three equations in the first row results in the voltage transfer functions for this class of circuits; taking $R_4 = R_3$, the three transfer functions are given by

$$\frac{V_1}{V_i} = \frac{s^2 C_1 C_2 R_1 R_2}{s^2 C_1 C_2 R_1 R_2 + s C_2 R_3 + 1} \tag{2a}$$

$$\frac{V_2}{V_i} = \frac{-s C_2 R_2}{s^2 C_1 C_2 R_1 R_2 + s C_2 R_3 + 1} \tag{2b}$$

$$\frac{V_3}{V_i} = \frac{1}{s^2 C_1 C_2 R_1 R_2 + s C_2 R_3 + 1} \tag{2c}$$

The ω_0 and Q are given, respectively, by

$$\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}}, \quad Q = \frac{1}{R_3}\sqrt{\frac{C_1 R_1 R_2}{C_2}} \tag{3}$$

The design equations are given by taking $C_1 = C_2 = C$

$$R_1 = R_2 = 1/\omega_0 C, \quad R_3 = R_4 = R_1/Q \tag{4}$$

It is seen that Q is controlled by the two equal resistors R_3 and R_4.

The band-pass center frequency gain $= Q$ and the LP DC gain is unity as well as the HP high-frequency gain is also unity.

Figure 3(b) represents the block diagram of the type A-class I circuits. It is similar to the classical KHN block diagram of Figure 1(a) except that the forward gain of the input voltage to the summer is unity.

It is seen that the circuit of Figure 3(a) uses only $Z+$ DVCC, which is an advantage in avoiding current mirrors for current transfer from X to Z terminals. The other four circuits given represent a variety of equivalent circuits based on terminal interchanges of the DVCC.

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The class II circuits employ two non-inverting integrators and three equivalent circuits are given in Figure 4 together with the block diagram shown in Figure 4(b), which is different from that of Figure 3(b). The three output voltages are all non-inverting, which could not be achieved with the three op amp KHN. The transfer functions and the design equations are the same as given by Equations (2) and (4) except for the sign of the band-pass, which is positive as given in Table IV. It is seen that the circuit of Figure 4(a) is the only circuit from this class which uses only $Z+$ DVCC, which is an advantage in avoiding current mirrors for current transfer from X to Z terminals and consumes less power than the circuits using the balanced output DVCC.

The class III circuits employ an inverting integrator and a non-inverting integrator and three equivalent circuits are given in Figure 5 together with the block diagram shown in Figure 5(b). The transfer functions and the design equations are the same as given by Equations (2) and (4)

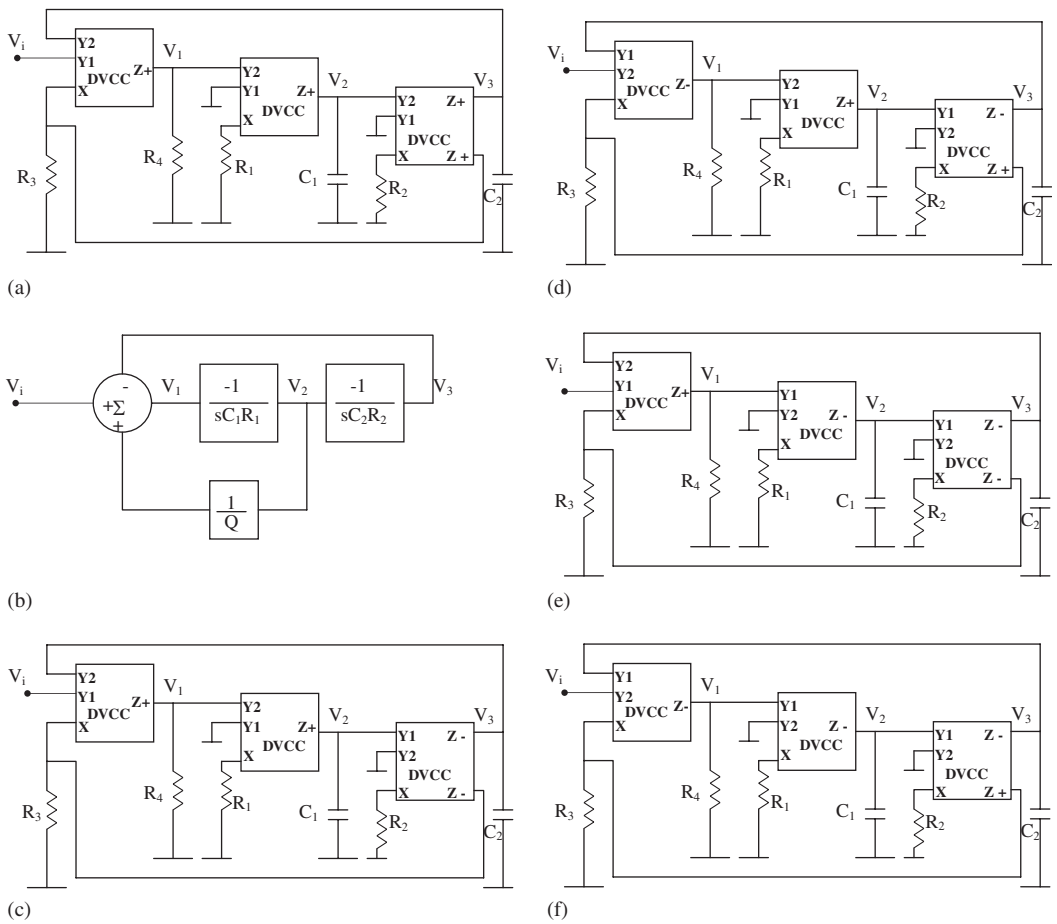

Figure 3. (a) Type A-class I-circuit 1 grounded resistor and capacitor KHN circuit and (b) block diagram of type A-class I KHN circuits, (c) circuit 2, (d) circuit 3, (e) circuit 4, and (f) circuit 5.

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Table III. Circuit equations of the three stages of the type A-KHN.

Type A class	Summer stage $R_4 = R_3$	Integrator 1 $\frac{V_2}{V_1}$	Integrator 2 $\frac{V_3}{V_2}$
I	$V_1 = V_i + \frac{R_4}{R_2} V_2 - V_3$	$\frac{-1}{sC_1R_1}$	$\frac{-1}{sC_2R_2}$
II	$V_1 = V_i - \frac{R_4}{R_2} V_2 - V_3$	$\frac{1}{sC_1R_1}$	$\frac{1}{sC_2R_2}$
III	$V_1 = -V_i + \frac{R_4}{R_2} V_2 + V_3$	$\frac{-1}{sC_1R_1}$	$\frac{1}{sC_2R_2}$
IV	$V_1 = -V_i - \frac{R_4}{R_2} V_2 + V_3$	$\frac{1}{sC_1R_1}$	$\frac{-1}{sC_2R_2}$

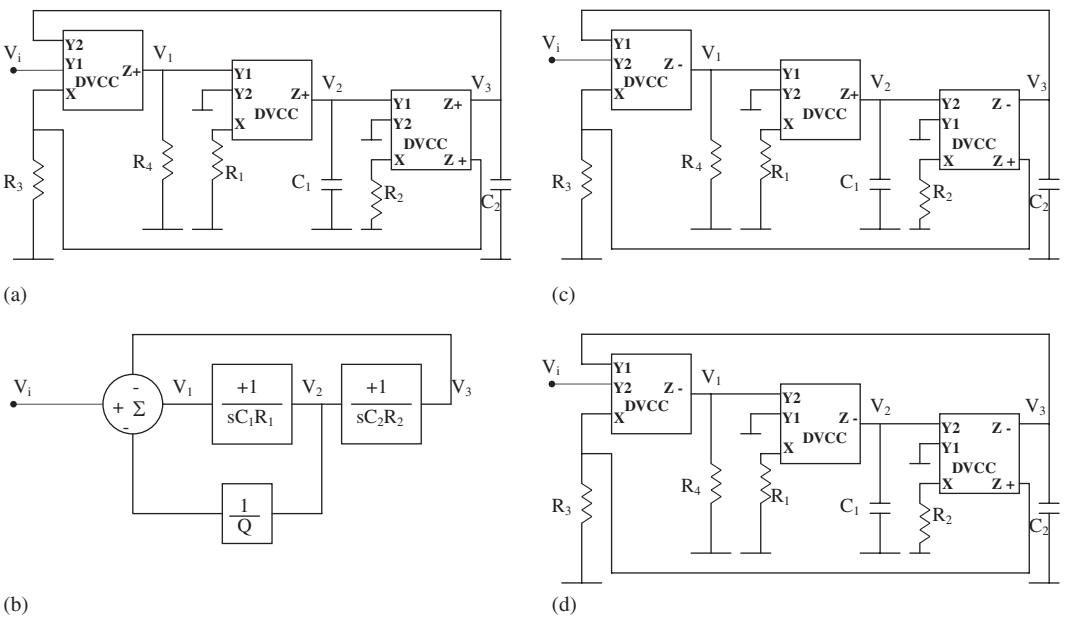

Figure 4. Type A-class II circuit 1 grounded resistor and capacitor KHN circuit and (b) block diagram of type A-class II KHN circuits, (c) circuit 2, and (d) circuit 3.

Table IV. Three output voltage polarities in type A-KHN circuits.

Type A-class	Polarity V_{HP}	Polarity V_{BP}	Polarity V_{LP}
I	+	−	+
II	+	+	+
III	−	+	+
IV	−	−	+

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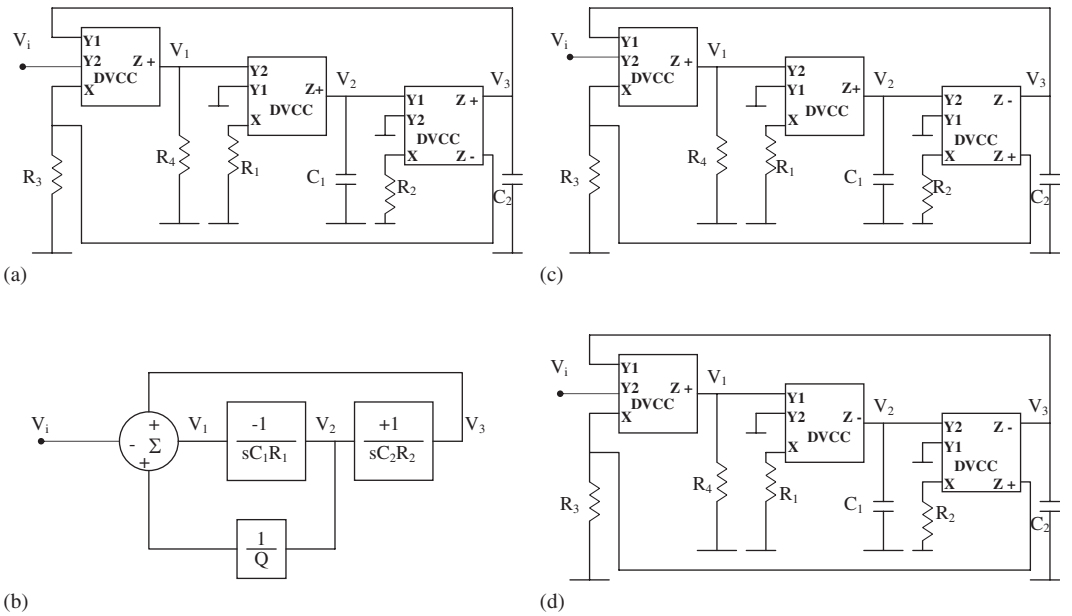

Figure 5. (a) Type A-class III circuit 1 grounded resistor and capacitor KHN circuit and (b) block diagram of type A-class III KHN circuits, (c) circuit 2, and (d) circuit 3.

except for the signs of the HP and the band-pass which are negative and positive, respectively, as given in Table IV.

The class IV circuits employ a non-inverting integrator followed by an inverting integrator and three equivalent circuits are given in Figure 6 together with the block diagram shown in Figure 6(b). The transfer functions and the design equations are the same as given by Equations (2) and (4) except for the sign of the HP which is negative as given in Table IV.

The above four classes provide four possible sign combinations of the three filter responses, so there are four more possible sign combinations. Based on the three DVCC structure used in the type-A circuits and to avoid the use of floating resistors a new type of the KHN circuits referred to as type-B will be introduced in the next section to achieve the remaining feedback mixing combinations.

3. TYPE B-KHN CIRCUITS USING FOUR DVCC

The type-B KHN circuits include four classes of circuits and employ four DVCC, two capacitors and five resistors, that is, it uses one DVCC and one resistor more than the type-A KHN.

3.1. Class I-type B-KHN

Figure 7 represents three equivalent type-B class I KHN circuits using two inverting integrators and the block diagram is shown in Figure 7(b). The circuit equation for each block is given in

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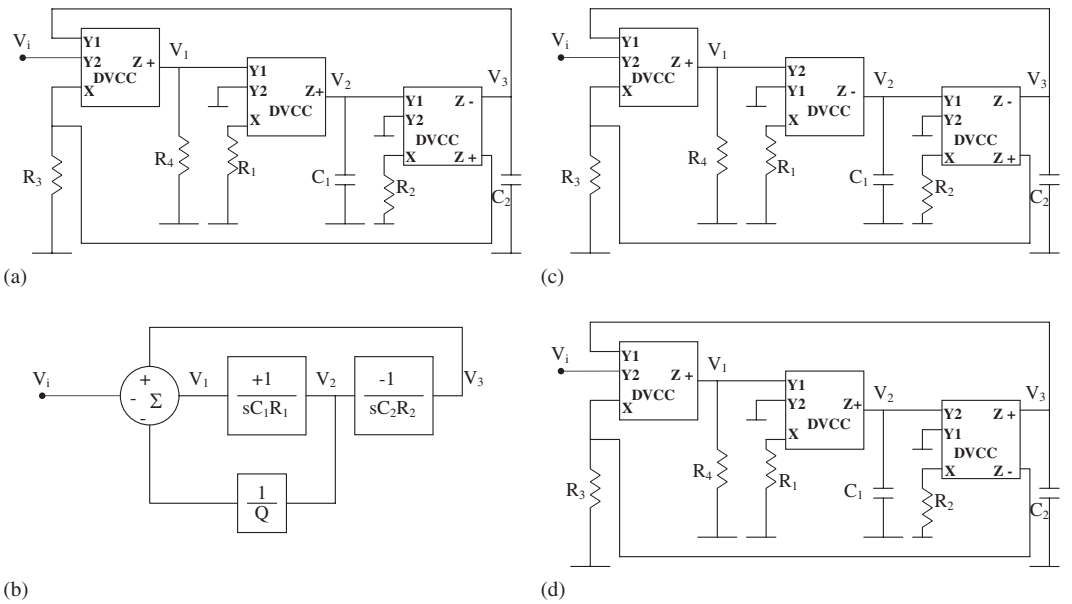

Figure 6. (a) Type A-class IV circuit 1 grounded resistor and capacitor KHN circuit and (b) block diagram of type A-class IV KHN circuits, (c) circuit 2, and (d) circuit 3.

Table V. Solving the three equations of the three blocks the three transfer functions are obtained as:

$$\frac{V_1}{V_i} = \frac{-s^2 C_1 C_2 R_1 R_2 \dfrac{R_4}{R_3}}{s^2 C_1 C_2 R_1 R_2 + sC_2 R_2 \dfrac{R_4}{R_3} + \dfrac{R_4}{R_5}} \tag{5a}$$

$$\frac{V_2}{V_i} = \frac{sC_2 R_2 \dfrac{R_4}{R_3}}{s^2 C_1 C_2 R_1 R_2 + sC_2 R_2 \dfrac{R_4}{R_3} + \dfrac{R_4}{R_5}} \tag{5b}$$

$$\frac{V_3}{V_i} = \frac{-\dfrac{R_4}{R_3}}{s^2 C_1 C_2 R_1 R_2 + sC_2 R_2 \dfrac{R_4}{R_3} + \dfrac{R_4}{R_5}} \tag{5c}$$

Taking $R_5 = R_4$ (and is arbitrary), the ω_0 and Q are given, respectively, by

$$\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}}, \quad Q = \frac{R_3}{R_4}\sqrt{\frac{C_1 R_1}{C_2 R_2}} \tag{6}$$

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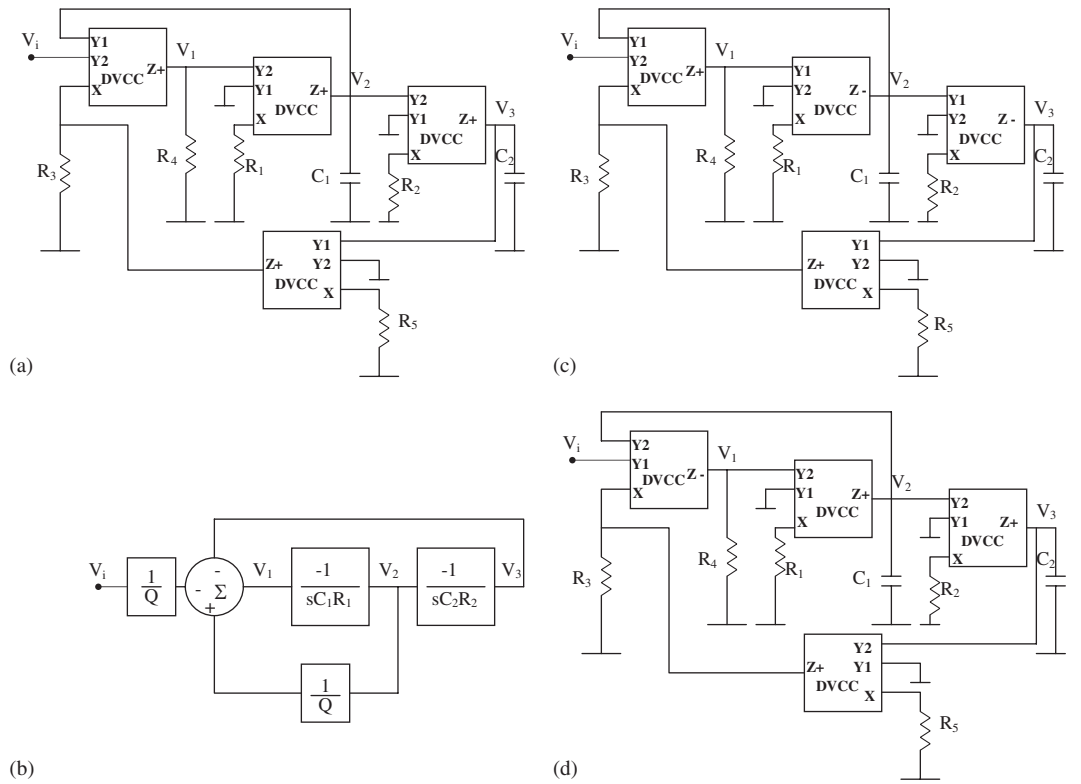

Figure 7. (a) Type B-class I grounded R and C KHN circuit 1 using four DVCC and (b) block diagram of the type B-class I-KHN circuit. Type B-class I Grounded R and C KHN (c) circuit 2 using four DVCC and (d) circuit 3 using four DVCC.

The design equations are given by taking $C_1 = C_2 = C$

$$R_1 = R_2 = 1/\omega_0 C, \quad R_3 = Q R_4 \tag{7}$$

It is seen that Q is controlled by R_3 without affecting ω_0 which is an advantage over type-A circuits in which Q is adjusted by varying two equal resistors.

3.2. Class II-type B-KHN

The class II circuits employ a non-inverting integrator followed by an inverting integrator and the circuit is given in Figure 8(a) together with the block diagram shown in Figure 8(b), which is different from that of Figure 7(b) in all of the three signs at the summation stage. The transfer functions and the design equations are the same as given by Equations (5) and (7) except for the sign of the HP which is positive as given in Table VI.

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Table V. Circuit equations of the three stages of the type B-KHN.

Type B class	Summer stage $R_4 = R_5$	Integrator 1 $\frac{V_2}{V_1}$	Integrator 2 $\frac{V_3}{V_2}$
I	$V_1 = -\frac{R_4}{R_3}V_i + \frac{R_4}{R_3}V_2 - V_3$	$\frac{-1}{sC_1R_1}$	$\frac{-1}{sC_2R_2}$
II	$V_1 = \frac{R_4}{R_3}V_i - \frac{R_4}{R_3}V_2 + V_3$	$\frac{1}{sC_1R_1}$	$\frac{-1}{sC_2R_2}$
III	$V_1 = \frac{R_4}{R_3}V_i + \frac{R_4}{R_2}V_2 + V_3$	$\frac{-1}{sC_1R_1}$	$\frac{+1}{sC_2R_2}$
IV	$V_1 = -\frac{R_4}{R_3}V_i - \frac{R_4}{R_2}V_2 - V_3$	$\frac{+1}{sC_1R_1}$	$\frac{+1}{sC_2R_2}$

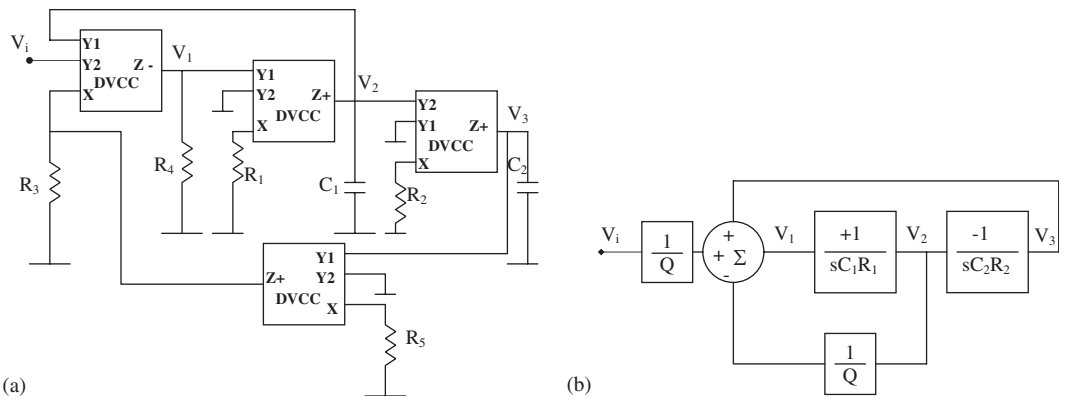

Figure 8. (a) Type B-class II-Grounded R and C KHN circuit using four DVCC and (b) block diagram of the type B-class II-KHN circuit.

Table VI. Three output voltage polarities in type B-KHN circuits.

Type B-class	Polarity V_{HP}	Polarity V_{BP}	Polarity V_{LP}
I	−	+	−
II	+	+	−
III	+	−	−
IV	−	−	−

3.3. Class III-type B-KHN

In this class the integrators are inverting and non-inverting, respectively. In this case the summation of V_i, V_2 and V_3 will be different from all previous classes as they are mixed with the same polarity. In this case both types of feedback from V_2 and V_3 will be based on shunt mixing as shown in Figure 9(a). The circuit equation for each block is given in Table V. Solving the three equations

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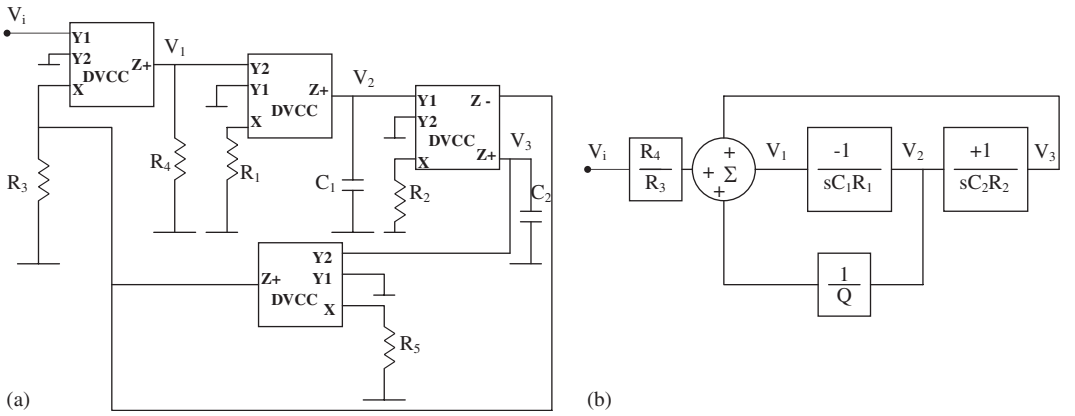

Figure 9. (a) Type B-class III-grounded R and C KHN circuit using four DVCC and (b) block diagram of the type B-class III-KHN circuit.

of the three blocks and taking $R_5 = R_4$ the three transfer functions are obtained as:

$$\frac{V_2}{V_i} = \frac{s^2 C_1 C_2 \dfrac{R_1 R_2 R_4}{R_3}}{s^2 C_1 C_2 R_1 R_2 + s C_2 R_4 + 1} \tag{8a}$$

$$\frac{V_2}{V_i} = \frac{-s C_2 \dfrac{R_2 R_4}{R_3}}{s^2 C_1 C_2 R_1 R_2 + s C_2 R_4 + 1} \tag{8b}$$

$$\frac{V_3}{V_i} = \frac{-\dfrac{R_4}{R_3}}{s^2 C_1 C_2 R_1 R_2 + s C_2 R_4 + 1} \tag{8c}$$

The ω_0 and Q are given, respectively, by

$$\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}}, \quad Q = \frac{1}{R_4}\sqrt{\frac{C_1 R_1 R_2}{C_2}} \tag{9}$$

The design equations are given by taking $C_1 = C_2 = C$

$$R_1 = R_2 = 1/\omega_0 C, \quad R_4 = R_1/Q \tag{10}$$

It is seen that Q is controlled by the two equal resistors R_4 and R_5 without affecting ω_0 which is the same as in type-A circuits in which Q is adjusted by varying two equal resistors. The circuit block diagram is shown in Figure 9(b).

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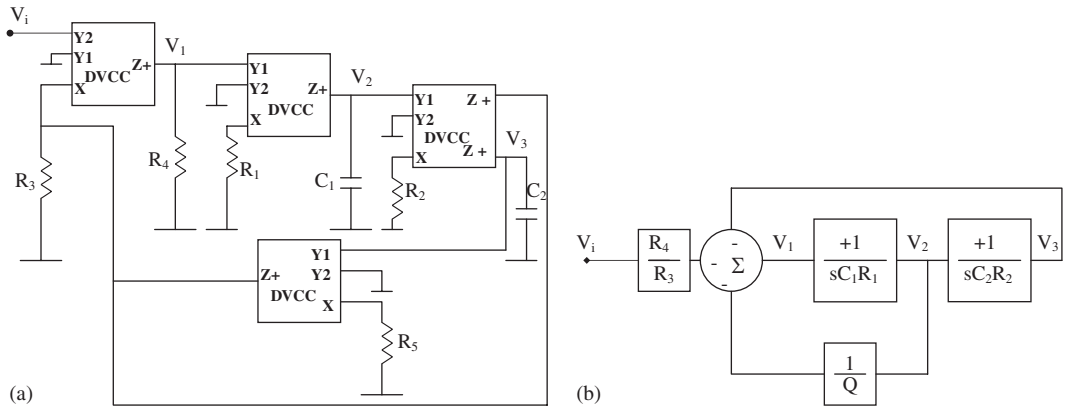

Figure 10. (a) Type B-class IV grounded R and C KHN circuit using four DVCC and (b) block diagram of the type B-class IV KHN circuit.

Examining the circuit of Figure 9(a) it is seen that all the four DVCC are used with one Y input thus this circuit can also be realized with four CCII, but in this case two of the DVCC will be replaced by two CCII− to achieve the same signs. Of course it is an advantage to use DVCC having $Z+$ outputs over using the CCII with $Z-$ outputs.

3.4. Class IV-type B-KHN

In this class the integrators are both non-inverting and in this case the summation of V_i, V_2 and V_3 will be mixed with an inverting polarity, which is opposite to mixing sign in the class III. In this case both types of feedback from V_2 and V_3 will be based on shunt mixing (as in class III) as shown in Figure 10(a). The circuit block diagram is shown in Figure 10(b) and the circuit equation for each block is given in Table V.

The transfer functions and the design equations are the same as given by Equations (8) and (10) except for the sign of the HP which is negative as given in Table VI.

Examining the circuit of Figure 10(a) it is seen that all the four DVCC are used with one Y input thus this circuit can also be realized with four CCII, but in this case the three DVCC will be replaced by two CCII− and one balanced output CCII to achieve the same signs. Of course it is an advantage to use DVCC having $Z+$ outputs over using the CCII with $Z-$ outputs since current mirrors will be avoided in current transfer to port Z.

4. SIMULATION RESULTS

Spice simulation results using technology SCN 05 feature size 0.5 μm from MOSIS vendor: AGILENT and the CMOS parameters are given in Table VII. Figure 11(a) represents the CMOS circuit of a DVCC with a double output $Z+$ terminal that can be used with the KHN circuits of Figures 3(a), 4(a), 7(a) and 10(a) reported in this paper.

The operation of the circuits of Figure 11 is insensitive to the threshold voltage variation caused by the body effect. All the PMOS transistors have sources that are connected to V_{DD}, while all the

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Table VII. Mosis parametric test results.

RUN: T1AY VENDOR: AGILENT
TECHNOLOGY: SCN05 FEATURE SIZE: 0.5-μm

T1AY SPICE BSIM3 VERSION 3.1 PARAMETERS
SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8
*DATE: Dec 20/01
*LOT: T1AY WAF: 5257
*Temperature_parameters=Default

.MODEL CMOSN NMOS (LEVEL=49
+VERSION=3.1 TNOM=27 TOX=9.6E−9
+XJ=1.5E−7 NCH=1.7E17 VTH0=0.6483663
+K1=0.785558 K2=−0.0281666 K3=66.1499719
+K3B=0.3568819 W0=1E−5 NLX=4.818148E−8
+DVT0W=0 DVT1W=0 DVT2W=0
+DVT0=6.2143051 DVT1=0.8626149 DVT2=−0.1445423
+U0=433.5416887 UA=1.155899E−12 UB=1.586984E−18
+UC=1.93783E−11 VSAT=1.191034E5 A0=0.9506575
+AGS=0.1587282 B0=1.669745E−6 B1=5E−6
+KETA=1.295011E−3 A1=0 A2=1
+RDSW=1.420487E3 PRWG=7.314585E−3 PRWB=−0.057998
+WR=1 WINT=2.298334E−7 LINT=1.044286E−7
+XL=−1E−7 XW=0 DWG=−6.736529E−9
+DWB=1.106778E−8 VOFF=−0.0721654 NFACTOR=1.3430839
+CIT=0 CDSC=2.4E−4 CDSCD=0
+CDSCB=0 ETA0=0.1497588 ETAB=−1.615258E−3
+DSUB=0.8064761 PCLM=0.6735544 $PDIBLC_1$=1.986696E−3
+$PDIBLC_2$=1.283923E−3 PDIBLCB=−0.4066049 DROUT=0.0385606
+PSCBE1=4.272111E10 PSCBE2=1.948039E−8 PVAG=0.1731962
+DELTA=0.01 RSH=2.8 MOBMOD=1
+PRT=0 UTE=−1.5 KT1=−0.11
+KT1L=0 KT2=0.022 UA1=4.31E−9
+UB1=−7.61E−18 UC_1=−5.6E−11 AT=3.3E4
+WL=0 WLN=1 WW=0
+WWN=1 WWL=0 LL=0
+LLN=1 LW=0 LWN=1
+LWL=0 CAPMOD=2 XPART=0.5
+CGDO=2.58E−10 CGSO=2.58E−10 CGBO=1E−9
+CJ=5.099718E−4 PB=0.99 MJ=0.8004678
+CJSW=4.710071E−10 PBSW=0.99 MJSW=0.1
+CJSWG=2.2346E−10 PBSWG=0.99 MJSWG=0.1
+CF=0 PVTH0=2.017836E−3 PRDSW=−58.6417673
+PK2=9.166371E−3 WKETA=−4.350083E−3 LKETA=−0.0111891
+PAGS=0.0968

.MODEL CMOSP PMOS (LEVEL=49
+VERSION=3.1 TNOM=27 TOX=9.6E−9
+XJ=1.5E−7 NCH=1.7*E*17 VTH0=−0.8383834
+K1=0.3788685 K2=0.0214697 K3=86.4688573
+K3B=−5 W0=1E−5 NLX=2.031912E−7
+DVT0W=0 DVT1W=0 DVT2W=0 DVT0=3.4382916 DVT1=
0.521383 DVT2=−0.0409272
+U0=182.6903678 UA=1.386759E−9 UB=1.042229E−18

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Table VII. *Continued*.

+UC = −5.27252E−11 VSAT = 2.212376E5 *A*0 = 1.0076933
+AGS = 0.3094791 B0 = 4.390319E−6 B1 = 5E−6
+KETA = 1.979498E−3 A1 = 0A2 = 1
+RDSW = 3.5E3 PRWG = 5.885773E−4 PRWB = 0.0487413
+WR = 1 WINT = 2.227753E−7 LINT = 4.452357E−8
+XL = −1E−7 XW = 0 DWG = −1.906589E−8
+DWB = 7.860856E−9 VOFF = −0.102204 NFACTOR = 0.8806869
+CIT = 0 CDSC = 2.4E−4 CDSCD = 0
+CDSCB = 0 ETA0 = 0.0372607 ETAB = 3.880962E−3
+DSUB = 0.2239032 PCLM = 4.5968321 $PDIBLC_1$ = 5.937743E−5
+$PDIBLC_2$ = 3.951956E−3 PDIBLCB = −0.5 DROUT = 0
+PSCBE1 = 8E10 PSCBE2 = 7.602193E−9 PVAG = 13.2601653
+DELTA = 0.01 RSH = 2.5 MOBMOD = 1
+PRT = 0 UTE = −1.5 KT1 = −0.11 KT1L = 0 KT2 = 0.022 UA1 = 4.31E−9
+UB1 = −7.61E−18 UC_1 = −5.6E−11 AT = 3.3E4
+WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 2.44E−10 CGSO = 2.44E−10 CGBO = 1E−9
+CJ = 9.444673E−4 PB = 0.9358919 MJ = 0.4757353
+CJSW = 1.492172E−10 PBSW = 0.3189517 MJSW = 0.1124474
+CJSWG = 4.256E−11 PBSWG = 0.3189517 MJSWG = 0.1124474
+CF = 0 PVTH0 = 7.703892E−3 PRDSW = 258.8687021
+PK2 = 2.699384E−3 WKETA = 9.038445E−3 LKETA = −0.0117499
+PAGS = 0.09532

NMOS transistors except M_1 to M_4 have sources connected to VSS. This causes no variation in the threshold voltage because the source to body voltage is maintained equal to zero at all times. Although the sources of transistors M_1 and M_2 are not connected to the body, their operation is still unaffected by the body effect because they form a differential pair, and hence have the same source voltage. This causes equal variation in the threshold voltage of M_1 and M_2 and hence the two threshold voltage cancels out. The same is true for the differential pair M_3 and M_4. Therefore, the circuits shown in Figure 11 can be implemented effectively in either N-well or P-well CMOS process [16].

The spice simulations reported next are carried out using the CMOS-DVCC of Figures 11(a) and (b) [16] with the aspect ratios given in Table VIII(a) and (b), respectively, and with $V_{DD} = 1.5\,V$, $V_{SS} = -1.5\,V$.

The circuit of Figure 3(a) is simulated to have $f_0 = 1\,MHz$ and $Q = 0.707$ for LP maximally flat magnitude response using the CMOS circuit of Figure 11(a).

The circuit design parameters taken are $C_1 = C_2 = 10\,PF$, $R_1 = R_2 = 15.9\,k\Omega$, $R_3 = R_4 = 22.5\,k\Omega$.

Figure 12(a) represents the magnitude and phase characteristics together with the ideal response. It is seen that the simulated results agree well with the ideal responses. Total power dissipation is equal to 2.0598 mW.

The circuit of Figure 3(a) is simulated again for $f_0 = 1\,MHz$ and $Q = 10$ for a band-pass response and using the CMOS circuit of Figure 11(a).

The circuit design parameters taken are $C_1 = C_2 = 10\,PF$, $R_1 = R_2 = 15.9\,k\Omega$, $R_3 = R_4 = 1.59\,k\Omega$.

Figure 12(b) represents the magnitude and phase characteristics together with the ideal response. It is seen that the simulated results agree well with the ideal responses.

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The circuit of Figure 3(d) is simulated to have $f_0 = 1\,\text{MHz}$ and $Q = 0.707$ for LP maximally flat magnitude response and $Q = 10$ for band-pass response. The circuit design parameters are the same as given above.

Figure 13(a) represents the magnitude and phase characteristics of the LP response together with the ideal response. It is seen that the simulated results agree well with the ideal responses. Total power dissipation is equal to 2.9338 mW.

Figure 13(b) represents the magnitude and phase characteristics of the band-pass response together with the ideal response. It is seen that the simulated results agree well with the ideal responses.

Next, the circuit of Figure 4(a) is simulated to have $f_0 = 1\,\text{MHz}$ and $Q = 0.707$ for LP maximally flat magnitude response and $Q = 10$ for band-pass response. The circuit design parameters are the same as given above.

Figure 14(a) represents the magnitude and phase characteristics of the LP response together with the ideal response. The total power dissipation is equal to 2.8018 mW.

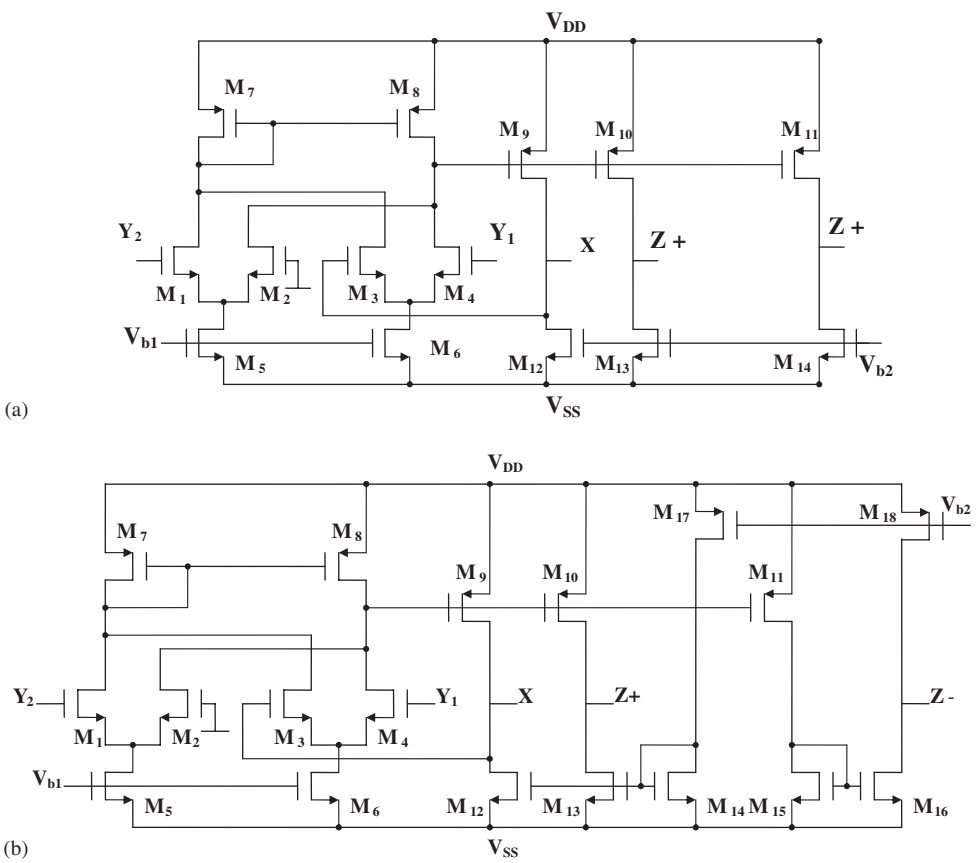

Figure 11. (a) The CMOS DVCC with double $Z+$ outputs and (b) with balanced outputs $Z+$ and $Z-$ [16].

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Table VIII. Transistor aspect ratios of the CMOS DVCC shown in: (a) Figure 11(a) and (b) Figure 11(b).

NMOS transistors	W (μm)/L (μm)
(a)	
M_1, M_2, M_3, M_4	8/1
M_5, M_6	8/1
M_{12}, M_{13}, M_{14}	20/2.5
PMOS transistors	W (μm)/L (μm)
M_7, M_8	10/1
M_9, M_{10}, M_{11}	40/2
NMOS transistors	W (μm)/L (μm)
(b)	
M_1, M_2, M_3, M_4	8/1
M_5, M_6	8/1
M_{12}, M_{13}, M_{14}, M_{15}, M_{16}	20/2.5
PMOS transistors	W (μm)/L (μm)
M_7 and M_8	10/1
M_9, M_{10}, M_{11}, M_{17}, M_{18}	40/2

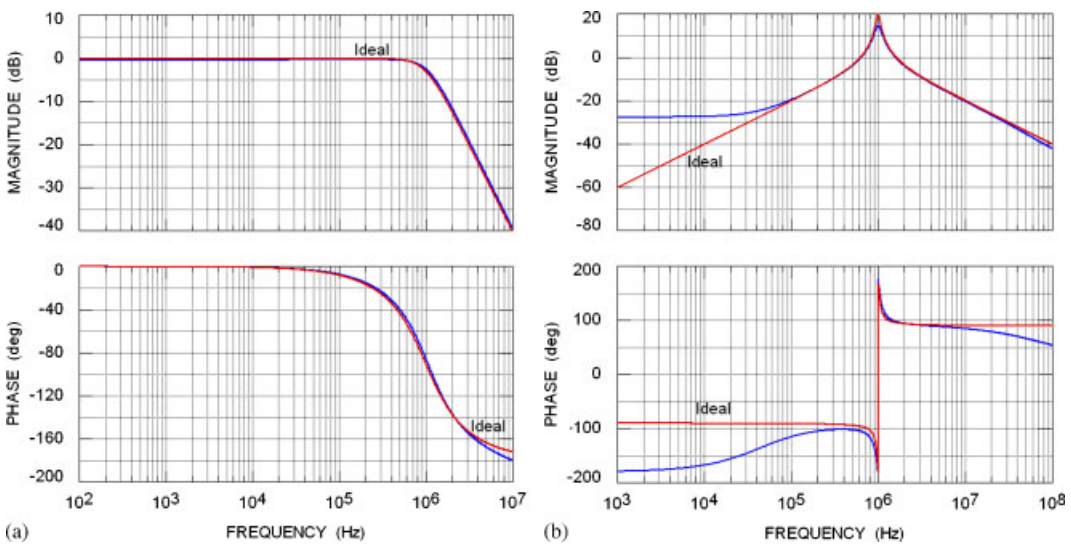

Figure 12. Magnitude and phase characteristics of the (a) low-pass response and (b) band-pass response of the circuit of Figure 3(a) for $f_0 = 1$ MHz.

Figure 14(b) represents the magnitude and phase characteristics of the band-pass response together with the ideal response. It is seen that the simulated results agree well with the ideal responses.

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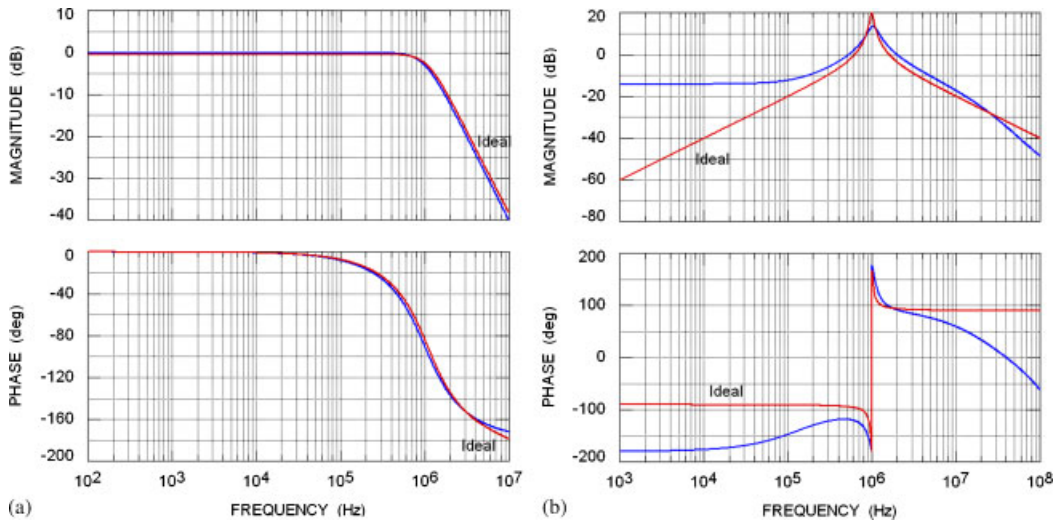

Figure 13. Magnitude and phase characteristics of the (a) low-pass response and (b) band-pass response of the circuit of Figure 3(d) for $f_0 = 1\,\text{MHz}$.

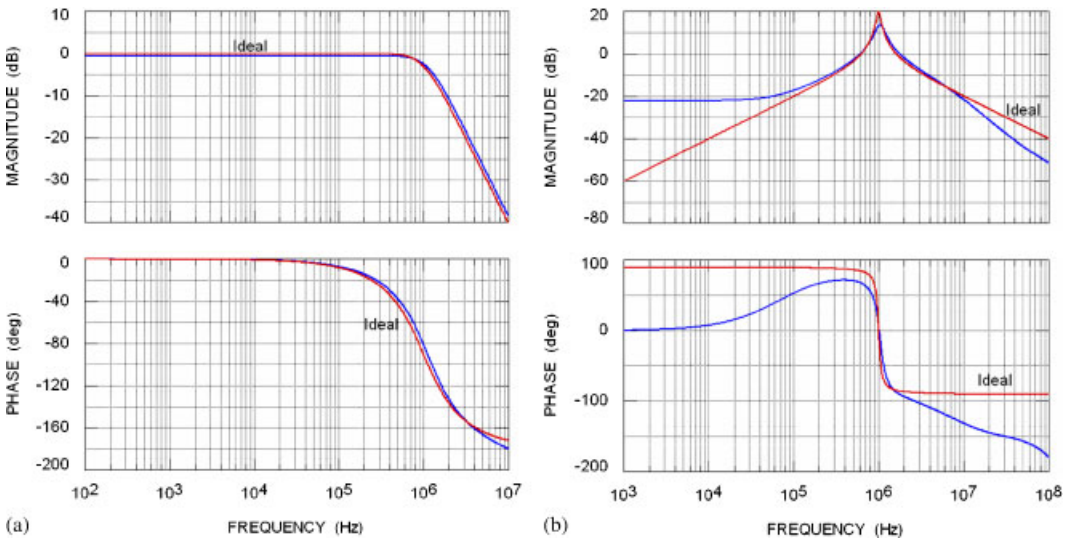

Figure 14. Magnitude and phase characteristics of the (a) low-pass response and (b) band-pass response of the circuit of Figure 4(a) at $f_0 = 1\,\text{MHz}$.

Next, the circuit of Figure 4(c) is simulated to have $f_0 = 1\,\text{MHz}$ and $Q = 0.707$ for LP maximally flat magnitude response and $Q = 10$ for band-pass response. The circuit design parameters are the same as given above.

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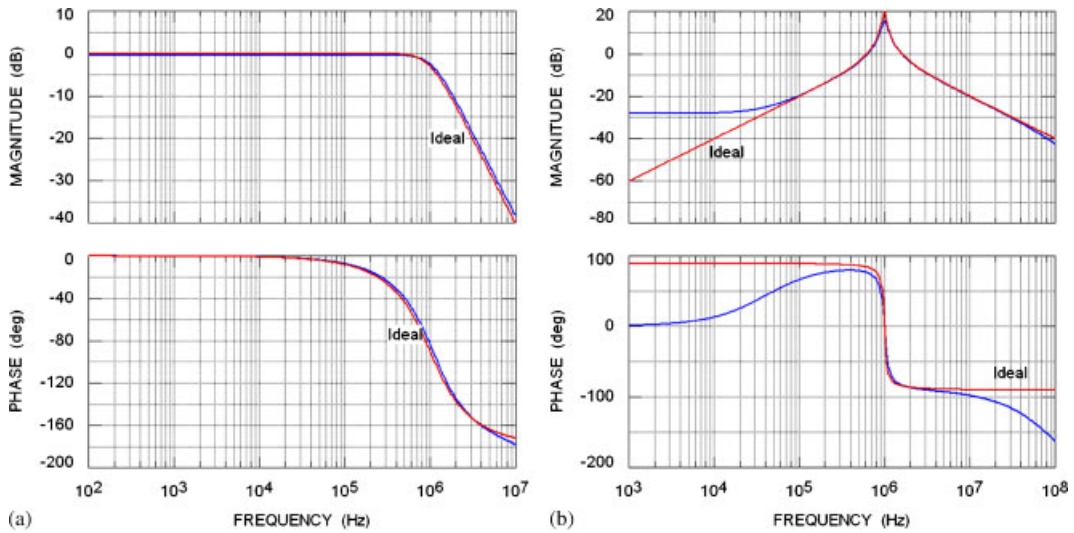

Figure 15. Magnitude and phase characteristics of the (a) low-pass response and (b) band-pass response of the circuit of Figure 4(c) at $f_0 = 1\,\text{MHz}$.

Figure 15(a) represents the magnitude and phase characteristics of the LP response together with the ideal response.

Figure 15(b) represents the magnitude and phase characteristics of the band-pass response together with the ideal response. It is seen that the simulated results agree well with the ideal responses.

The frequency response for the circuits is close to the ideal response, the power dissipation in the circuits that use the DVCC with $Z+$ only terminals is slightly lower than the circuits that use the balanced output DVCC of Figure 11(b).

5. COMPARISONS WITH CCII KHN

The current conveyor-based KHN circuit using five CCII is shown in Figure 16(a) [11]. The simulation results for a BP filter with $Q = 10$, $f_0 = 100\,\text{kHz}$ and 1 MHz using five AD844 are shown in Figures 16(b) and (c), respectively. It is seen that the deviation from the ideal response increases as the frequency increases. Other CMOS CCII circuits may give better results than the commercially available AD 844.

It is worth noting that the proposed type A-KHN circuits using the DVCC employs three DVCC, two grounded capacitors and four grounded resistors; on the other hand, the KHN circuit using CCII reported in [11] and shown in Figure 16(a) employs five CCII, two grounded capacitors and six grounded resistors.

The two circuits of Figures 9(a) and 10(a) can be realized with CCII and they are new CCII KHN circuits. The DVCC and CCII belong to the same family and it is the objective of this paper to complete the set of KHN circuits using DVCC and CCII as basic building blocks.

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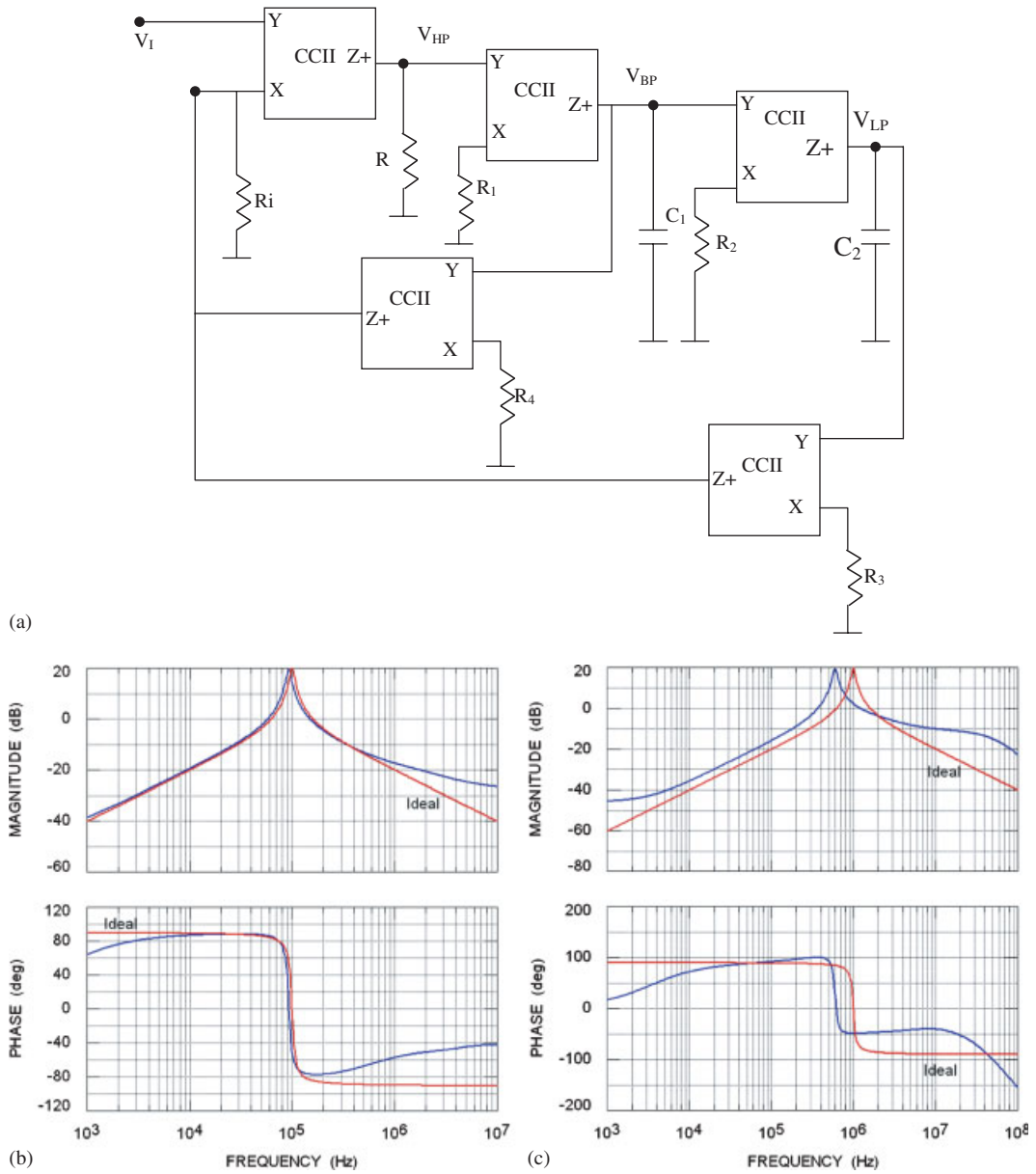

Figure 16. (a) The grounded resistor grounded capacitor KHN circuit using five CCII+ [11]. Magnitude and phase characteristics of the band-pass response of the KHN CCII circuit at (b) $f_0 = 100\,\text{kHz}$ and (c) $f_0 = 1\,\text{MHz}$.

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6. CONCLUSIONS

New high input impedance voltage mode circuits realizing the KHN and using three or four DVCC are generated from the basic KHN and the inverted KHN block diagrams. The availability of non-inverting integrators with grounded resistors and capacitors gives more degrees of freedom in designing two integrator loop filters. The circuits are classified into two types, type A employs three DVCC and type B employs four DVCC. Each type includes four classes of circuits depending on the four possible integrator polarities. Each class can be realized by several circuits as demonstrated in the paper. All the eight possible sign combinations of the output voltages polarities are obtainable from the two types; four sign combinations from each type. The eight block diagrams are included to demonstrate the difference between each class of circuits. It is worth noting that the use of CCII in KHN realization given in [11] results also in all possible sign combinations but was limited to one circuit only for each sign combinations. Spice simulation results demonstrating the practicality of the proposed filters are included. For all simulations it is seen that the simulated results agree well with the ideal responses. It should be noted that the circuits of Figures 3(a), 4(a), 7(a) and 10(a) have only $Z+$ outputs which is an advantage in avoiding current mirrors to produce $Z-$. The circuit of Figure 7(a) is the only circuit that uses DVCC with single $Z+$ output. The circuits of Figures 9(a) and 10(a) can be realized with CCII as a special case, thus this generation of the DVCC-based KHN circuits resulted in new CCII-based KHN circuits not previously known in the literature. It is hoped that this paper will open the door for the development of new MOS-C KHN filters using the DVCC. It is worth noting that other forms of MOS-C filters using operational transresitance amplifier (OTRA) have been recently introduced in the literature [20].

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