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ON THE INTRODUCTION OF NEW FLOATING CURRENT CONVEYORS

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Two new types of floating current conveyors are introduced. Each type has four ports: Y, X and two Z ports. The first type is the Floating Second Generation Current Conveyor (FCCII) and includes both CCII+ and CCII− as special cases. The second type is the Floating Inverting Second Generation Current Conveyor (FICCII) and includes both ICCII+ and ICCII− as special cases. The Nodal Admittance Matrix (NAM) stamp for the Nullator-Pathological Current Mirror is derived. Examples are given together with a CMOS circuit realizing both the FCCII and FICCII.

Keywords: Current conveyor; inverting current conveyor; floating current conveyor.

1. Introduction

Since the introduction of the Second Generation Current Conveyor (CCII),[1] it has attracted the attention of several authors.[2–7] The Inverting Second Generation Current Conveyor (ICCII) was introduced in Ref. 8 to complete the CCII family with single output.

The basic matrix equation of the CCII and ICCII is given as:

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & \pm 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix}. \tag{1}$$

In the above equation all currents are assumed to be inwards. The positive sign in the first row applies to CCII, whereas the negative sign applies to ICCII. The positive sign in the third row applies to CCII+ and ICCII+, whereas the negative sign applies to CCII− and ICCII−.

From the four types of CCII and ICCII, the only two floating types are the CCII− and ICCII− as demonstrated in Fig. 1.

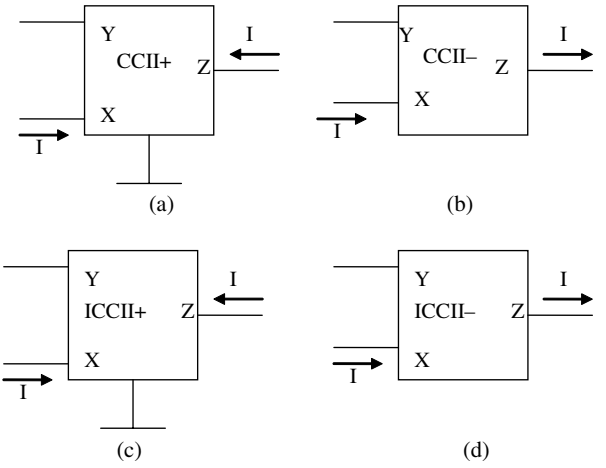

Fig. 1. The two types of CCII and the two types of ICCII.

The objective of this paper is to generalize the CCII+ and ICCII+ to two new floating four-port current conveyors. The floating CCII includes both of the CCII+ and CCII− as special cases. Also the floating ICCII includes both of the ICCII+ and ICCII− as special cases.

2. The New Floating CCII

The Floating Second Generation Current Conveyor (FCCII) is a four-port building block as shown in Fig. 2(a) and is defined by the following matrix equation:

$$\begin{bmatrix} V_X \\ I_Y \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ -2 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_{Z+} \\ V_{Z-} \end{bmatrix}. \tag{2}$$

In the above equation all currents are assumed to be inwards. It is seen that this new four-port active building block includes the CCII+ as special case with the Z-port grounded. If the two Z output terminals are connected together it realizes the CCII− as a special case.

3. The New Floating ICCII

The Floating Inverting Second Generation Current Conveyor (FICCII) is a four-port building block as shown in Fig. 2(b) and is defined by the following matrix equation:

$$\begin{bmatrix} V_X \\ I_Y \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ -2 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_{Z+} \\ V_{Z-} \end{bmatrix}. \tag{3}$$

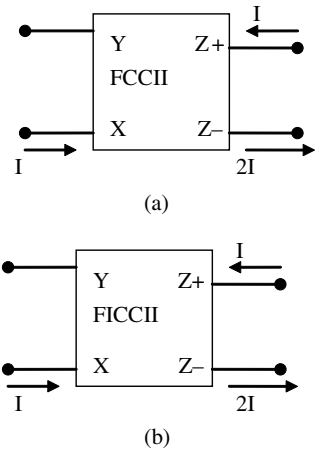

Fig. 2. Symbolic representation of the FCCII and FICCII.

In the above equation all currents are assumed to be inwards. It is seen that this new four-port active building block realizes the ICCII+ as a special case with the Z-port grounded. If the two Z output terminals are connected together it realizes the ICCII− also as special case.

4. General NAM Stamp for Nullator-CM Pair

Consider the general five terminal Nullator-Current Mirror (CM) pair shown in Fig. 3(a), which consists of a Nullator whose terminals are connected to nodes a and b and a floating pathological CM[9] whose terminals are connected to nodes d, e, and c and defined by:

$$V_a = V_b \quad \text{and} \quad I_a = I_b = 0\,, \tag{4a}$$

$$\begin{aligned} &V_{dc} \text{ and } V_{ec} \text{ are arbitrary and} \\ &I_d = I_e \text{ and are also arbitrary}\,. \end{aligned} \tag{4b}$$

Node c is the reference node for the CM. This five-terminal Nullator-CM pair can be represented using two dependent sources when their gains tend to infinity, with every dependent source describing the relation between the voltage at the nullator and the current at one port in the CM element as shown in Fig. 3(b). Since the considered synthesis framework[10] uses the admittance matrices and since the voltage-controlled current sources (VCCS) is the only dependent source that possesses an admittance matrix,[10–14] thus the Nullator-CM pair in Fig. 3(a) should be described in terms of VCCS for which the transconductance gains tend to infinity. Hence, the admittance matrix stamp for the representation of this five-terminal Nullator-CM pair shown in Fig. 3(a) can be considered as that for the VCCS-based ideal model in Fig. 3(b), with the transconductance gain of every VCCS is G_{mi} and

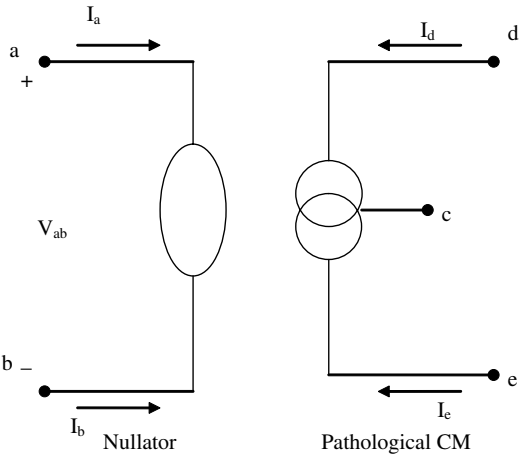

Fig. 3(a). Nullator-pathological CM pair.

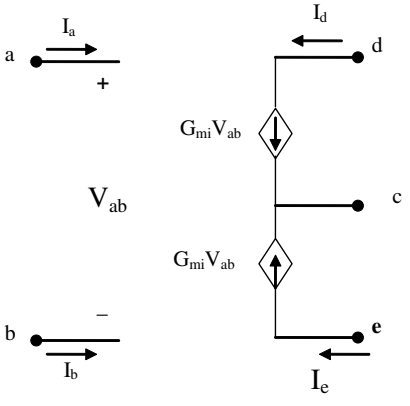

Fig. 3(b). Voltage controlled current sources ideal model of the nullator-pathological CM pair.

is taken to a limit of infinity. This VCCS-based ideal model can be entered into the NAM in the following form:

$$\begin{array}{c} \\ d \\ e \\ c \end{array} \begin{array}{c} \begin{array}{cc} a & b \end{array} \\ \begin{bmatrix} G_{mi} & -G_{mi} \\ G_{mi} & -G_{mi} \\ -2G_{mi} & 2G_{mi} \end{bmatrix} \end{array}, \tag{5}$$

where G_{mi} is taken to a limit of infinity. Then, rows d, e, and c of the NAM equation set will have the form:

$$\begin{bmatrix} I_d \\ I_e \\ I_c \end{bmatrix} = \begin{bmatrix} G_{mi} & -G_{mi} \\ G_{mi} & -G_{mi} \\ -2G_{mi} & 2G_{mi} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \end{bmatrix} + \begin{bmatrix} \text{finite terms} \\ \text{finite terms} \\ \text{finite terms} \end{bmatrix}. \tag{6}$$

It is known that in order to preserve the finiteness of an equation containing a parameter that tends to infinity, the whole equation must be divided by this parameter before taking the limit. This is provided that the limit applies to the whole equation and not to that parameter individually.[10] In order to apply this principle to the above equation corresponding to rows d, e, and c of the NAM equation set, these equations are divided by G_{mi} and limit of G_{mi} when it tends to infinity is taken for both sides of each row. Thus, rows d, e, and c are described by:

$$\begin{bmatrix} \frac{I_d}{G_{mi}} \\ \frac{I_e}{G_{mi}} \\ \frac{I_c}{G_{mi}} \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ 1 & -1 \\ -2 & 2 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \end{bmatrix} + \begin{bmatrix} \frac{\text{finite terms}}{G_{mi}} \\ \frac{\text{finite terms}}{G_{mi}} \\ \frac{\text{finite terms}}{G_{mi}} \end{bmatrix}, \tag{7}$$

where $G_{mi} \to \infty$. When the limit is taken, dependent current terms on the LHS and finite terms on the RHS will vanish as described by:

$$\begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ 1 & -1 \\ -2 & 2 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}. \tag{8}$$

The three rows in the NAM equation set corresponding to the CM nodes yield the same relation between independent voltage variables:

$$V_a - V_b = 0 \to V_a = V_b\,. \tag{9}$$

Since the Nullator-CM pair description in Eq. (7) has no matrix entries for rows a and b then:

$$I_a = I_b = 0\,. \tag{10}$$

The similarity between the coefficients of rows d and e in Eq. (7) imposes the constraint that the current entering (leaving) the CM at node d is equal to that entering (leaving) it at node e, and the coefficients of row c indicates that both currents are leaving (entering) the CM at node c. Equation (7) indicates KCL at node c for the currents flowing between each of nodes d and e and node c within the CM; however, the values of the currents at the terminals of the CM are unconstrained. Since the column corresponding to the nodes d, e, or c does not exist in the floating mirror description of Eq. (8), therefore there are no constraints on the terminal voltages of the CM. Thus, the NAM description in Eq. (7) with $G_{mi} \to \infty$ imposes finite relationships between the nodal voltages and currents which correctly describe a Nullator-CM pair shown in Fig. 3(b).

As explained in Ref. 10, nullor element can be represented in the NAM using infinity-variables. In this notation the variables in the NAM that are taken to an infinite limit are written as ∞_i, where ∞_i indicates that the limit is taken to infinity and i refers to the active element the nullor is representing.

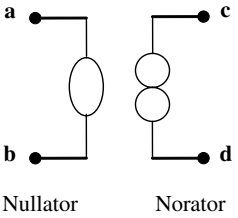

Fig. 4. Two-port nullor represented by nullator and norator.

For the nullor in Fig. 4, it has been deduced in Ref. 10 that this nullor description in the NAM using infinity-variables takes the form:

$$\begin{array}{c} \\ c \\ d \end{array} \begin{array}{c} \begin{array}{cc} a & b \end{array} \\ \begin{bmatrix} \infty_i & -\infty_i \\ -\infty_i & \infty_i \end{bmatrix} \end{array}. \tag{11}$$

On applying this infinity-variables notation to the nullator-CM pair, the nullator CM description in Eq. (6) becomes:

$$\begin{array}{c} \\ d \\ e \\ c \end{array} \begin{array}{c} \begin{array}{cc} a & b \end{array} \\ \begin{bmatrix} \infty_i & -\infty_i \\ \infty_i & -\infty_i \\ -2\infty_i & 2\infty_i \end{bmatrix} \end{array}. \tag{12}$$

From the set of infinity-variables describing the floating nullor pair in Eq. (11), the presence of a nullator between the two nodes a and b causes the infinity-variables in the two NAM columns corresponding to nodes a and b to have equal coefficients with opposite signs and, similarly, the presence of a norator between the two nodes c and d causes the infinity-variables in the two NAM rows corresponding to nodes c and d to have equal coefficients with opposite signs. The same approach can be adopted to describe the effect of nullator-CM pair on the relation between infinity-variables occupying the NAM rows and columns corresponding to the nodes at which the terminals of the nullator and CM are connected. The set of infinity-variables describing the Nullator CM pair in Eq. (12) indicates that the nullator whose two terminals are connected between each of the nodes a and b causes the infinity-variables in the two columns a and b to be equal and having opposite signs. On the other hand, the floating current mirror whose two ports are connected between each of the nodes d and e and the floating reference node c causes the infinity-variables in the two rows d and e to be equal and having the same signs while the coefficients of the infinity-variables in row c are double those in each of rows d and e and having opposite signs.

5. NAM Stamp for the FCCII and FICCII

The FCCII shown in Fig. 5 is a special case from the nullator-CM pair shown in Fig. 3(a) with X as a common terminal between the nullator and the CM.

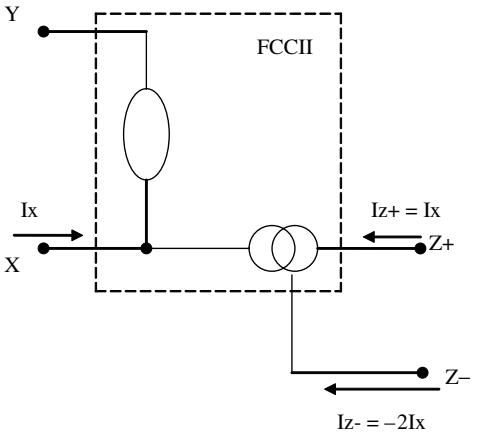

Fig. 5. Nullator-CM with a common terminal realizing a FCCII.

The NAM stamp of the floating CCII is described as:

$$\begin{array}{c} \\ X \\ Z+ \\ Z- \end{array} \begin{array}{c} \begin{array}{cc} X & Y \end{array} \\ \begin{bmatrix} \infty_i & -\infty_i \\ \infty_i & -\infty_i \\ -2\infty_i & 2\infty_i \end{bmatrix} \end{array}. \tag{13}$$

The FICCII shown in Fig. 6 is a special case from the Voltage Mirror (VM)-CM pair with X as a common terminal between the VM and CM.[12]

Similarly the NAM stamp of the FICCII can be obtained as:

$$\begin{array}{c} \\ X \\ Z+ \\ Z- \end{array} \begin{array}{c} \begin{array}{cc} X & Y \end{array} \\ \begin{bmatrix} \infty_i & \infty_i \\ \infty_i & \infty_i \\ -2\infty_i & -2\infty_i \end{bmatrix} \end{array}. \tag{14}$$

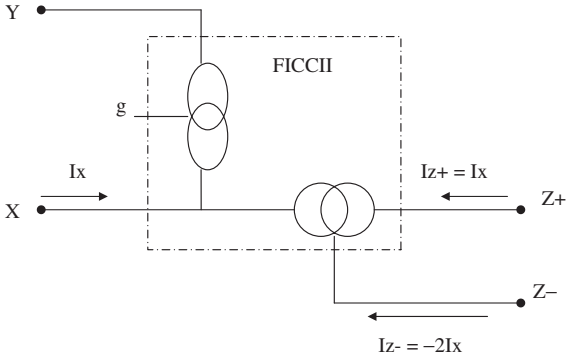

Fig. 6. VM-CM with a common terminal realizing a FICCII.

6. CMOS Realization of the FCCII and FICCII

Although the main paper objective is to introduce new FCCII and FICCII, it may be suitable to show a practical CMOS realization of both of the FCCII and FICCII.

The CMOS circuit realizing both the FCCII and FICCII as well is obtained directly from the well known DVCC[5, 15] by doubling the aspect ratio of M_{16} and M_{18}.

The FCCII-CMOS circuit is shown in Fig. 7(a) and the transistor aspect ratios are given in Table 1 based on the $0.5\,\mu$m CMOS model from MOSIS. The supply voltages used are $\pm 1.5\,$V and $V_{B1} = -0.52\,$V and $V_{B2} = 0.33\,$V.

The FCCII is obtained by using Y_1 as the Y input and grounding Y_2, on the other hand the IFCCII is obtained by using Y_2 as the Y input and grounding Y_1.

The Spice simulation transient analysis of the FCCII with a pulse input waveform of magnitude $\pm 0.5\,$V applied the Y input is shown in Figs. 7(b) and 7(c) demonstrating the circuit stability and showing that the magnitude of I_{Z-} is the sum of I_{Z+} and I_X. Simulation is carried out with each of ports X, $Z+$ and $Z-$ terminated by a $10\,$kΩ resistor.

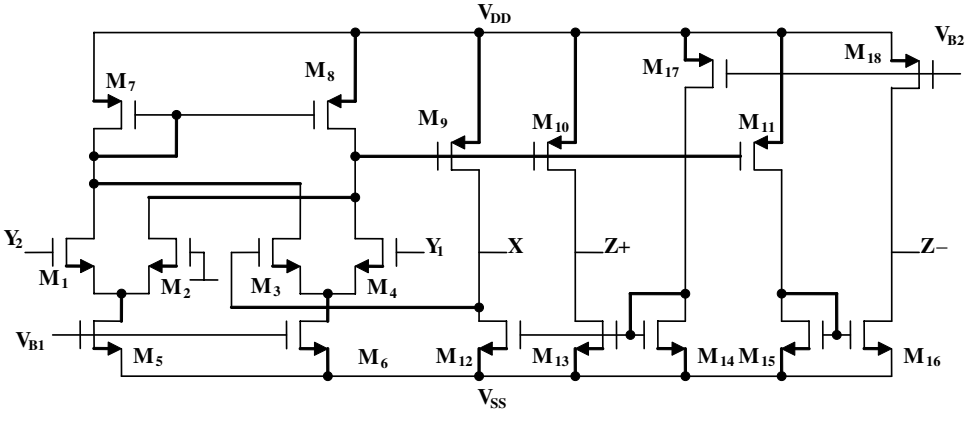

Fig. 7(a). CMOS realization of the FCCII and the FICCII.

Table 1. Transistor aspect ratios of the FCCII.

	$W(\mu\text{m})/L(\mu\text{m})$
NMOS transistors	
M_1, M_2, M_3, M_4	8/1
M_5, M_6	8/1
$M_{12}, M_{13}, M_{14}, M_{15}$	20/2.5
M_{16}	40/2.5
PMOS transistors	
M_7 and M_8	10/1
$M_9, M_{10}, M_{11}, M_{17}$	40/2
M_{18}	80/2

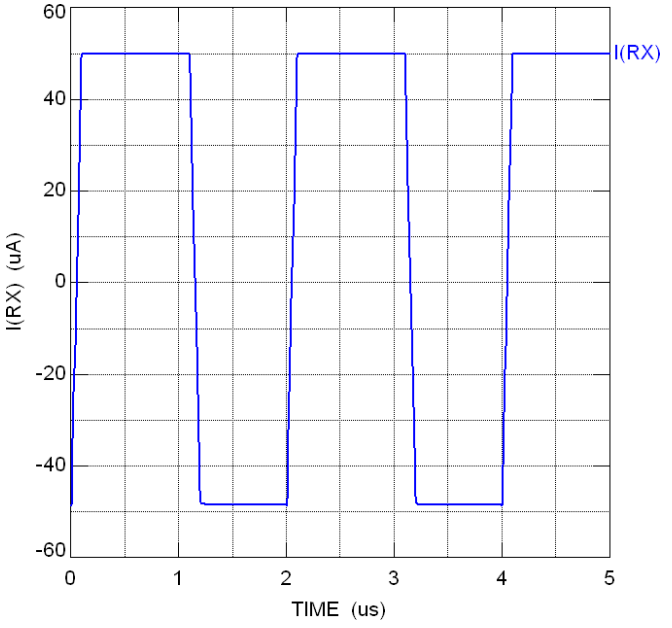

Fig. 7(b). Spice simulated transient analysis showing I_X of the FCCII.

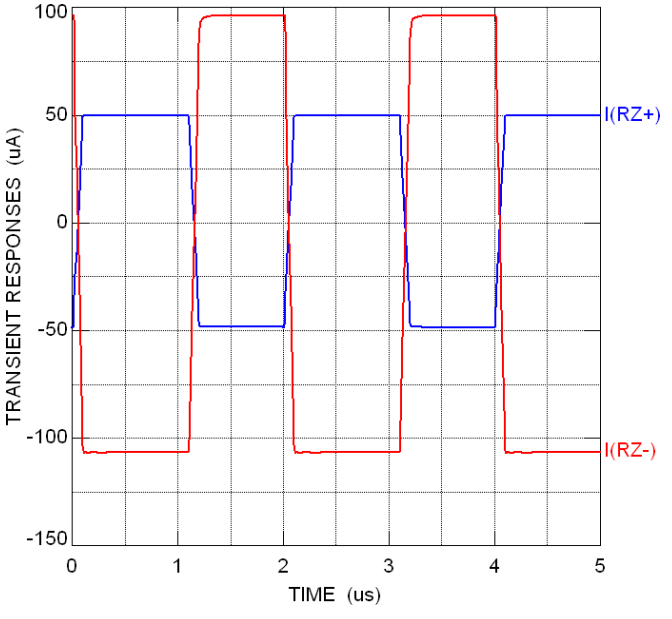

Fig. 7(c). Spice simulated transient analysis showing I_{Z+} and I_{Z-} of the FCCII.

7. Example

As an application of the new FCCII a voltage controlled voltage source (VCVS) using equal resistors is shown Fig. 8(a). It has two outputs: one of them V_{O2} provides double the output V_{O1} and with opposite phase. Due to the floating nature of the FCCII the current in the ground terminal is zero.

A similar VCVS using FICCII can also be realized and provides two outputs.

Figure 8(b) represents the Spice simulated magnitude and phase responses of the circuit of Fig. 8(a) with $R = 1\,\text{k}\Omega$ and using an input sinusoidal voltage of 1 V.

Figure 8(c) represents the simulated currents I_{Z+} and I_{Z-} of the circuit of Fig. 8(a). It should be noted that the current I_X coincides with I_{Z+} and is not shown to make a clear figure.

It is seen that the simulation results are in good agreement with the expected ones and the current flowing in ground is very close to zero as expected.

8. Conclusions

Two new types of floating current conveyors are introduced. Each type has four ports Y, X and two Z ports. The first type is CCII and includes both CCII+ and CCII− as special cases. The second type is ICCII and includes both ICCII+ and ICCII− as special cases.

CMOS circuit realizing both of the FCCII and FICCII is included with simulation results. Example is given of VCVS with two opposite polarity outputs and

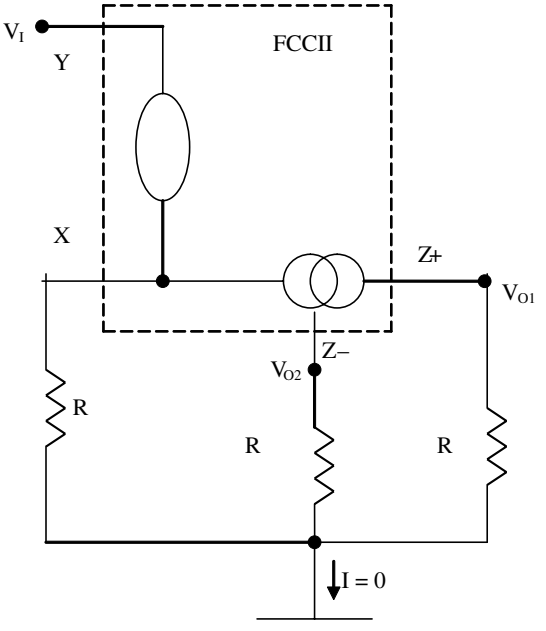

Fig. 8(a). VCVS with two outputs using FCCII.

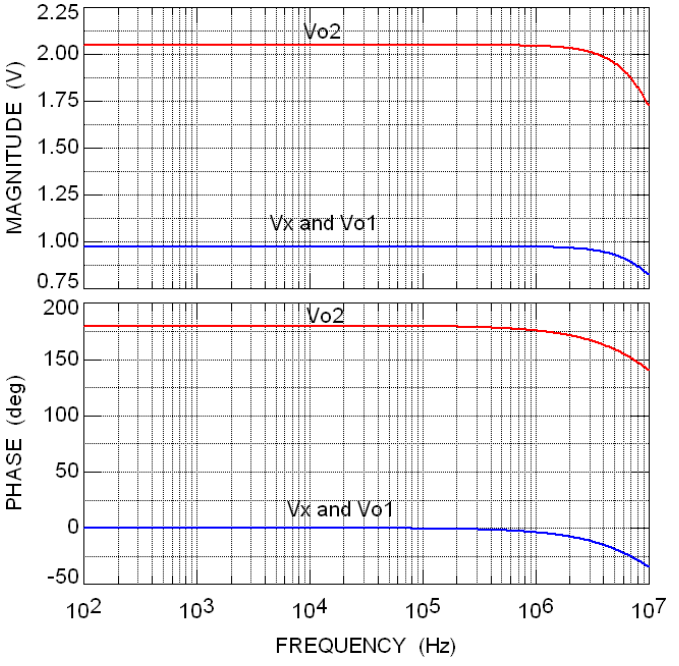

Fig. 8(b). Spice simulated magnitude and phase responses of V_X and the two outputs of the VCVS using FCCII.

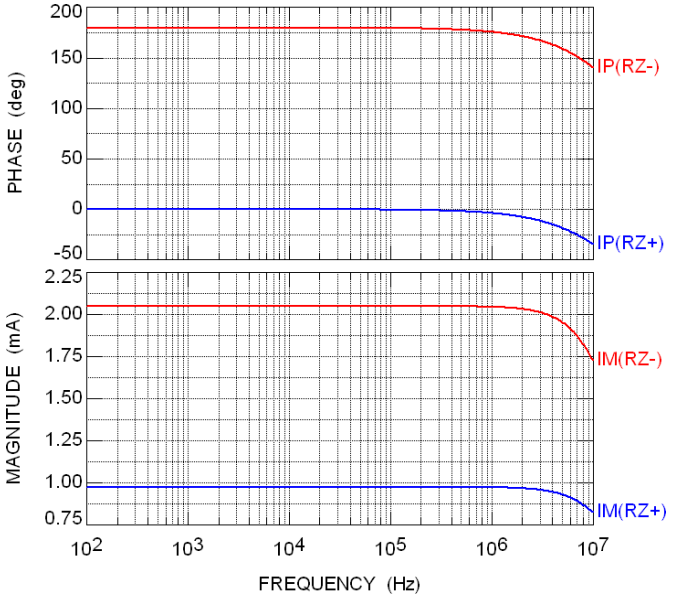

Fig. 8(c). Spice simulated magnitude and phase responses of the two output currents of the VCVS using FCCII.

gain at one output is double the gain at the other output which cannot be achieved with single CCII+ or CCII−.

The NAM stamp for the Nullor-Pathological Current Mirror is derived in details.

Acknowledgment

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