inverter based on two AlGaN-GaN HFETs with threshold voltages of –0.5V (T1) and –1.0V (T2). The epilayer design of the T2 HFET was similar to that of T1. However, to increase the threshold voltage of transistor T2, the AlGaN barrier thickness was increased to 20nm. The inverter also used a GaN Schottky barrier diode connected in series with the HFET gate for level shifting. At room temperature, the measured inverter characteristics exhibited a large gain (up to 180) and had a noise margin of ~0.5V. We also tested the performance of the inverter (without the Schottky diode) at elevated temperatures (see Fig. 3). The estimated temperature coefficient of the switching voltage of the device was ~3.5mV/°C up to 90°C, which is about three times higher than in a similar silicon device [5].

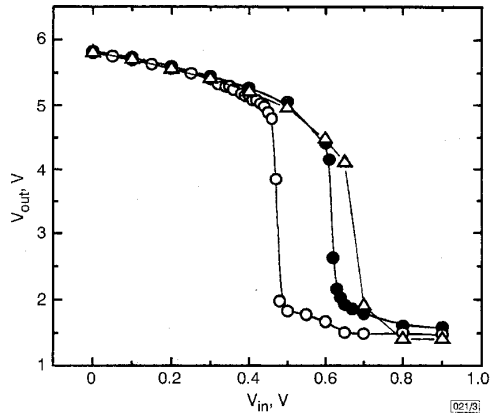


**Fig. 3** *Characteristics of inverter*

Based on two AlGaN-GaN HFETs and without level lifting Schottky diode at three different temperatures
Estimated voltage switching coefficient is 3.5mV/°C
○ $T$ = 17.5°C
● $T$ = 50°C
△ $T$ = 75°C

The measured device characteristics and the inverter transfer curves are in good agreement with the simulated dependencies that were obtained using the AIM-SPICE AlGaN-GaN HFET model [6]. Using the calculated temperature coefficients of the electron mobility at elevated temperatures and the previously measured temperature coefficient of the threshold voltage, we predict that such an inverter should operate up to ~230°C. A much higher operating temperature and a larger noise margin can be obtained using a switching transistor with a more positive threshold voltage and with an optimised transistor load. Both the measured data and simulated results clearly demonstrate that GaN-based digital circuits are possible.

In conclusion, we have fabricated a low-threshold voltage AlGaN-GaN HFET and demonstrated the first GaN-based digital circuit. The HFET devices with ultra-thin $Al_{0.25}G_{0.75}N$ barrier demonstrated very low leakage currents and high electric breakdown fields. The AlGaN-GaN HFET-based inverter exhibited a positive switching voltage coefficient of 3.5mV/K and had a stable performance at elevated temperatures up to 90°C. The experimental data and simulation results indicate that further improvement in the device characteristics could make GaN-based devices suitable for high temperature digital applications.

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## Wideband CMOS current conveyor

A.M. Ismail and A.M. Soliman

A CMOS second generation current conveyor consisting of two matched differential pairs and based on the first generation current conveyor is presented. PSPICE simulations have shown that its performance is quite satisfactory for wideband current-mode signal processing.

*Introduction:* The second-generation current conveyor (CCII) is the most versatile building block in current mode signal processing [1]. To exploit wideband and wide dynamic range capabilities under low power operation of current-mode signal processing, a CCII based on the translinear loop has been proposed [2 – 4]. These translinear CMOS circuits exhibit an excellent current following behaviour from port X to port Z over a wide bandwidth but the voltage following property from port Y to port X is poor and the offset voltage is rather high. Other simple CMOS realisations of the CCII have been introduced [5 – 12]. In this Letter, a novel CMOS realisation of the CCII based on the long tail differential pair is introduced.

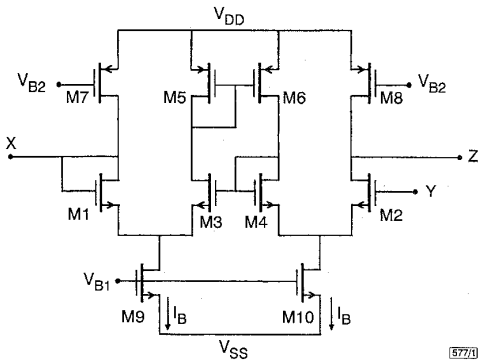


**Fig. 1** *Circuit configuration of proposed CCII*

*Circuit description:* The circuit configuration of the proposed CCII is shown in Fig. 1. It consists mainly of two differential pairs (M1-M3 and M2-M4). It can be easily noted that transistors M3-M6 form the first generation current conveyor introduced in [1]. The action of the proposed CCII can be described as follows: Assuming that the two differential pairs M1, M3 and M2, M4 are perfectly matched, the CCI formed by M3-M6 conveys the voltage from the source of transistor M4 to the source of transistor M3 and the current from transistor M5 to transistor M6, thus the voltage $v_Y$ applied to the gate of M2 does not affect the current flowing in M4 since the latter follows the current flowing in M3,

and, since the sources of transistors M1 and M2 have the same voltage (due to the action of the CCI) and carry the same current (since the currents in M3 and M4 are equal), the voltage $v_Y$ is conveyed to node X successfully. The current coming from X can be reproduced in Z without the need for current mirrors as shown in Fig. 1.

The voltage transfer function is given by

$$\frac{v_x}{v_y} = \frac{1}{1 + \frac{1}{g_m^2 r_o R_L}} \quad (1)$$

where $g_m$ and $r_o$ are the transconductance of the differential pair and the resistance seen at the drain of transistor M4 (before connecting it to its gate terminal), respectively. $R_L$ is the load resistance connected at node X ($R_L$ is replaced by $R_X$ when no load is connected to the node X).

The resistance $R_X$ at node X is given by

$$R_X = \frac{r_o}{1 + g_m^2 r_o^2} \quad (2)$$

With the simple configuration shown in Fig. 1, it follows therefore that $R_X$ is very small and $v_X$ follows exactly $v_Y$.

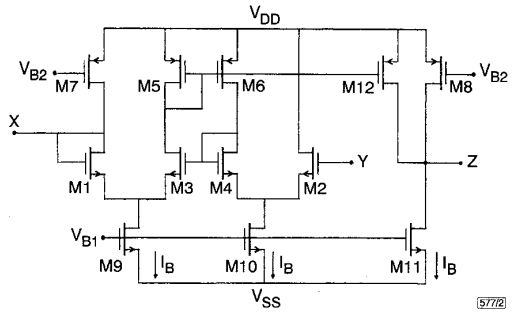


**Fig. 2** *Modified circuit configuration of CCII*

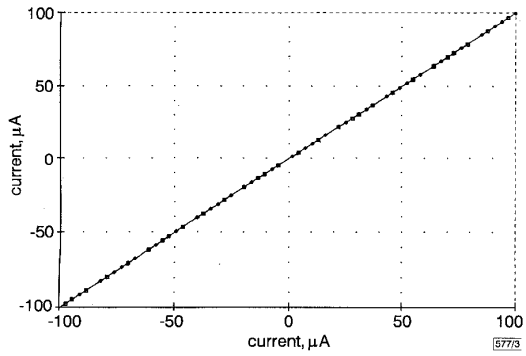


**Fig. 3** *Current transfer characteristics from node X to node Z*

□ -I (V3)
◇ I (I5)

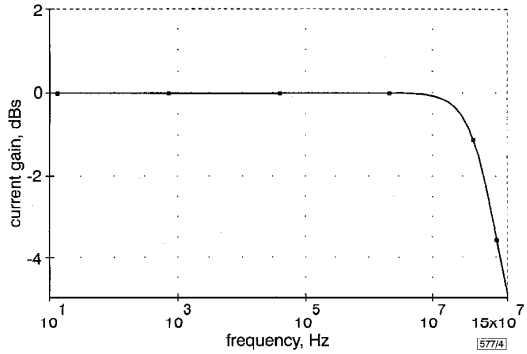


**Fig. 4** *Current gain in decibels of CCII circuit against frequency*

It is noted that in the configuration of Fig. 1, the value of the voltage $v_Z$ at the node Z is restricted to be higher than ($v_Y$ + $v_{DS2,sat}$) for proper operation. To overcome this problem, the circuit is modified as shown in Fig. 2.The voltage $v_Z$ can then take values less than $v_Y$ which is necessary to design voltage amplifiers with gain less than unity.

The above analysis of the circuit operation confirms that the circuits shown in Figs. 1 and 2 are each CCII+ and their input-output relation can be described in terms of the ideal 3 × 3 matrix representation [1]. A CCII version can be easily realised by inverting the direction of $i_Z$ using current nurrors.

**Table 1**: W/L of transistors of CCII shown in Fig. 2

| Transistor | Aspect ratio |
|---|---|
| M1–M4 | 35/1.4 |
| M5, M6, M12 | 49/3.5 |
| M7, M8 | 49/3.5 |
| M9, M10, M11 | 35/2.8 |

*PSPICE simulations:* Performances of the CCII shown in Fig. 2 are simulated using PSPICE. Transistor aspect ratios in Table 1 and 0.7μm CMOS process are used. Supply voltages are $V_{DD} = -V_{SS} = 2.5$V and $I_B$ is set to 100μA.

It is found that the resistance $R_X$ is 8 Ω. The offset voltage at node X when Y is grounded is < 0.5mV. Fig. 3 shows the current transfer characteristics from node X to node Z. An excellent current-following action can be seen over the wide current range. Fig. 4 illustrates the current gain of the circuit against frequency. The simulations show that the circuit is also an excellent current follower that can be widely used in current-mode signal processing.


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