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GENERATION OF OSCILLATORS BASED ON GROUNDED CAPACITOR CURRENT CONVEYORS WITH MINIMUM PASSIVE COMPONENTS

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In this paper, eight new Frequency Dependent Negative Resistance (FDNR) circuits using two current conveyors or inverting current conveyors or a combination of the two types are introduced. The proposed circuits are canonic and they use two grounded capacitors and one floating resistor. The generation of grounded capacitor minimum passive component oscillators from the FDNR circuits is also considered. It is found that two of the recently reported attractive oscillators are among the family of the generated oscillator circuits. Additional six new oscillator circuits based on the FDNR circuits are introduced in this paper. Spice simulation results using technology: SCN 05 feature size 0.5 μm, MOSIS Vendor: AGILENT to demonstrate the practicality of the proposed oscillators are included.

Keywords: Oscillators; current conveyors; inverting current conveyors.

1. Introduction

One of the early and important applications of the Second Generation Current Conveyor (CCII) is the grounded capacitor circuit shown in Fig. 1(a)[1] which realizes a Frequency Dependent Negative Resistor (FDNR)[2] in parallel with a capacitor. This FDNR-C circuit has been used in the generation of several filter circuits using CCII.[3] This circuit is equivalent to the well known single Operational Amplifier (Op Amp) circuit reported in Ref. 4, which uses two floating capacitors to realize the FDNR-C parallel combination. In integrated circuits fabrication, it is easier to obtain grounded capacitors than floating ones.[5] The grounded capacitors can absorb parasitic capacitances and need smaller chip area than the floating ones.[6] Besides the advantage of using grounded capacitors, the use of the CCII[7] instead of the Op Amp provides many other advantages including higher frequency range of operation thus overcoming the finite gain band-width limitations of the Op Amp circuits.[8]

Several CCII-based oscillators have been reported in the literature.[9–14]

The oscillators reported in Refs. 10 and 11 are based on the application of a single CCII+ in realizing an ideal grounded inductor or an ideal FDNR respectively. The oscillator reported in Ref. 12 has the advantage of using grounded capacitors but it is not canonic as it employs three capacitors.

A Wien type oscillator using the CCII has been introduced in Ref. 13 and is generated from the conventional Wien oscillator using the nullor concept. The oscillator given in Ref. 13 employs the CCII as a negative impedance converter (NIC). Other Wien type oscillators using CCII and based on replacing the voltage controlled voltage source (VCVS) in the classical Wien oscillator by a transconductance circuit were given in Ref. 14, these oscillators, however, employ floating capacitors.

The Inverting Second Generation Current Conveyor (ICCII) was introduced in Ref. 15 to complete the single output CCII family. The ICCII are universal building blocks[16] and have applications in filter realizations as demonstrated in Ref. 17.

In this paper, eight new grounded capacitor ideal FDNR circuits using two CCII or two ICCII, or a combination of CCII and ICCII are introduced. The proposed FDNR circuits are used as basic building blocks in the generation of two of the recently reported grounded capacitor oscillators as well as six more new oscillators. Spice simulation results are included to support the theoretical analysis.

2. Grounded Capacitor FDNR Circuits

The first grounded capacitor minimal component FDNR-C circuit was introduced in the literature in Ref. 1 and is shown in Fig. 1(a). The circuit uses a single CCII− and it has input admittance given by:

$$Y_i = sC_1 + sC_2 + s^2C_1C_2R_2\,. \tag{1}$$

Application of this circuit in the generation of grounded capacitor low-pass filters from passive RLC filters was reported in Ref. 3.

Equation (1) can also be realized using ICCII+ as shown in Fig. 1(b)[16] where the ICCII+[15] is defined by the following matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & +1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}. \tag{2}$$

The two circuits of Fig. 1 are equivalent in realizing grounded admittance. It should be noted that although the circuit of Fig. 1(a) is valid for floating admittance realization, the circuit of Fig. 1(b) does not realize floating admittance.

If a CCII+ is used in place of the CCII− in the circuit of Fig. 1(a) the circuit realizes Eq. (1) with a negative sign.[18] The same is true if an ICCII− is used in place of the CCII− in Fig. 1(a).

The first modification to the circuit of Fig. 1(a) by adding another CCII+ acting as a Negative Impedance Converter (NIC) as shown in Fig. 1(c) was given in Ref. 18.

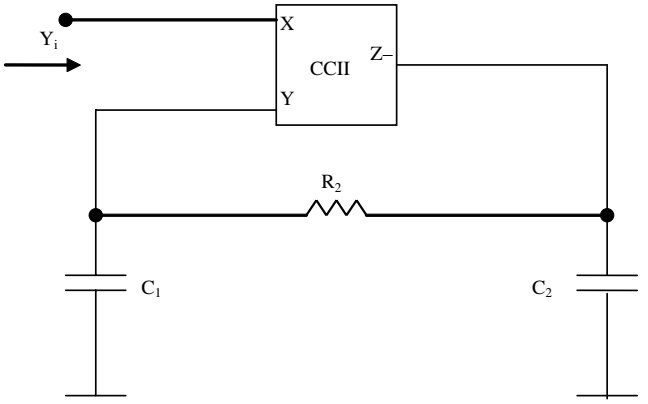

Fig. 1(a). Grounded capacitor FDNR-C circuit using CCII−.[1]

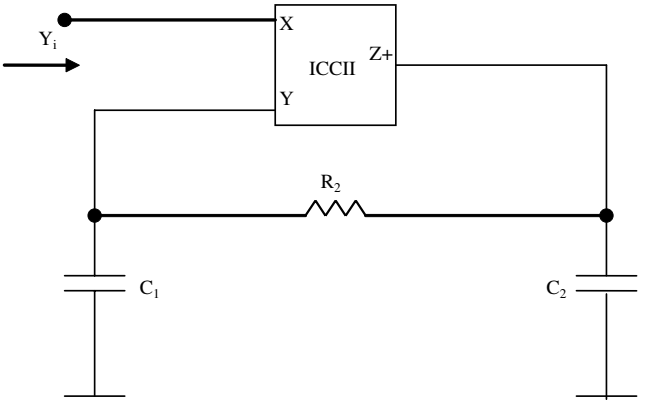

Fig. 1(b). Grounded capacitor FDNR-C circuit using ICCII+.[16]

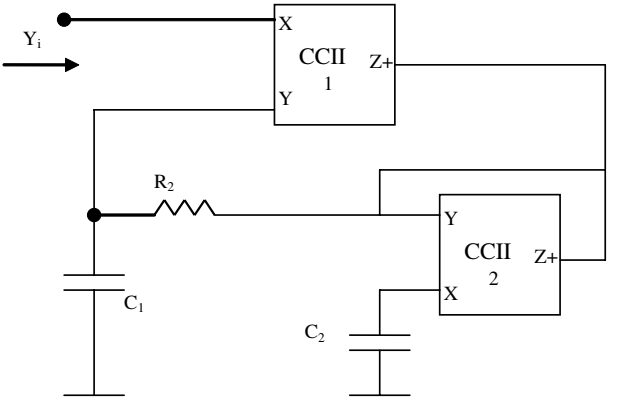

Fig. 1(c). Grounded capacitor ideal FDNR circuit using two-CCIIs+.[18]

The circuit uses two of CCII+ and it has input admittance given by:

$$Y_i = -sC_1 + sC_2 + s^2 C_1 C_2 R_2 \,. \tag{3}$$

The above equation indicates that if the two capacitors C_1 and C_2 are equal, the circuit realizes an ideal FDNR of magnitude D equal to $C_1 C_2 R_2$.

The main disadvantage of the circuit of Fig. 1(c) is that the capacitor C_2 is connected to the X terminal of the second CCII+, which will affect the circuit operation at high frequencies due to the parasitic resistance R_x of the second CCII+. In this case, the effective impedance connected to port X of the second CCII+ that has to be considered as R_x in series with the capacitor C_2 instead of just the capacitor C_2 in the ideal case. Therefore at high frequencies, the effective impedance connected to port X deviates from its ideal value and this tends to modify the ideal behavior of the circuit.[19]

2.1. *New ideal FDNR circuits*

Eight new FDNR circuits that belong to two generalized configurations are introduced in this paper. The proposed configurations avoid a capacitor connection to the X terminal of the CCII or the ICCII, thus having better performance at high frequencies as will be discussed below.

Figure 2(a) represents the first generalized configuration realizing four different ideal FDNR circuits. Each FDNR circuit uses two grounded capacitors, one resistor and two conveyors (CCII or ICCII). The type of each of the two conveyors is given in Table 1.

Each of the four FDNR circuits that belong to this first configuration has an input admittance given by Eq. (3) as illustrated in Table 1.

Figure 2(b) represents the second generalized configuration realizing four alternative ideal FDNR circuits.

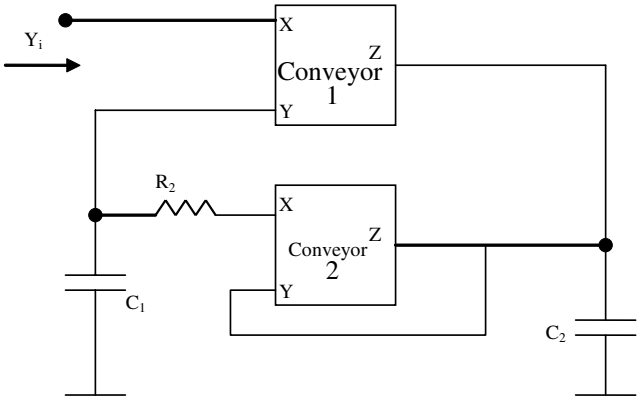

Fig. 2(a). The generalized configuration-I realizing ideal FDNR.

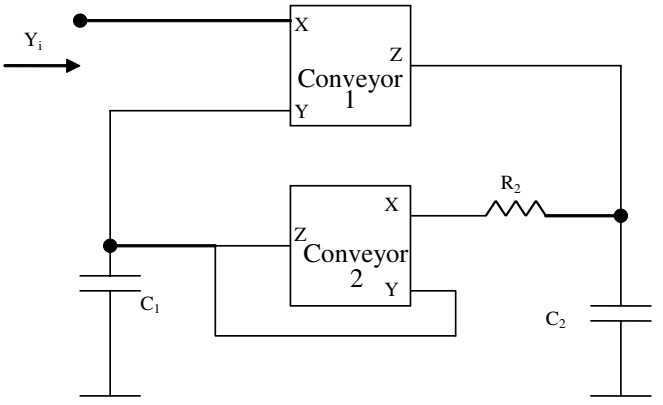

Fig. 2(b). The generalized configuration-II realizing ideal FDNR.

Table 1. The types of the two conveyors in the eight ideal FDNR circuits.

FDNR circuit	Configuration	Conveyor 1	Conveyor 2	Y_i equation	Adjoint circuit
1	I-Fig. 2(a)	CCII−	CCII+	3	7
2	I-Fig. 2(a)	ICCII−	ICCII−	3	5
3	I-Fig. 2(a)	CCII+	ICCII−	3	8
4	I-Fig. 2(a)	ICCII+	CCII+	3	6
5	II-Fig. 2(b)	CCII+	CCII+	4	2
6	II-Fig. 2(b)	ICCII+	ICCII−	4	4
7	II-Fig. 2(b)	CCII−	ICCII−	4	1
8	II-Fig. 2(b)	ICCII−	CCII+	4	3

Each FDNR circuit uses two grounded capacitors, one resistor and two conveyors (CCII or ICCII). The type of each of the two conveyors is given in Table 1. Each of the four FDNR circuits that belong to this second configuration has an input admittance given by:

$$Y_i = sC_1 - sC_2 + s^2 C_1 C_2 R_2 \,. \tag{4}$$

The above equation is different from Eq. (3) in the two capacitor signs. If the two capacitors C_1 and C_2 are equal, the circuit realizes an ideal FDNR of magnitude D equal to $C_1 C_2 R_2$.

All of the eight new ideal FDNR circuits illustrated in Table 1 are based on the original circuit of Fig. 1(a) used with any of the two types of CCII (CCII+, CCII−) or the two types of ICCII (ICCII+, ICCII−) and using an additional CCII+ or ICCII− employed as an NIC and inserted in the branch of the resistor R_2.

From the eight FDNR circuits it is seen that circuit 1 uses one CCII− and one CCII+ and circuit 5 uses two CCII+. That is, only two ideal FDNR circuits are realizable using only CCIIs. Another two circuits are realizable using only two ICCIIs, namely circuits 2 and 6. The other FDNR circuits employ one CCII and one ICCII with the proper Z polarity as illustrated in Table 1. This provides an

example of the importance of the ICCII in completing the CCII family and providing an increase in the number of FDNR circuits from two with CCIIs only, to eight with all the four family members of CCII and ICCII.

It is worth noting that the four FDNR circuits that belong to configuration-I are related to the four FDNR circuits that belong to configuration-II by the adjoint transformation,[20] as mentioned in the right column of Table 1. As an example applying the adjoint network theorem to the FDNR circuit 1 results in the FDNR circuit 7 after inter changing C_1 and C_2.

Before considering the FDNR based oscillators, the CCII Wien oscillator based on the use of CCII as an NIC will be reviewed.

3. The Grounded Capacitors NIC Oscillators

Figure 3(a) represents the grounded capacitor minimum component oscillator which is based on the current conveyor version of the Wien bridge oscillator.[13]

Figure 3(b) represents a new ICCII− Wien oscillator circuit. The advantage of both circuits is that they are directly compensated for the parasitic resistance R_x and the stray capacitance C_Z by subtracting their values from R_2 and C_2, respectively.

The state equation of the circuit of Fig. 3(b) in matrix form is given by:

$$\begin{bmatrix} \dfrac{dv_1}{dt} \\ \dfrac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} -\dfrac{1}{C_1R_2} & -\dfrac{1}{C_1R_2} \\ \dfrac{1}{C_2R_2} & \dfrac{1}{C_2R_2} - \dfrac{1}{C_2R_1} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \tag{5}$$

The condition of oscillation and the radian frequency of oscillation are given by:

$$\frac{C_2}{C_1} + \frac{R_2}{R_1} = 1\,, \tag{6a}$$

$$\omega_0 = \frac{1}{\sqrt{C_1C_2R_1R_2}}\,. \tag{6b}$$

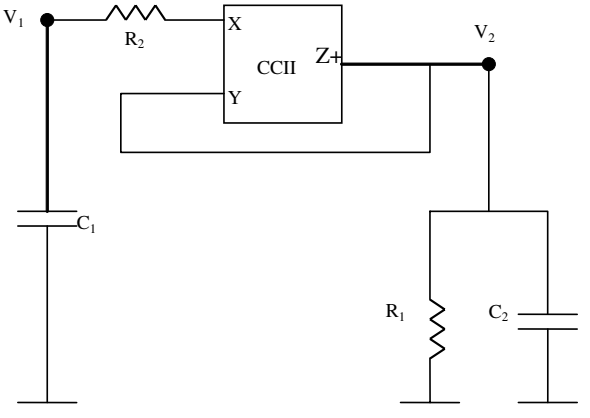

Fig. 3(a). Grounded-C minimum component oscillator reported in Ref. 13.

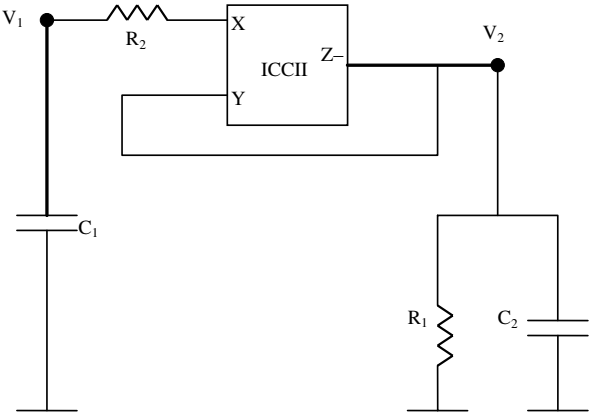

Fig. 3(b). Grounded-C minimum component oscillator using ICCII−.

The disadvantage of this oscillator circuit is that there is no independent control on the condition of oscillation or on the frequency of oscillation.

4. The Grounded Capacitors FDNR Oscillators

Two CCII attractive oscillators have been introduced earlier in the literature in Refs. 21 and 22 without any indication to a generation method. In fact the oscillator given in Ref. 21 is obtained as a modification to the two CCII+ oscillators originally introduced in Ref. 22.

Here it is shown that these two oscillators are generated from the FDNR circuits numbers 1 and 5 in Table 1, respectively, by shunting the grounded resistor R_1 to the input FDNR port.

For the oscillator obtained from the FDNR circuit number 1 in Table 1 and reported in Ref. 21, the state equation in matrix form is given by:

$$\begin{bmatrix} \dfrac{dv_1}{dt} \\ \dfrac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} -\dfrac{1}{C_1R_2} & \dfrac{1}{C_1R_2} \\ -\dfrac{1}{C_2R_2} - \dfrac{1}{C_2R_1} & \dfrac{1}{C_2R_2} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \tag{7}$$

For the new oscillator obtained from the FDNR circuit number 2 in Table 1, the state equation in matrix form is given by:

$$\begin{bmatrix} \dfrac{dv_1}{dt} \\ \dfrac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} -\dfrac{1}{C_1R_2} & -\dfrac{1}{C_1R_2} \\ \dfrac{1}{C_2R_2} + \dfrac{1}{C_2R_1} & \dfrac{1}{C_2R_2} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \tag{8}$$

For the oscillator obtained from the FDNR circuit number 5 in Table 1 and reported in Ref. 22, the state equation in matrix form is given by:

$$\begin{bmatrix} \dfrac{dv_1}{dt} \\ \dfrac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} \dfrac{1}{C_1R_2} & -\dfrac{1}{C_1R_2} \\ \dfrac{1}{C_2R_2}+\dfrac{1}{C_2R_1} & -\dfrac{1}{C_2R_2} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \tag{9}$$

For the new oscillator obtained from the FDNR circuit number 6 in Table 1, the state equation in matrix form is given by:

$$\begin{bmatrix} \dfrac{dv_1}{dt} \\ \dfrac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} \dfrac{1}{C_1R_2} & \dfrac{1}{C_1R_2} \\ -\dfrac{1}{C_2R_2}-\dfrac{1}{C_2R_1} & -\dfrac{1}{C_2R_2} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \tag{10}$$

All of the eight oscillators described by the four state matrix Eqs. (7)–(10) have the same condition of oscillation and the same radian frequency of oscillation that are given by:

$$C_1 = C_2\,, \tag{11a}$$

$$\omega_0 = \frac{1}{\sqrt{C_1C_2R_1R_2}}\,. \tag{11b}$$

The grounded resistor R_1 controls the frequency of oscillation without affecting the condition of oscillation which is controlled by any of the two grounded capacitors.

It is worth noting all of the eight oscillators reported in Table 2 and belong to the generalized configurations shown in Figs. 4(a) and 4(b) are easily compensated for the parasitic resistance R_{x_1} and R_{x_2} by subtracting their values from R_1 and R_2, respectively.

The four oscillators that belong to configuration-I shown in Fig. 4(a) can absorb the parasitic capacitances C_{z_1} and C_{z_2} by subtracting their sum value $(C_{z_1}+C_{z_2})$ from C_2.

The four oscillators that belong to configuration-II shown in Fig. 4(b) can absorb the parasitic capacitances C_{z_1} and C_{z_2} by subtracting their values from C_2 and C_1, respectively.

Table 2. Eight minimal component grounded C oscillator circuits.

Oscillator circuit	Configuration	Conveyor 1	Conveyor 2	State matrix equation	Reference
1	I-Fig. 4(a)	CCII−	CCII+	7	21
2	I-Fig. 4(a)	ICCII−	ICCII−	8	New
3	I-Fig. 4(a)	CCII+	ICCII−	8	New
4	I-Fig. 4(a)	ICCII+	CCII+	7	New
5	II-Fig. 4(b)	CCII+	CCII+	9	22
6	II-Fig. 4(b)	ICCII+	ICCII−	10	New
7	II-Fig. 4(b)	CCII−	ICCII−	10	New
8	II-Fig. 4(b)	ICCII−	CCII+	9	New

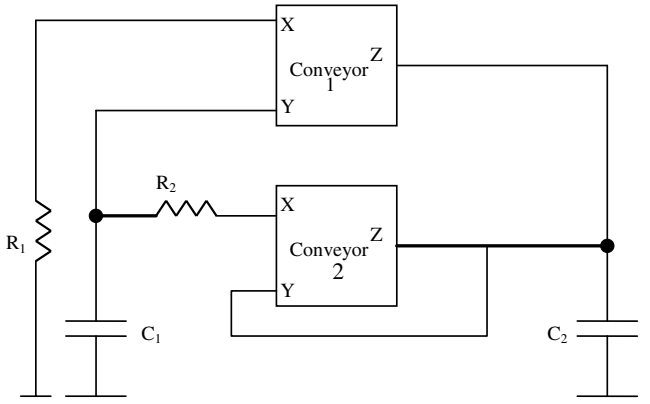

Fig. 4(a). Generalized configuration-I realizing grounded-C oscillators.

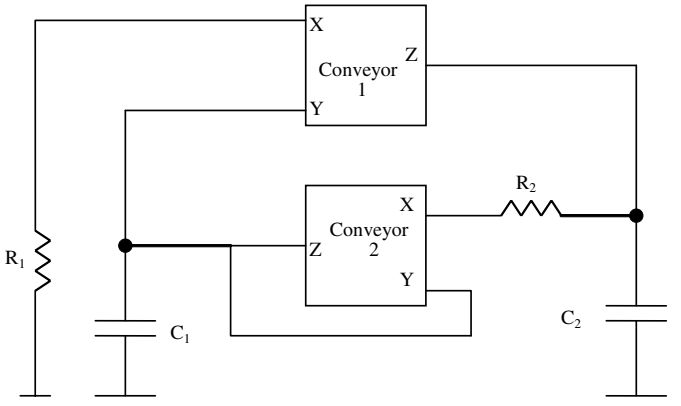

Fig. 4(b). Generalized configuration-II realizing grounded-C oscillators.

5. Generation of Equivalent Oscillators

In this section, it is shown that by interchanging one circuit connection in the oscillator circuit numbers 1 and 2, will result in two additional grounded capacitors minimum component oscillators. One of the generated oscillators is new and the other was published before in Ref. 23.

Consider first the oscillator circuit number 2, in Table 2 and shown here in Fig. 5(a). By disconnecting the $Z-$ terminal of the second ICCII$-$ from node N and connecting it to the X terminal of the first ICCII$-$ results in the circuit shown in Fig. 5(b). As seen from Figs. 5(a) and 5(b) this terminal change does not affect the circuit in the ideal case. Figure 5(b) is redrawn in an alternative simpler form as shown in Fig. 5(c).

The same concept applies to oscillator circuit 1, in Table 2 and shown in Fig. 6(a) resulting in the equivalent oscillator shown in Fig. 6(b). It is worth noting that this

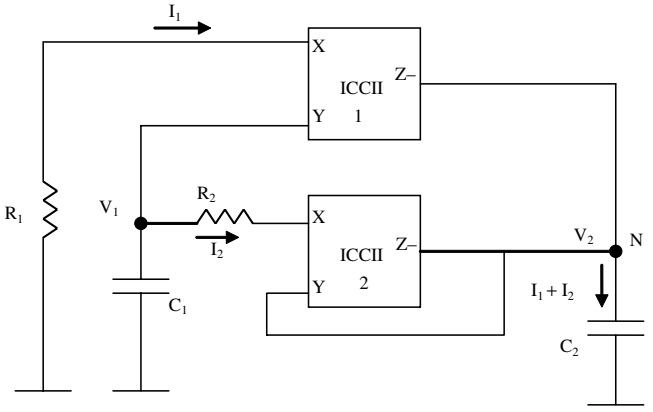

Fig. 5(a). The grounded-C oscillator circuit 2 using two ICCII−.

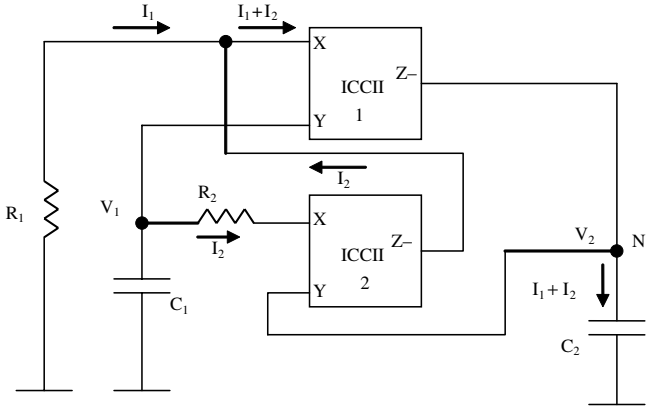

Fig. 5(b). New generated grounded-C oscillator using two ICCII−.

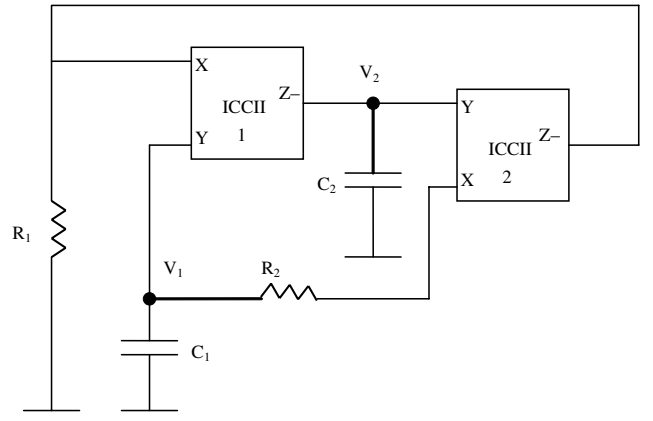

Fig. 5(c). Simplified drawing of the oscillator of Fig. 5(b).

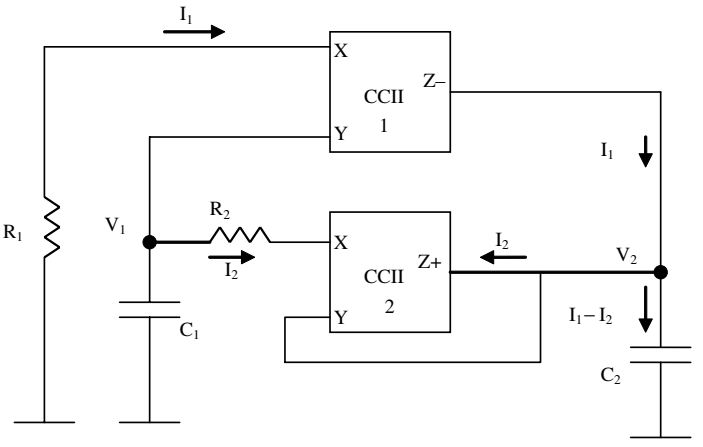

Fig. 6(a). The grounded-C oscillator circuit 1 using CCII+ and CCII−.

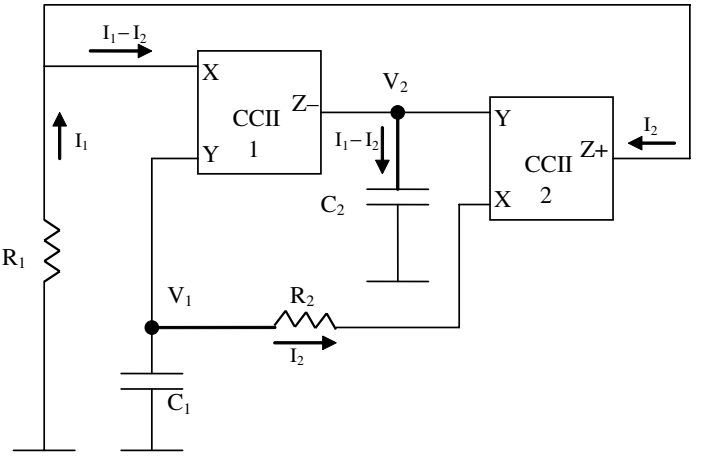

Fig. 6(b). Generated grounded-C oscillator circuit from Fig. 6(a).[23]

oscillator was reported before in Ref. 23. Thus the proposed Z-terminal change method results in providing new generation method of the oscillator in Ref. 23 from the FDNR grounded capacitor circuit number 1 in Table 1.

It should be noted that the generated oscillators of Figs. 5(c) and 6(b) are affected by the parasitic parameters R_{x_1} and C_{z_2}. The parasitic parameters R_{x_2} and C_{z_1}, however, can be absorbed in R_2 and C_2, respectively.

6. SPICE Simulation Results

The active building block used in the simulations included in this paper is the Differential Voltage Current conveyor (DVCC).[24] The DVCC is defined as a four-port

building block with a describing matrix of the form:

$$\begin{bmatrix} I_{Y_1} \\ I_{Y_2} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_{Y_1} \\ V_{Y_2} \\ I_X \\ V_Z \end{bmatrix} . \tag{12}$$

The DVCC is a very powerful building block as it realizes each of CCII+, CCII−, ICCII+ and ICCII− as special cases.

Figure 7 represents the CMOS-DVCC circuit,[24] the transistor aspect ratios are given in Table 3 based on the 0.5 μm CMOS model from MOSIS. The supply voltages used are ± 1.5 V and $V_{B_1} = -0.52$ V and $V_{B_2} = 0.33$ V. The Spice simulation results for different oscillator circuits are shown in Figs. 8–10.

Figure 8 represents the output waveform of the oscillator of Fig. 3(b) designed for f_0 equal to 1 MHz by taking $C_1 = 80$ pF, $C_2 = 40$ pF, $R_1 = 4\,\text{k}\Omega$ and $R_2 = 2\,\text{k}\Omega$.

Figure 9(a) represents the output waveform of the oscillator number 2 in Table 2, which is shown in Fig. 5(a) designed for f_0 equal to 1 MHz by taking $C_1 = C_2 = 40$ pF, $R_1 = R_2 = 4\,\text{k}\Omega$. The simulation results indicate an oscillation frequency slightly less than 1 MHz due to the parasitic R_X and C_Z added to the circuit parameters.

Figure 9(b) represents the output waveform of the oscillator circuit number 1 in Table 2 designed for f_0 equal to 0.5 MHz by taking $C_1 = C_2 = 80$ pF, $R_1 = R_2 = 4\,\text{k}\Omega$.

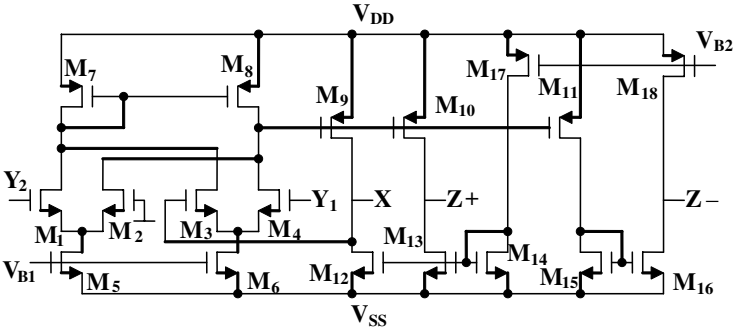

Fig. 7. CMOS realization of the DVCC.[24]

Table 3. Dimensions of the MOS transistors in the DVCC of Fig. 8.

Transistor	W (μm)/L (μm)
M_1, M_2, M_3, M_4	2.5/1
M_5, M_6	8/1
M_{12}, M_{13}, M_{14}, M_{15}, M_{16}	20/2.5
M_7, M_8	10/1
M_9, M_{10}, M_{11}, M_{17}, M_{18}	40/2

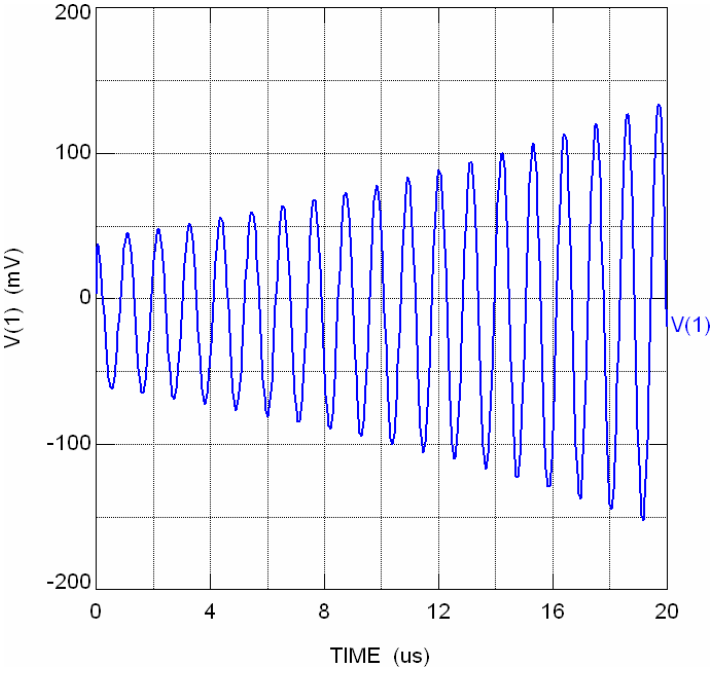

Fig. 8. Simulated output waveform for the circuit of Fig. 3(b).

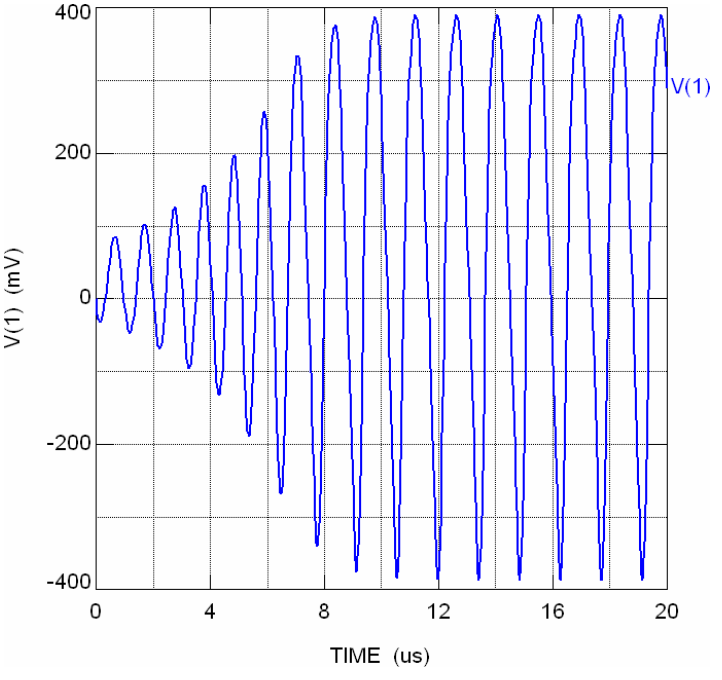

Fig. 9(a). Simulated output waveform for circuit 2 in Table 2.

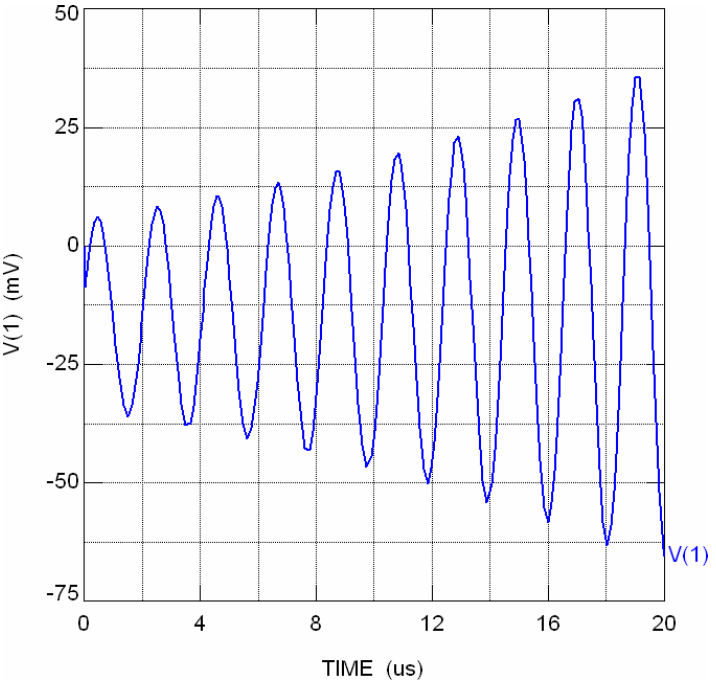

Fig. 9(b). Simulated output waveform for circuit 1 in Table 2.

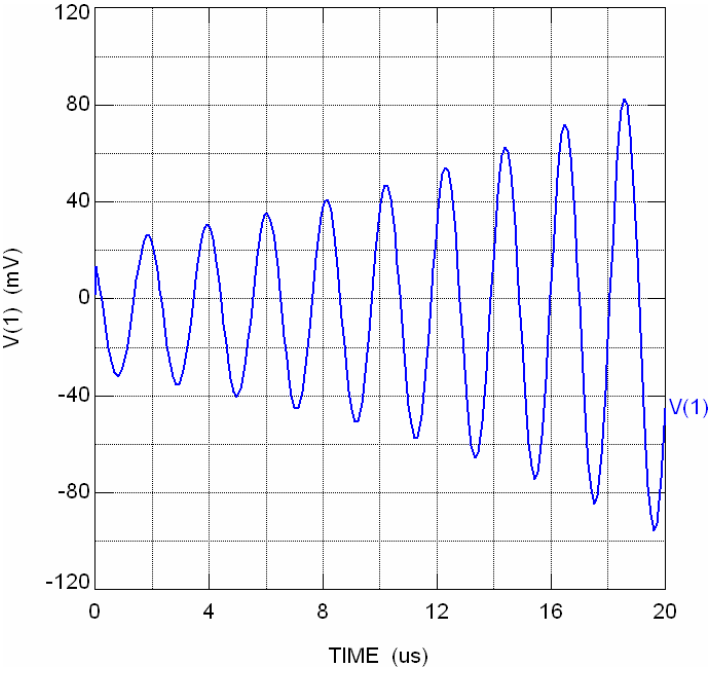

Fig. 9(c). Simulated output waveform for circuit 6 in Table 2.

Figure 9(c) represents the output waveform of the oscillator circuit number 6 in Table 2 designed for f_0 equal to 0.5 MHz by taking $C_1 = C_2 = 80\,\text{pF}$, $R_1 = R_2 = 4\,\text{k}\Omega$.

It should be noted that the oscillator circuit numbers 1 and 5 in Table 2 have been simulated and tested experimentally in Refs. 21 and 22. The active building block used in Refs. 21 and 22 is the Bipolar AD 844[25] and the simulated frequency is around 15 kHz which is much lower than the simulation frequency in this paper. A detailed comparison between the two circuits; numbers 1 and 5 in Table 2 is given in Ref. 21.

Figure 10(a) represents the output waveform of the oscillator circuit of Fig. 5(c) designed for f_0 equal to 1 MHz by taking $C_1 = C_2 = 40\,\text{pF}$, $R_1 = R_2 = 4\,\text{k}\Omega$.

Figure 10(b) represents the output waveform of the oscillator circuit of Fig. 6(b) designed for f_0 equal to 1 MHz by taking $C_1 = C_2 = 40\,\text{pF}$, $R_1 = R_2 = 4\,\text{k}\Omega$.

It should be noted that the oscillator circuit performance depends on the current conveyor circuit used whether it is a CMOS circuit or a bipolar circuit and the accuracy of the current conveyor is the dominant factor affecting the oscillator performance.

7. Conclusions

Eight new grounded capacitor FDNR circuits based on the FDNR circuits of Fig. 1 are introduced in this paper. The eight FDNR circuits are used to generate eight

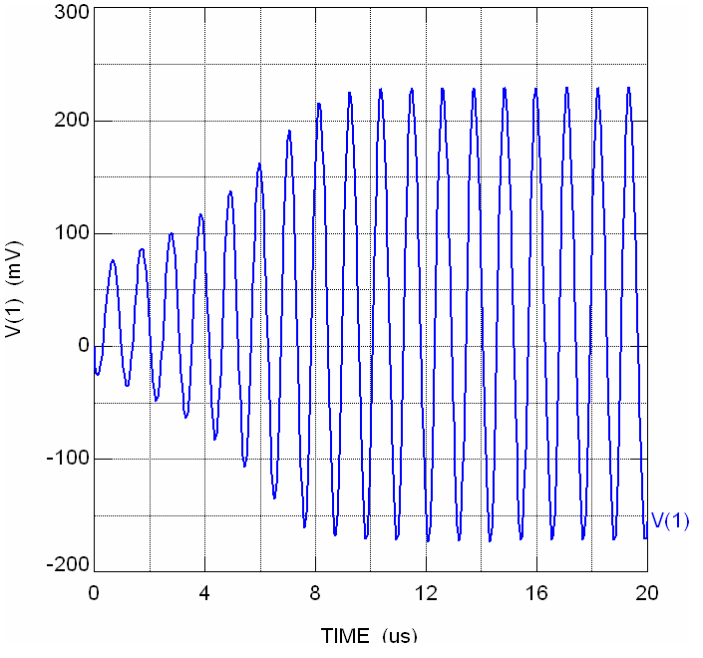

Fig. 10(a). Simulated output waveform for the oscillator circuit of Fig. 5(c).

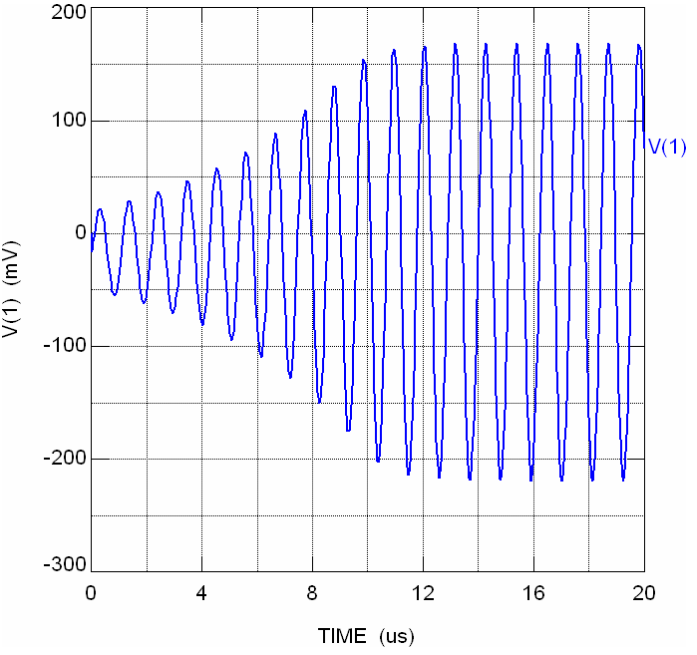

Fig. 10(b). Simulated output waveform for the oscillator circuit of Fig. 6(b).

grounded capacitor oscillators. Two of the generated oscillators were reported before in Refs. 21 and 22 and the current controlled CCII (CCCII) version was also given. All of the generated eight oscillators have the advantage of being easily compensated by absorbing the magnitude of the parasitic resistance R_x and the parasitic capacitance C_z in resistors and capacitor circuit elements.

Two additional oscillators circuits are obtained by simple Z terminal change method; one of them uses two ICCII− and the other uses one CCII− and one CCII+ and was reported before in Ref. 23. These two oscillators given in Fig. 5(c) and Fig. 6(b) are directly compensated for C_{z_1} and R_{x_2}. They are affected however by the stray parameters C_{z_2} and R_{x_1}.

Spice simulation results using technology: SCN 05 feature size 0.5 μm, MOSIS Vendor: AGILENT to demonstrate the practicality of the proposed oscillators are included. It is worth noting that the oscillator circuits number 2 and 7 in Table 2 have a floating property.

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