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# New Square-Root Domain Oscillators

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**Abstract.** This paper proposes a systematic design procedure to transform the conventional $G_m$-C oscillators to square-root domain voltage oscillators. These transformed oscillators have the square-root domain advantages such as good bandwidth-linearity compromise in addition to low power dissipation. An oscillator will be considered as an example with its analytical derivations and simulation results.

**Key Words:** square root domain, oscillators, $G_m$-C

## 1. Introduction

Square-root domain (SRD) circuits are considered a subclass from the family of externally linear internally nonlinear (ELIN) circuits. As a part of ELIN circuits they enjoy a very good bandwidth-linearity compromise in addition to the low power dissipation [1–6]. In the coming sections a proposal for a systematic design method to transform the conventional Gm-C oscillators into voltage-mode SRD is presented. Section 2 presents the transformation design method. Section 3 introduces the used building blocks. Section 4 gives an example of a transformed oscillator and demonstrates its derivations and its simulation results.

## 2. The Transformation Design Method

$G_m$-C circuit transformation method [2, 7] addressed only the case of transforming conventional $G_m$-C circuits which use single input single output nonlinear transconductors into SRD counterpart. This transformation makes ELIN filter externally equivalent to the $G_m$-C filter, but with internal voltages as compressed version of their $G_m$-C counterparts. However, there are other types of $G_m$-C circuits which use the differential input linear transconductors as shown in Fig. 1.

Those other types of $G_m$-C circuits [8] can be transformed easily into square-root domain counterparts by component substitution. This component substitution means to replace every linear transconductor by its SRD equivalent. For example, the SRD equivalent for the differential input single output transconductor is shown in Fig. 2.

This equivalence can be proven by the following derivations:

$$I_{\text{out}} = \sqrt{I_i I_{o1}} - \sqrt{I_j I_{o2}} = \sqrt{\frac{K_i I_{o1}}{2}}(V_i - V_T) - \sqrt{\frac{K_j I_{o2}}{2}}(V_j - V_T) \quad (1)$$

Taking $I_{o1} = I_{o2} = I_o$ and $K_i = K_j = K$ then the equation will be:

$$I_{\text{out}} = g_m(V_i - V_j) \quad (2)$$

Where $g_m = \sqrt{\frac{K I_o}{2}}$ is the SRD transconductance.

Similarly one can get the SRD equivalent for both double output and balanced output linear transconductors. This can be done using the SRD equivalent of single output case as shown in Fig. 3(a, b).

In all other design techniques of square-root domain circuits [1, 2, 5, 6], the main purpose of them is to keep the nonlinearity inherent inside the circuits, while performing a linear external function. As in those techniques the compressor block, compresses the input current swings nonlinearly into small internal voltage swings, and these compressed voltages are nonlinearly processed, thus the signal dynamic range becomes less influenced by a reduction in supply voltage, so it is suitable to achieve a large dynamic range in a low supply voltage environment, and the expander block will expand the resulted voltage nonlinearly into output current again. This concept of linearizing only the external performance is used to avoid loses in the frequency response or the linearity as was the problem in $G_m$-C circuits. Because linearizing each block may increase the complexity and hence degrades the frequency response or the input

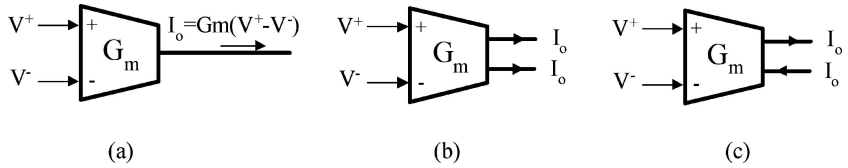


*Fig. 1.* Differential input linear transconductors. (a) Single output. (b) Double output. (c) Balanced output.

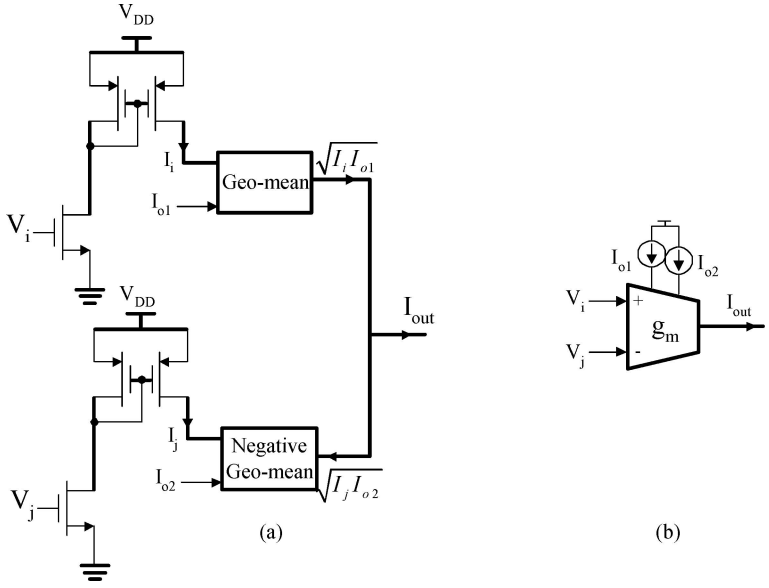


*Fig. 2.* (a) SRD equivalent implementation of single output linear transconductor. (b) Its symbol.

signal must be limited significantly to work in the linear region of all blocks and in this case linearity is highly reduced. But the difference here than any other techniques that by this substitution, every block has a linear relationship between its inputs and outputs (linearizing each block of the circuit) plus obtaining the overall linear function (the same purpose of other techniques). This new technique is simple and gives the designer the facility to derive easily the square-root domain transfer function from the linear counterpart as it is direct linear substitution. Besides these linearized blocks (transconductors) can work under lower supplies, the advantage of square-root domain circuits because of its compression nature, as they are implemented using square-root domain building blocks. And the linearizing of each block will not increase the complexity to the limit that may degrade the frequency response of the circuit. Though the linearizing of each block may cause the circuit to lose a part of the advantage of working with compressed voltages in the nodes between those linearized blocks, it still works under lower supplies with wide dynamic range because these

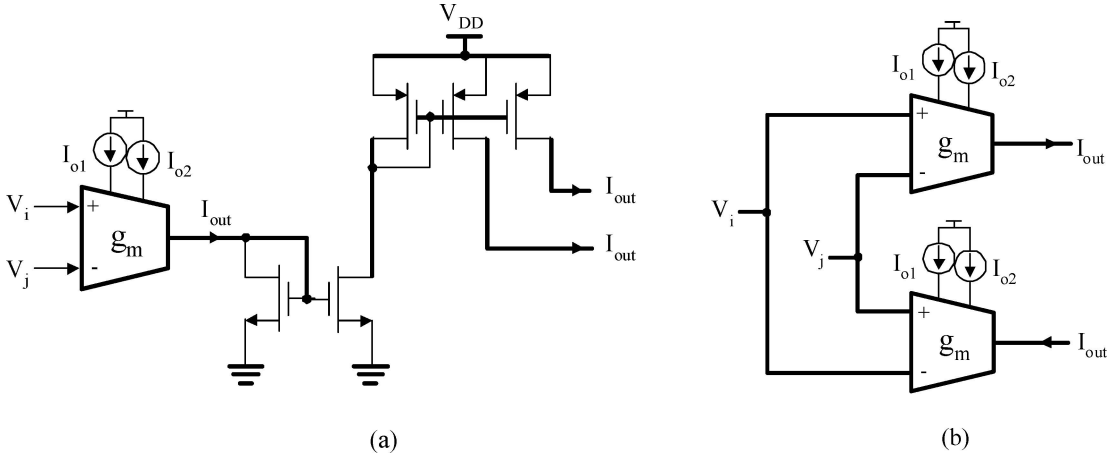


*Fig. 3.* (a) SRD equivalent implementation of double output linear transconductor. (b) SRD equivalent implementation of balanced output linear transconductor.

*Table 1.* The transistor aspect ratios of the geometric mean implementation circuit.

| Transistor | $M_{1-4}$ | $M_5$ | $M_{6-7}$ | $M_{8-9}$ | $M_{10}$ | $M_{11}$ | $M_{12-13}$ | $M_{14-17}$ |
|---|---|---|---|---|---|---|---|---|
| W ($\mu$m) | 4 | 64 | 16 | 8 | 32 | 16 | 8 | 16 |
| L ($\mu$m) | 4 | 4 | 4 | 4 | 4 | 4 | 1 | 1 |

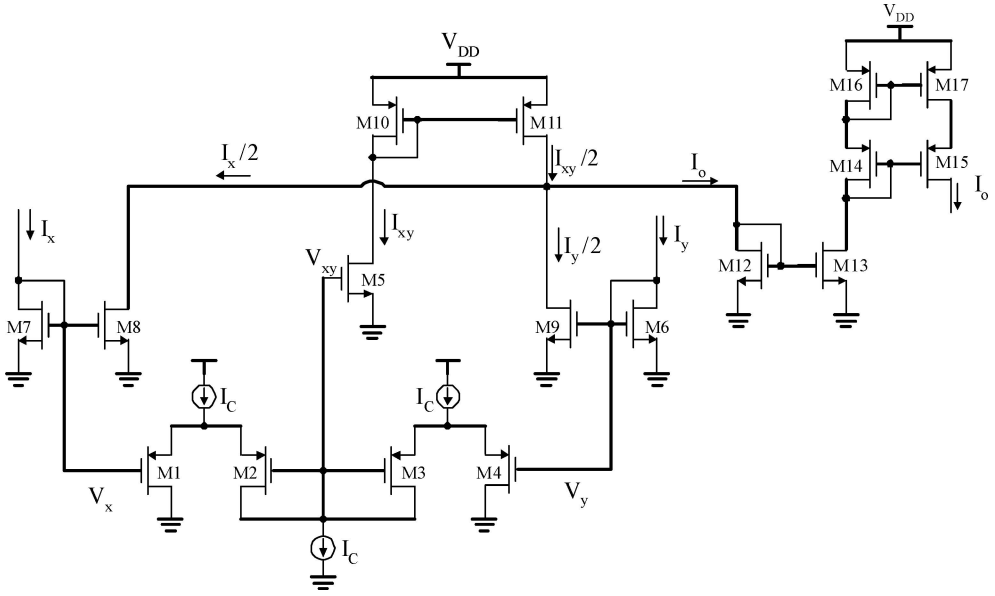


*Fig. 4.* Positive geometric mean implementation.

nodes connected to square-root domain blocks; hence their voltage swing is still limited and may be considered as compressed voltage processing. Thus, this method is very useful especially for those applications that may not need very high dynamic range.

## 3. Building Blocks Used

The building blocks needed here are positive and negative geometric mean blocks. The geometric mean block realizes the relation $I_{\text{geomean}} = \sqrt{I_x I_y}$. The positive and negative versions depend on the direction of the output current $I_{\text{geomean}}$ (positive means to source the output current and negative means to sink the output current). From a fair comparison between the common implementations of geometric mean cells [6 ] it is found that Vlassis' geometric mean block [3] combines the good functionality besides small area, low complexity and low power dissipation. But it suffers from the sensitivity towards the output node voltage variations which usually happens because of connecting it to a capacitor whose voltage may vary over a wide range. Thus a modification is done by adding a cascoded current mirror as an output stage to isolate the voltage variations from the functioning core of the circuit to not affect its performance as shown in Fig. 4.

Its supply is reduced also to be 3V and its transistors are resized to step down the channel length to 1 $\mu$m (as shown in Table 1) to not enter submicron region with its host of second order and short channel effects. This resizing and supply reduction reduced more the power dissipation and the area of this circuit to be 144 $\mu m^2$ while the bandwidth is increased because long channel length devices much above 1 $\mu$m have a large parasitics that limit the bandwidth dramatically.

## 4. An Example of a New Square-Root Domain Oscillator

By applying the previous substitution on any conventional $G_m$-C oscillator [8], one can obtain its SRD counterpart as shown in Fig. 5 as an example.

One can obtain the condition of oscillation and hence the oscillation frequency in the new square-root domain oscillator shown in Fig. 5 similarly as in the $G_m$-C counterpart

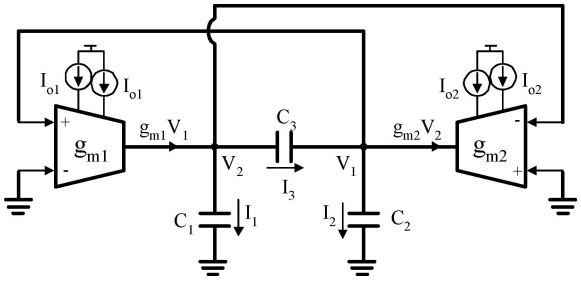


*Fig. 5.* The equivalent SRD counterpart of the example oscillator.

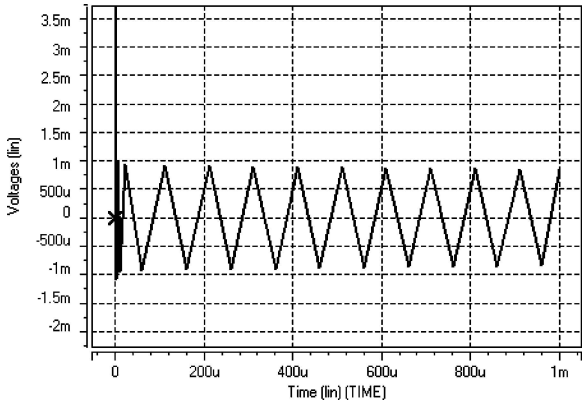


*Fig. 6.* The performance of equivalent SRD counterpart of the example oscillator.

circuit because of the direct linear substitution used in this technique, and that can be derived as follows:

$$g_{m1}V_1 = I_1 + I_3 = (V_2 - V_1)sC_3 + V_2sC_1 \tag{3}$$

$$g_{m2}V_2 = I_3 - I_2 = (V_2 - V_1)sC_3 - V_1sC_2 \tag{4}$$

These equations can be rewritten as follows:

$$V_1(g_{m1} + sC_3) = V_2(sC_3 + sC_1) \tag{5}$$

$$V_1(sC_3 + sC_2) = V_2(sC_3 - g_{m2}) \tag{6}$$

From (5) and (6) one can deduce that:

$$\frac{(sC_3 + sC_1)}{(g_{m1} + sC_3)} = \frac{(sC_3 - g_{m2})}{(sC_3 + sC_2)} \tag{7}$$

$$\therefore \quad s^2(C_1C_2 + C_1C_3 + C_2C_3) + s(g_{m2}C_3 - g_{m1}C_3) + g_{m1}g_{m2} = 0 \tag{8}$$

Hence, the condition of oscillation is:

$$g_{m1} = g_{m2} \tag{8}$$

$$\therefore\ I_{o1} = I_{o2} = I_o \text{ and } K_1 = K_2 = K \tag{8}$$

And the frequency of oscillation is:

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2 + C_1C_3 + C_2C_3}} = \sqrt{\frac{K\,I_o}{2(C_1C_2 + C_1C_3 + C_2C_3)}}$$

The oscillator performance at $V_1$ is shown in Fig. 6 (using HSPICE and a BISIM 3v3 0.5 $\mu$m model) for $I_o = 100\,\mu A$ (where $C_1 = C_2 = C_3 = 10$ pF). Notice, it is a voltage-mode oscillator with amplitude of 2 mV because it is the acceptable range of voltage variations on the gate to source nodes.

Though these transformed oscillators may lose some advantages of the current-mode circuits, they are very important to complete the design tools to build any SRD large application circuits, as they are still needed in some cases where the current oscillators can not be used. Of course they have to be employed in square-root domain environment to be useful as an oscillator with their small amplitudes. Because these small amplitudes are in the acceptable range to drive a MOS gate which may be an input device of another square-root domain stage or circuit.

## 5. Conclusions

A systematic design procedure to transform the conventional $G_m$-C oscillators to square-root domain voltage oscillators is given. These transformed oscillators have the square-root domain advantages such as good bandwidth-linearity compromise in addition to low power dissipation. An oscillator is considered as an example with its analytical derivations and simulation results. This design procedure can be used also to transform other conventional $G_m$-C circuits to square-root domain counterparts.

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