Available online at www.sciencedirect.com
SCIENCE DIRECT®
Int. J. Electron. Commun. (AEÜ) 59 (2005) 384–391
International Journal AEÜ of Electronics and Communications
www.elsevier.de/aeue

New high accuracy CMOS current conveyors

Wessam S. Hassanein[a], Inas A. Awad[b], Ahmed M. Soliman[c,*]

[a]*Department of Electrical and Computer Engineering, Carnegie Mellon University, 5000 Forbes Avenue, Pittsburgh PA 15213, USA*
[b]*Electronics and Communications Engineering Department, Cairo University, Fayoum-Campus, Fayoum, Egypt*
[c]*Electronics and Communications Engineering Department, Cairo University, Giza, Egypt*

Abstract

In this paper, a new CMOS CCII$^+$ is proposed. The circuit is characterized by high precision in voltage tracking and exhibits very low input resistance. An adaptive voltage offset cancellation methodology is introduced and then applied to the proposed circuit. As a result, a higher accuracy CCII$^+$ is presented. For both circuits, the voltage offset cancellation is independent of the input current and voltage. To demonstrate the strength of the proposed architectures, fair comparisons with Liu and Yodprasit CCII realizations are held.

Keywords: CMOS current conveyors; Current-mode; Analog signal processing; Adaptive voltage offset cancellation

1. Introduction

Over the last few years, the advantages of using current-mode circuits have made the current-mode approach very attractive to analog circuit designers [1–3]. One of the most versatile current-mode building blocks is the second generation current conveyor CCII which was introduced by Sedra and Smith in 1970 [4–6]. The demand for CCII CMOS realizations suitable for high accuracy analog signal processing has led analog designers to make efforts in finding CCII architectures that meet this requirement. The CCII$^+$ realizations proposed in [7–10] provides considerable accuracy as well as wide bandwidth. Among those circuits, Liu CCII [8] provides the highest accuracy. Yet, Yodprasit proposed a higher accuracy CCII suitable for low-frequency applications [11]. Throughout this paper the abbreviation CCII is used instead of CCII$^+$.

A new high accuracy class-A CMOS CCII is proposed in this paper (Fig. 1). The circuit exhibits voltage transfer gain of almost unity, voltage offset in the order of microvolts as well as very low input resistance in the order of milliohms. An adaptive voltage offset cancellation methodology is introduced and then applied to the circuit resulting in a new CCII (Fig. 2) that achieves the highest voltage tracking accuracy and the lowest input resistance among all the circuits reported in [7–11]. For the two CCII realizations proposed in this paper, the voltage offset cancellation is independent of the input current and voltage.

The proposed circuits as well as those reported in [7–11] are designed following a fair comparison criterion [12]. The supply voltages are fixed to 1.5 and −1.5 V. Aspect ratios of equivalent transistors are equal. Equivalent current sources are identical. TOP SPICE simulations are all carried out with level 8 model parameters of 0.5 μm CMOS process provided by MOSIS (AGILENT).

2. New high accuracy current conveyors

The CMOS realization of the proposed high accuracy CCII is shown in Fig. 1. The groups of the transistors (M1 and M2), (M3–M5), (M7–M9), as well as (M11–M13) are matched. Assuming that all the transistors operate in their

* Corresponding author.
E-mail address: asoliman@idsc.net.eg (Ahmed M. Soliman).

1434-8411/$ - see front matter © 2004 Elsevier GmbH. All rights reserved.
doi:10.1016/j.aeue.2004.10.001

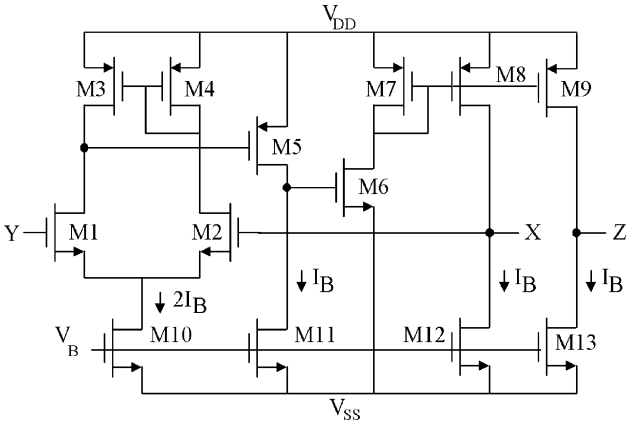

Fig. 1. High accuracy CCII.

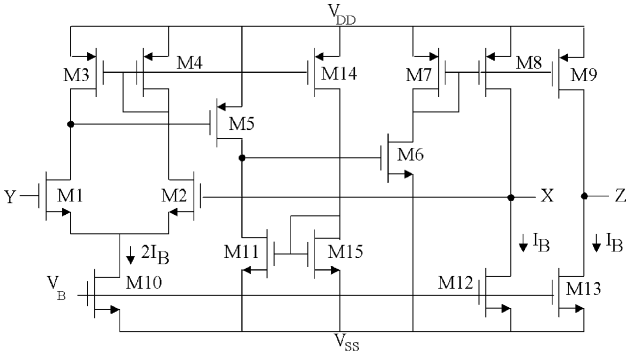

Fig. 2. High accuracy CCII with adaptive offset cancellation.

saturation regions, the operation of the circuit can be explained as follows. Transistors M10 to M13 serve as DC current sources. The structure is based on the long tail pair (M1 and M2). The current mirroring (achieved by M3 and M4) along with the equilibrium (achieved by feedback control) forces equal currents I_B in the transistors M1 and M2. This operation drives the gate-to-source voltages of M1 and M2 to be equal and, consequently, forces the voltage at terminal X to follow the voltage at terminal Y. Since M8 and M9 carry the same drain current as M7, and since M12 and M13 carry the same DC current I_B, the X terminal current is conveyed to the Z terminal.

The circuit adopts the following offset cancellation technique. The voltage offset is given by the following relation [13]:

$$\Delta V = V_x - V_y \approx [\lambda_n (V_{D1} - V_{D2})] \sqrt{\frac{I_B}{\mu_n C_{ox}\, W_1/L_1}}, \quad (1)$$

where λ_n is the channel length modulation parameter, V_{D1} and V_{D2} are the drain voltages of M1 and M2, respectively. This offset can be cancelled by making V_{D1} equal to V_{D2}.

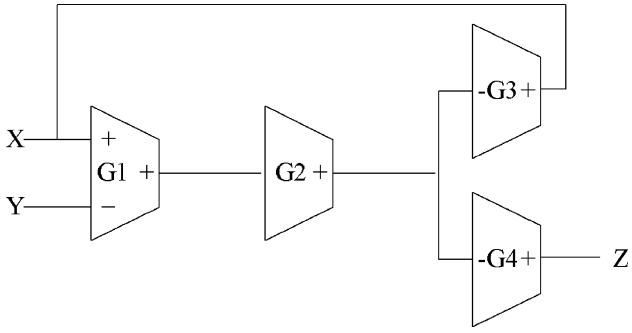

Fig. 3. Block diagram of the circuit shown in Fig. 1.

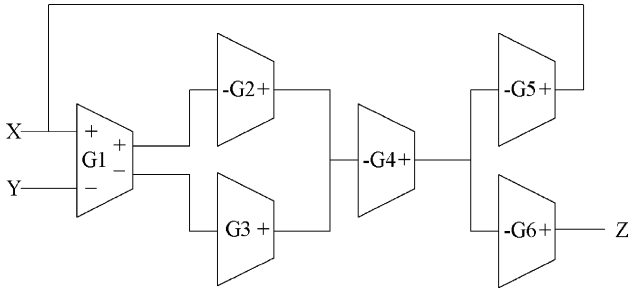

Fig. 4. Block diagram of the circuit shown in Fig. 2.

Table 1. Transistors aspect ratios of the circuit shown in Fig. 1

Transistor	$W(\mu m)/L(\mu m)$
M1, M2	60/1
M3–M5	100/2.5
M6	20/0.5
M7–M9	100/2.5
M10	100/2.5
M11–M13	50/2.5

$$V_{D1} - V_{D2} = \sqrt{\frac{I_{D4}}{\mu_p C_{ox}\, \frac{W_4}{L_4}}} - \sqrt{\frac{I_{D5}}{\mu_p C_{ox}\, \frac{W_5}{L_5}}}. \quad (2)$$

I_{D10} is taken equal to $2I_B$. It is seen from Eq. (2) that the offset cancellation is achieved by matching M4 and M5 and by making $I_{D4} = I_{D5} = I_B$. This is done by making $I_{D11} = \frac{1}{2} I_{D10} = I_B$. This offset cancellation is independent of the input current and voltage. Yet, the stated doubling cannot be achieved precisely as long as the drains of M10 and M11 are at different voltage levels. This is a disadvantage.

To overcome this disadvantage, a modified version of the circuit shown in Fig. 2 is proposed. Transistors M14 (matched to M3 and M4) and M15 (matched to M11) are added. The strength of this circuit is that it adopts an elegant adaptive voltage offset cancellation technique. To achieve

the equality of I_{D4} and I_{D5}, M14 copies I_{D4} and delivers it to M5 via the current mirror transistors (M11 and M15). To achieve precise current mirroring, the common source transistor M6 keeps the drain of M11 in a close potential to the drain of M15. Hence, the circuit overcomes the disadvantage mentioned above and exhibits higher accuracy. Still, the adaptive offset cancellation is independent of the input current and voltage.

In Liu CCII [8] (where cascoding is removed and ordinary current mirrors are used instead of the CCI cells in order to maintain fair tradeoffs for comparison), offset cancellation is dependent on the input current which is a considerable disadvantage. Another disadvantage is that the doubling constraint mentioned earlier exists. Yodprasit omitted this doubling constraint in his circuit [11]. Yet, the offset cancellation is dependent on the input voltage resulting in a narrow input voltage range which is a considerable disadvantage.

Fig. 3 shows the block diagram of the high accuracy CCII (Fig. 1). Four transconductances are included. The first represents the long tail pair (M1 and M2) where $G_1 = g_{m1} = g_{m2}$. The second represents the two cascaded common source stages (M5 and M11) and (M6 and M7) where $G_2 = g_{m5}g_{m6}/(g_{d5} + g_{d11})$. The third and the fourth represent the common source transistors M8 and M9, respectively, where $G_3 = g_{m8}$ and $G_4 = g_{m9}$. The block diagram is similar to that of Liu CCII except for the extra non-inverting transconductance G_2. Hence, a higher open-loop voltage gain CCII exists. Consequently, higher accuracy in voltage following and lower input resistance at terminal X are expected. However, the circuit is expected to pay degradation in bandwidth due to the well known trade off between gain and bandwidth. The small signal voltage transfer gain, input resistance and output resistance are given by

$$\frac{v_x}{v_y} = \frac{g_{m1}g_{m5}g_{m6}}{g_{m1}g_{m5}g_{m6} + (g_{d1} + g_{d3})(g_{d5} + g_{d11})(g_{d8} + g_{d12})}, \quad (3)$$

where $g_{m1} = g_{m2}$.

$$r_x = \frac{(g_{d1} + g_{d3})(g_{d5} + g_{d11})}{g_{m1}g_{m5}g_{m6}}, \quad (4)$$

$$r_z = \frac{1}{g_{d9} + g_{d13}}. \quad (5)$$

Fig. 4 shows the block diagram of the high accuracy CCII with adaptive offset cancellation (Fig. 2). The block diagram is similar to that in Fig. 3 except for the insertion of the non-inverting transconductance G_3 (which represent the common source transistor M14 and the current mirror transistors M11 and M15) as well as the split of G_2 and G_4. Hence, a higher open loop gain compared to the first proposed CCII exists. Consequently, higher accuracy in voltage tracking is expected. Finally, the circuit is to pay more degradation in bandwidth.

It should be mentioned that the new realizations proposed in this paper target very high accuracy and are not intended to achieve wide bandwidth.

3. Simulation results

3.1. High accuracy CCII

I_B is taken 100 μA. Transistors aspect ratios are reported in Table 1. Simulation results are tabulated in Table 2 and shown in Figs. 5–9. The input voltage range is −0.4 to 0.8 V. The average value of open circuit voltage transfer gain equals 1.00003. The voltage offset varies from 0.00027 to 0.071 mV within the input voltage range. Fig. 5 shows that the voltage offset is relatively independent of the input current. The open circuit voltage transfer bandwidth exhibits a 3 dB frequency of 1.15 MHz (Fig. 6). The input current range equals to 200 μA. The average value of the short circuit current transfer gain equals to 1.000001. The current offset varies from −0.00016 to −0.00006 μA within the input current range. The short circuit current transfer bandwidth

Table 2. Parameters of Liu CCII and the circuit shown in Fig. 1

Parameter	Unit	Liu CCII [8]	First proposed CCII
Input voltage range	V	−0.5 to 0.8	−0.4 to 0.8
A_v (average value)	—	0.99998	1.00003
Maximum deviation from A_v	—	0.22%	0.06%
Voltage offset variation	mV	−0.078 to −0.056	0.00027 to 0.071
$f_{3\,dB}$ of voltage transfer gain	MHz	1660	1.15
Input current range	μA	−100 to 100	−100 to 100
A_i (average value)	—	0.99991	1.000001
Maximum deviation from A_i	—	0.02%	0.0003%
Current offset variation	μA	−0.0035 to 0.006	−0.00016 to −0.00006
$f_{3\,dB}$ of current transfer gain	MHz	95	15
R_X	Ω	10.46	0.037
THD for a sinusoid of 10 kHz	—	0.0012%	0.01816%

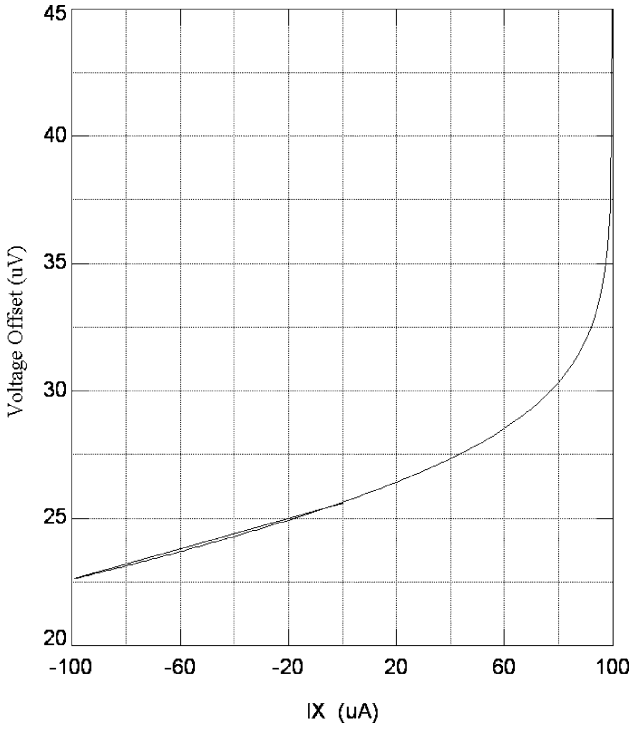

Fig. 5. Voltage offset variation versus I_X for the circuit shown in Fig. 1.

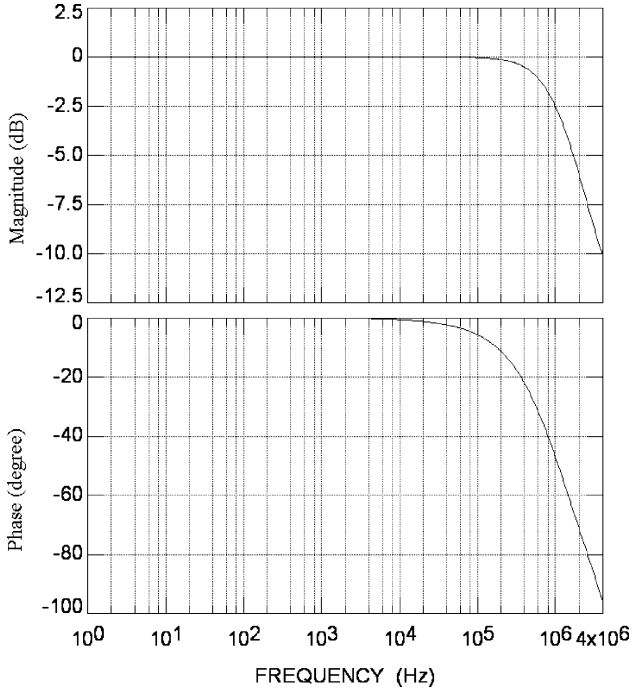

Fig. 6. Frequency characteristics of the open circuit voltage transfer gain between Y and X (V_X/V_Y) for the circuit shown in Fig. 1.

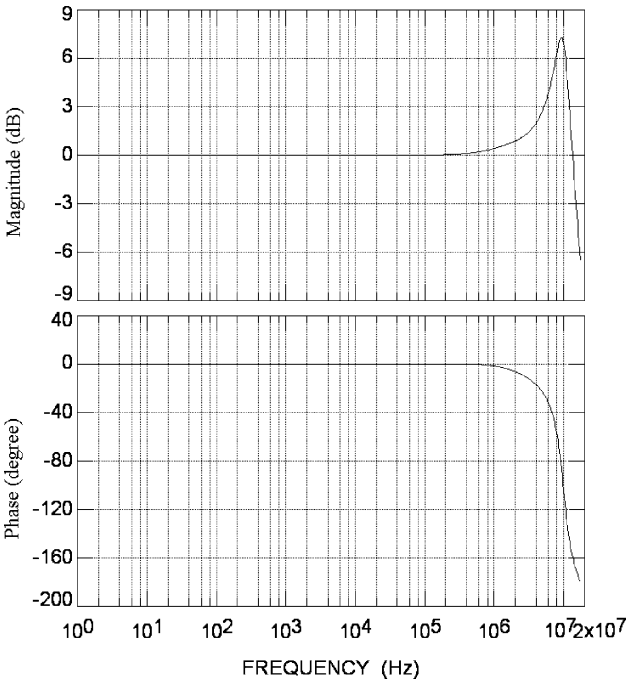

Fig. 7. Frequency characteristics of the short circuit current transfer gain between X and Z (I_Z/I_X) for the circuit shown in Fig. 1.

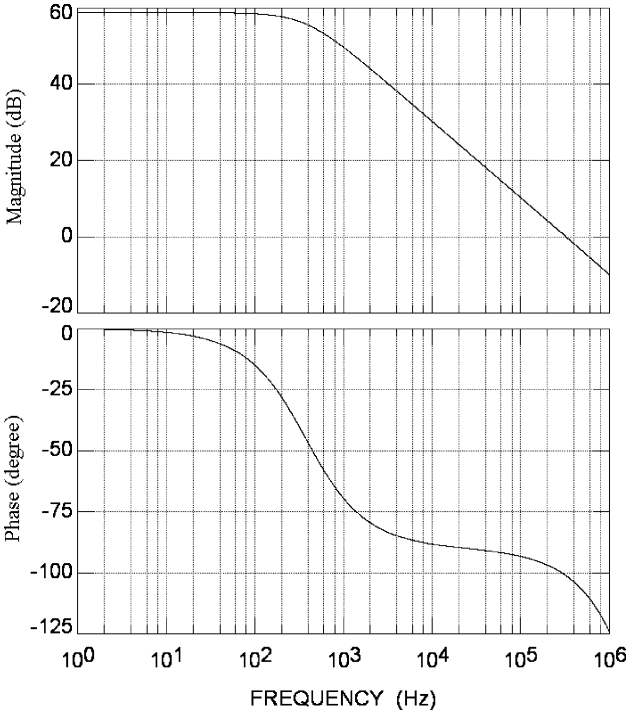

Fig. 8. Open loop frequency response of the circuit shown in Fig. 1.

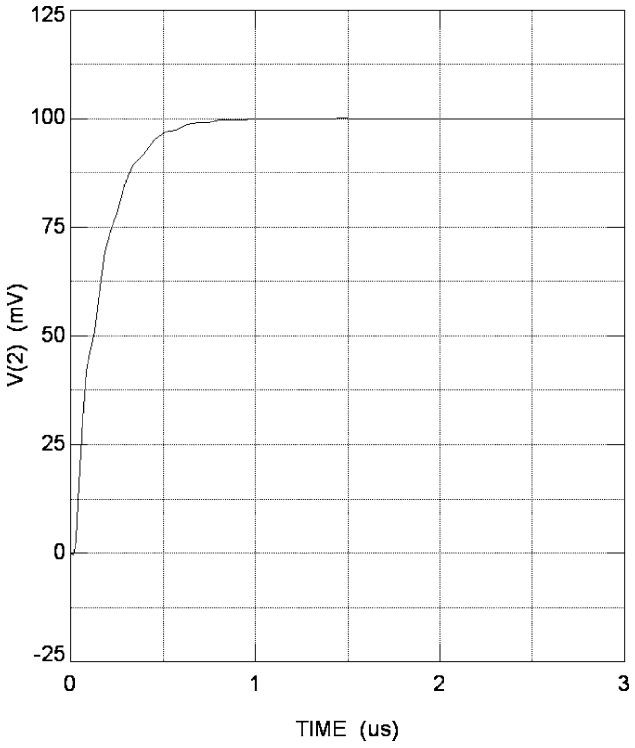

Fig. 9. The transient response of the circuit shown in Fig. 1.

Table 3. Transistors aspect ratios of the circuit shown in Fig. 2

Transistor	$W(\mu m)/L(\mu m)$
M1, M2	60/1
M3–M5, M14	100/2.5
M6, M11, M15	50/2.5
M7–M9	100/2.5
M10	100/2.5
M12, M13	50/2.5

exhibits a 3 dB frequency of 15 MHz (Fig. 7). The input resistance at terminal X at DC equals 0.037 Ω. The total harmonic distortion (THD) for an input sinusoid of frequency 10 kHz and amplitude 0.5 V p–p is 0.01816%.

To ensure the stability of the proposed architecture, the open loop circuit is simulated (Fig. 8) and the phase margin is found to be 79°. Also, the transient response of the closed loop circuit is simulated for an input step function at terminal Y (100 mV amplitude and 1 ns rise time). The output at terminal X is shown in Fig. 9. The output follows the input with no overshoots or oscillations where the settling time (within accuracy of 0.1%) equals to 1.5 μs.

Compared to Liu CCII [8], as shown in Table 2, the proposed CCII provides higher accuracy and much lower input resistance while achieving almost the same input voltage range.

3.2. High accuracy CCII with adaptive offset cancellation

I_B is taken 100 μA. Transistors aspect ratios are reported in Table 3. Simulation results are tabulated in Table 4 and shown in Figs. 10–14. The input voltage range is −0.46 to 0.96 V. The average value of the open circuit voltage transfer gain is exactly 1. The voltage offset varies from 0 to 0.00026 mV within the input voltage range. Fig. 10 shows that the voltage offset is relatively independent of the input current. The open circuit voltage transfer bandwidth exhibits a 3 dB frequency of 0.48 MHz (Fig. 11). The input current range equals to 200 μA. The average value of the short circuit current transfer gain equals to exactly 1. The current offset varies from −0.00009 to 0.00015 μA within the input current range. The short circuit current transfer bandwidth exhibits a 3 dB frequency of 2.16 MHz (Fig. 12). The input resistance at terminal X at DC equals 0.06 Ω. Finally, the total harmonic distortion (THD) for an input sinusoid of frequency 10 kHz and amplitude 0.5 V p–p is 1.03%.

Table 4. Parameters of Yodprasit CCII and the circuit shown in Fig. 2

Parameter	Unit	Yodprasit CCII [11]	Second proposed CCII
Input voltage range	V	−0.5 to 0.2	−0.46 to 0.96
A_v (average value)	—	0.999998	1
Maximum deviation from A_v	—	0.0025%	0.0018%
Voltage offset variation	mV	−0.0025 to −0.00047	0 to 0.00026
$f_{3\,dB}$ of voltage transfer gain	MHz	7.5	0.48
Input current range	μA	−100 to 100	−100 to 100
A_i (average value)	—	1.01034	1
Maximum deviation from A_i	—	1.11%	0.008%
Current offset variation	μA	−2.23 to −0.044	−0.00009 to 0.00015
$f_{3\,dB}$ of current transfer gain	MHz	6.6	2.16
R_x	Ω	0.1	0.06
THD for a sinusoid of 10 kHz	—	0.018%	1.03%

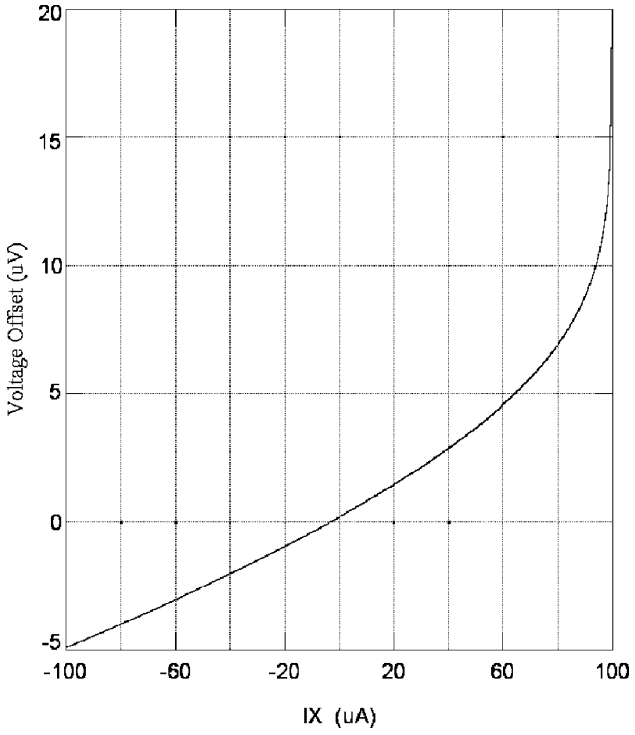

Fig. 10. Voltage offset variation versus I_X for the circuit shown in Fig. 2.

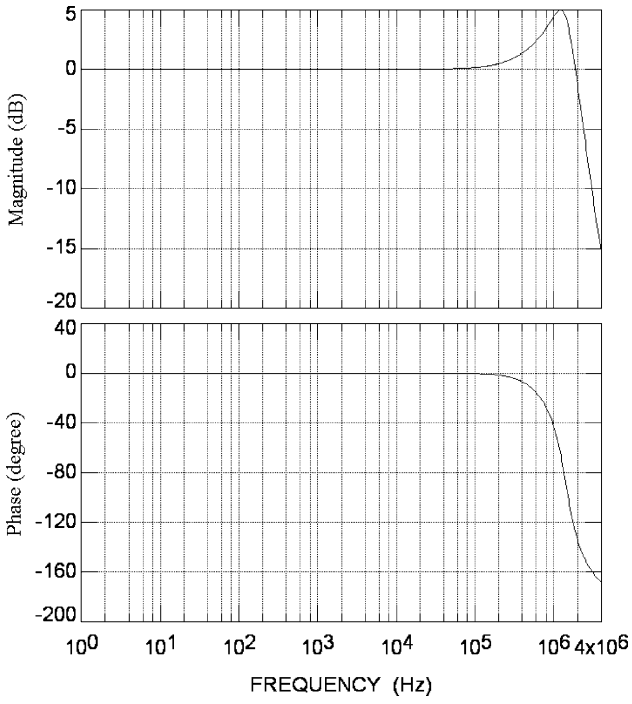

Fig. 12. Frequency characteristics of the short circuit current transfer gain between X and Z (I_Z/I_X) for the circuit shown in Fig. 2.

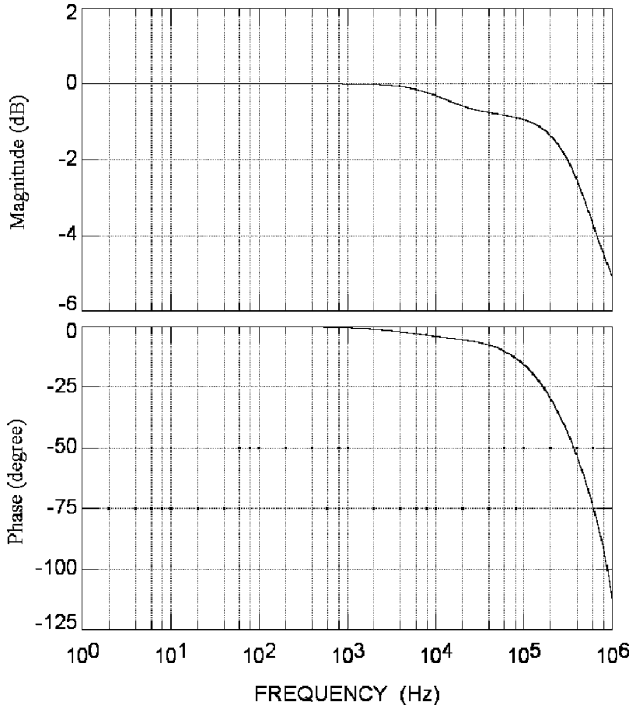

Fig. 11. Frequency characteristics of the open circuit voltage transfer gain between Y and X (V_X/V_Y) for the circuit shown in Fig. 2.

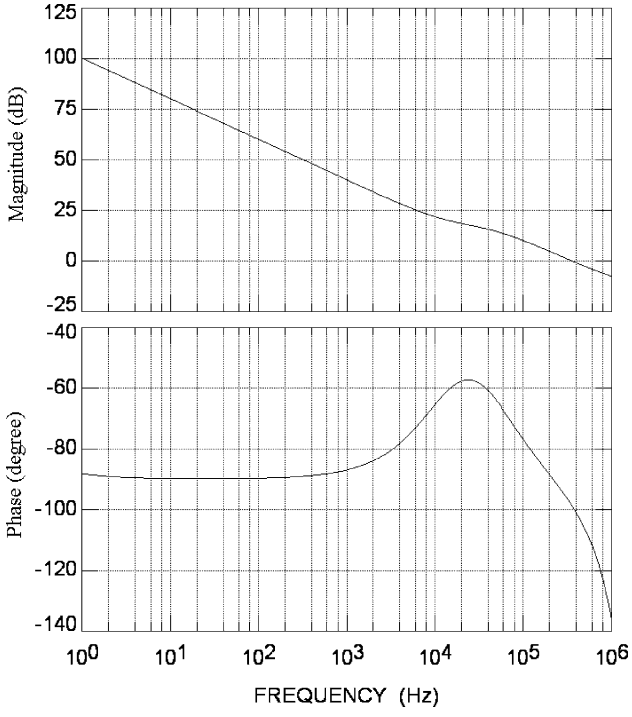

Fig. 13. Open loop frequency response of the circuit shown in Fig. 2.

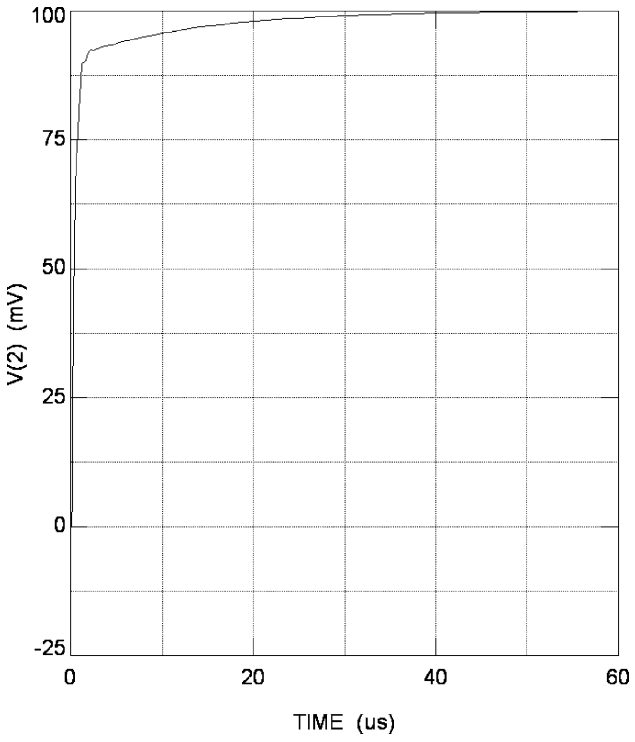

Fig. 14. The transient response of the circuit shown in Fig. 2.

Fig. 13 shows the open loop frequency response of the circuit. The phase margin equals 81°. Fig. 14 shows the transient response of the closed loop circuit for an input step function (100 mV amplitude and 1ns rise time). The output follows the input with no overshoots or oscillations where the settling time (within accuracy of 0.1%) equals to 60 μs.

Compared to Yodprasit CCII [11], as shown in Table 4, the proposed CCII exhibits wider input voltage range, higher voltage tracking accuracy as well as lower input resistance.

4. Conclusions

Firstly, a new high accuracy CMOS CCII was introduced. The circuit exhibits high precision in voltage tracking and an input resistance in the range of milliohms. Secondly, a new high accuracy CMOS CCII with adaptive offset cancellation was proposed. Comparisons based on simulation results showed that the circuit achieves the highest voltage tracking accuracy and the lowest input resistance among all the circuits reported in [7–11]. The proposed architectures serve high accuracy low frequency applications.

References

[1] Wilson B. Recent developments in current conveyors and current-mode circuits. IEE Proc-G 1990;137(2):63–77.
[2] Wilson B, Lidgey FJ, Toumazou C. Current mode signal processing circuits. IEEE international symposium on circuits and systems, Helsinki, vol. 3, 1998. p. 2665–8.
[3] Elwan HO. CMOS current mode circuits and its applications for analog VLSI. M.S. thesis, Cairo University, Cairo, Egypt, 1996.
[4] Sedra A, Smith KC. A second-generation current conveyor and its applications. IEEE Trans Circuit Theory 1970;17: 132–4.
[5] Smith KC, Sedra A. The current conveyor-a new circuit building block. IEEE Proc 1968;56:1368–9.
[6] Gohh F, Roberts GW, Sedra A. The current conveyor: history, progress and new results. IEE Proc-G 1990;137(2):78–87.
[7] Surakampontorn W, Riewruja V, Kumwachara K, Dejhan K. Accurate CMOS-based current conveyors. IEEE Trans Instrumentation Meas 1991;40:699–702.
[8] Liu S, Tsao H, Wu J. CCII-based continuous-time filters with reduced gain-bandwidth sensitivity. IEE Proc-G 1991; 138:210–6.
[9] Palmisano G, Palumbo G. A simple CMOS CCII^{+}. Int J Circuit Theory Appl 1995;23:599–603.
[10] Ismail AM, Soliman AM. Wideband CMOS current conveyor. Electron Lett 1998;34(25):2368–9.
[11] Yodprasit U. High-precision CMOS current conveyor. Electron Lett 2000;36:609–10.
[12] Ismail AM, Soliman AM. CMOS-CCII realizations based on the differential amplifier: a review. Frequenz 2000;54:182–7.
[13] Awad IA, Soliman AM. New CMOS realization of the CCII^{-}. IEEE Trans Circuits Systems II 1999;49(4):460–3.

Wessam S. Hassanein received the B.Sc. and M.Sc. degrees in Electronics and Communications Engineering from Cairo University, Cairo, Egypt in 2001 and 2003, respectively. He is currently a graduate student at Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh PA, USA.

He worked as a Teaching Assistant in Department of Electronics and Communications Engineering, Cairo University from September 2001 until July 2003. From January 2002 to May 2002, he worked as a Teaching Assistant in Department of Electronics Engineering, American University in Cairo. He has held a summer internship at Inter-University Microelectronics Center IMEC, Leuven, Belgium in 2000. His research interests include analog and digital circuits.

Inas A. Awad was born in Cairo, Egypt, in 1971. She received the Bachelor, the M.Sc. and the Ph.D. degrees in Electronics and Communications from Cairo University in 1994, 1997 and 2000, respectively. In 1995, she joined the department of Electronics and Communications, Cairo University, Fayoum-Campus as a teaching assistant and now she is an Assistant Professor at the same department. Her primary research interest is in analog circuits with particular emphasis on current-mode approach and low-voltage low-power CMOS designs.

Ahmed M. Soliman was born in Cairo Egypt, on November 22, 1943. He received the B.Sc. degree with honors from Cairo University, Cairo, Egypt, in 1964, the M.S. and Ph.D. degrees from the University of Pittsburgh, Pittsburgh, PA., USA, in 1967 and 1970, respectively, all in Electrical Engineering. He is currently Professor Electronics and Communications Engineering Department, Cairo University, Egypt. From September 1997–September 2003, Dr. Soliman served as Professor and Chairman Electronics and Communications Engineering Department, Cairo University, Egypt. From 1985–1987, Dr. Soliman served as Professor and Chairman of the Electrical Engineering Department, United Arab Emirates University, and from 1987–1991 he was the Associate Dean of Engineering at the same University. He has held visiting academic appointments at San Francisco State University, Florida Atlantic University and the American University in Cairo. He was a visiting scholar at Bochum University, Germany (Summer 1985) and with the Technical University of Wien, Austria (Summer 1987). In 1977, Dr. Soliman was decorated with the First Class Science Medal, from the President of Egypt, for his services to the field of Engineering and Engineering Education. Dr. Soliman is a member of the Editorial Board of Analog Integrated Circuits and Signal Processing. Dr. Soliman served as Associate Editor of the IEEE Transactions on Circuits and Systems I (Analog Circuits and Filters) from December 2001 to December 2003 and is currently Associate Editor of the Journal of Circuits, Systems and Signal Processing.