Current mode chaos generator

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Indexing terms: Chaos, Oscillators

A new chaos generator that uses the second generation current conveyor (CCII) as the active building block and produces a chaotic current output signal is introduced. The procedure of obtaining the generator by modifying a current mode sinusoidal oscillator using a nonlinear resistor of antisymmetrical current-voltage characteristics is emphasised. The small input resistance associated with the CCII inverting input terminal is found to be responsible for stimulating the circuit's chaotic nature. Experimental results, PSPICE simulations and numerical simulations of the derived mathematical model are included.

Introduction: Increasing interest in investigating the possible chaotic nature of conventional sinusoidal oscillators has been recently observed. It was first shown in [1, 2] that the Colpitts oscillator can behave chaotically. Innovative modifications of the Wien-bridge oscillator leading to simple RC chaos generators were introduced in [3, 4]. However, most of the proposed generators provide a voltage output signal which is less advantageous than a current output signal in terms of bandwidth and noise immunity. Moreover, current signals facilitate the design of many signal processing blocks such as adders, filters [5] and multipliers [6].

In this Letter, a new current mode sinusoidal oscillator, that uses the second generation current conveyor [7], is modified for chaos. A procedure based on the oscillator linear design equations is adopted for estimating all component values.

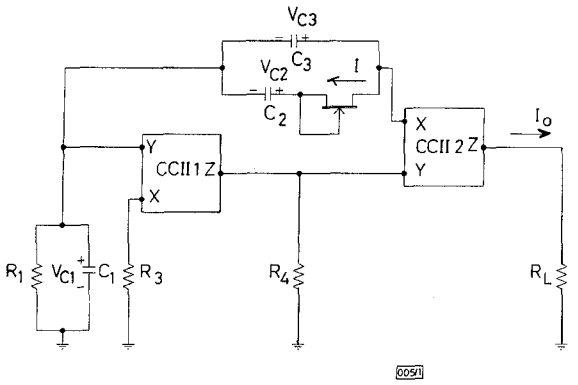

Fig. 1 *Proposed current mode chaos generator*

Circuitry and PSPICE simulations: The circuit shown in Fig. 1 represents the proposed chaos generator using a nonlinear resistor of antisymmetric current-voltage characteristics formed by a JFET operating in the triode region and requiring two CCII devices. If the JFET is replaced with a linear resistor R_2 and capacitor C_3 is eliminated, the sinusoidal oscillator circuit is retrieved, hence, the condition and frequency of oscillation are given, respectively, by

$$K = \frac{R_4}{R_3} = \frac{C_1}{C_2} + \frac{R_2}{R_1} + 1 \quad \omega_o = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \tag{1}$$

A simple design set is to take:

$$C_1 = C_2 = C \text{ and } R_1 = R_2 = R$$
$$\text{hence } K = 3 \text{ and } \omega_o = \frac{1}{RC} \tag{2}$$

In Fig. 1, adopting the design set of eqn. 2, resistor R_1 should be taken around the same value of the small signal resistance of the JFET at the operating point (R_J) and the sum of C_2 and C_3 should be equal to C_1. A JFET of the type J2N4338, which has a small signal resistance of 750Ω and a threshold voltage (V_T) of approximately –0.7V, is used. This JFET is especially suitable as a voltage controlled resistor. Fig. 2 represents a PSPICE simulation of the output current in a 1kΩ load and the V_{C1}–V_{C2} phase space trajectory with R_1 = 600Ω, R_3 = 1kΩ, R_4 = 3030Ω, C_1 = 2nF, C_2 = C_3 = 1nF and using the AD844A/AD as a CCII biased with ±9V. The generated signal has a chaotic broadband spectrum around the centre frequency ω_o estimated by eqn. 2.

Mathematical model and experimental results: It was found evident that the very small input resistance R_X of the CCII inverting input terminal X is responsible for stimulating the observed chaotic behaviour by allowing for a third rather than a second-order system to exist. This effect of R_X is associated with the device CCII 2 of Fig. 1. Other CCII and JFET parasitics were found to contribute little, thus the circuit is described by the following equation set:

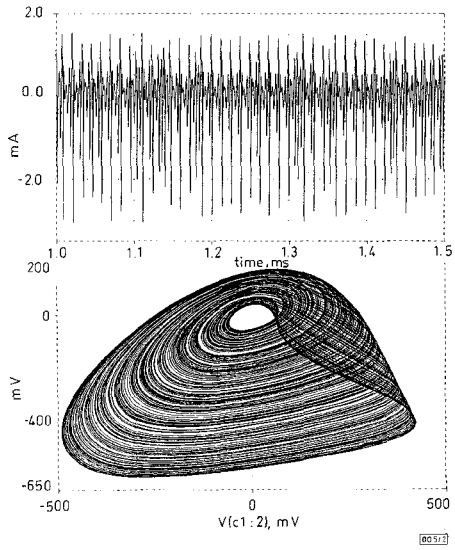

Fig. 2 *PSpice simulations of output current driving 1kΩ load and V_{C1}–V_{C2} phase space trajectory*

$$\begin{aligned} R_X C_1 \dot{V}_{C1} &= \left(K - 1 - \frac{R_X}{R_1}\right) V_{C1} - V_{C3} \\ C_2 \dot{V}_{C2} &= I \\ R_1 C_3 \dot{V}_{C3} &= R_1 C_1 \dot{V}_{C1} - R_1 C_2 \dot{V}_{C2} + V_{C1} \end{aligned} \tag{3}$$

Where I is the JFET current, approximated as:

$$I = \frac{1}{R_J} \begin{cases} (V_{C3} - V_{C2}) & (V_{C3} - V_{C2}) \geq V_T \\ V_T & (V_{C3} - V_{C2}) < V_T \end{cases} \tag{4}$$

The chaotic output current is given by

$$I_o = \frac{(K-1)V_{C1} - V_{C3}}{R_X} \tag{5}$$

Setting $X = V_{C1}/V_T$, $Y = V_{C2}/V_T$, $Z = V_{C3}/V_T$, $t_n = t/R_1C_1$, $K_1 = R_X/R_1$, $\varepsilon = C_2/C_1$, $\alpha = R_1/R_J$, and with $C_1 = C_2 + C_3$, the dimensionless form of eqns. 3 and 4 becomes:

$$\begin{aligned} \dot{X} &= \frac{1}{K_1}[(K - K_1 - 1)X - Z] \\ \dot{Y} &= \frac{\alpha}{\varepsilon} \begin{cases} (Z - Y) & (Z - Y) \leq 1 \\ 1 & (Z - Y) > 1 \end{cases} \\ \dot{Z} &= \frac{1}{(1-\varepsilon)}[\dot{X} - \varepsilon \dot{Y} + X] \end{aligned} \tag{6}$$

Although R_X (approximately 65Ω for the AD844) is a device parasitic, it is possible to add an external resistance in series with R_X and adjust design parameters accordingly. Numerical integration of eqn. 6 was carried out using a 0.005 step fourth-order Runge-Kutta algorithm. The obtained trajectory is shown in Fig. 3 with α = 0.8, ε = 0.5, K_1 = 0.1 and K = 2.87.

With simple manipulation, eqn. 6 can be rewritten in the following form:

$$\begin{bmatrix} \dot{X} \\ \dot{Y} \\ \dot{Z} \end{bmatrix} = \begin{bmatrix} \frac{K-K_1-1}{K_1} & 0 & \frac{-1}{K_1} \\ 0 & \frac{-a}{\varepsilon} & \frac{a}{\varepsilon} \\ \frac{K-1}{K_1(1-\varepsilon)} & \frac{a}{1-\varepsilon} & -\frac{a+\frac{1}{K_1}}{1-\varepsilon} \end{bmatrix} \begin{bmatrix} X \\ Y \\ Z \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{b}{\varepsilon} \\ -\frac{b}{1-\varepsilon} \end{bmatrix} \tag{7}$$

where

$$\begin{cases} a = \alpha & b = 0 \quad (Z - Y) \leq 1 \\ a = 0 & b = \alpha \quad (Z - Y) > 1 \end{cases}$$

For the parameter set (α, ε, K_1) = (0.8, 0.5, 0.1) and considering K as the bifurcation parameter, the Routh-Hurwitz criteria for

absolute stability applied to the Jacobian results in $K < 3.1$. For the choice of $K = 2.87$ the following eigenvalues are calculated:

$$\begin{cases} -6.8572, 0.678602 \pm j2.05088 & (Z-Y) \le 1 \\ 0, -1.15 \pm j4.32175 & (Z-Y) > 1 \end{cases}$$

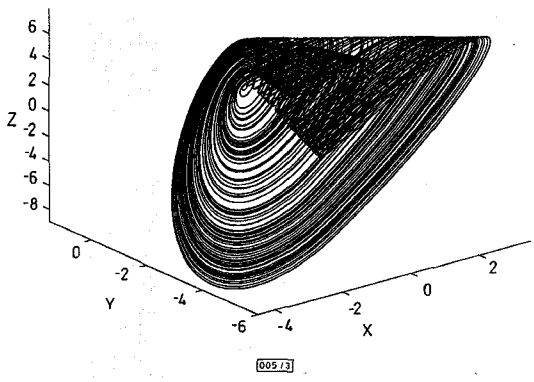

Fig. 3 *Trajectory obtained by solving eqn. 6*

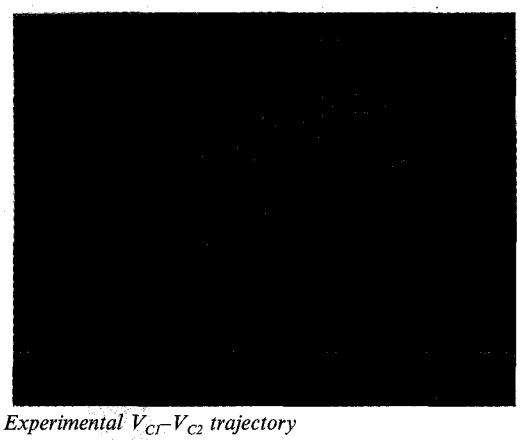

Fig. 4 *Experimental V_{C1}–V_{C2} trajectory*

The circuit was experimentally tested with $C_1 = 1$nF, $C_2 = C_3 = 0.5$nF, $R_3 = 1$kΩ, $R_4 = 5$kΩ pot., $R_1 = 1$kΩ pot. and a 1kΩ load. An experimental V_{C1}–V_{C2} trajectory is shown in Fig. 4. Tunability of the circuit is achieved by any or both of R_4 and R_1 through a period doubling route to chaos and loads up to 5kΩ could be driven. It is worth noting that the proposed chaos generator is suitable for VLSI integration. A CMOS CCII such as that in [5] can be used while the JFET can be replaced with a NMOS transistor.

Conclusion: A simple current mode RC chaos generator requiring two CCIIs, three capacitors, three grounded resistors and a floating nonlinear resistor was proposed.

13 August 1997
Electronics Letters Online No: 19971199

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Low-output-impedance class AB bipolar voltage buffer

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Indexing terms: Bipolar transistor circuits, Buffer circuits

A new ±1.5V class AB bipolar voltage buffer that can drive low load impedance is presented. A current compensation technique is used for achieving a low output impedance, resulting in a large unitary gain bandwidth and low distortion. Simulation results are included demonstrating the circuit performance.

Introduction: Voltage buffers play an essential role in most analogue electronic systems. Many applications based on current conveyors and operational amplifiers [1, 2] need high performance voltage buffers. To achieve high performances, low output resistance and high frequency unit gain bandwidth are the key parameters in designing voltage buffers. In CMOS technology, a solution that achieves low output resistance has been proposed [3]. Nevertheless, a high-speed bipolar process is more appropriate for high frequency applications. In this Letter, a low-output impedance bipolar voltage buffer is introduced without using composite active cells [4]. PSPICE simulation confirms the improved performance achieved by the proposed structure.

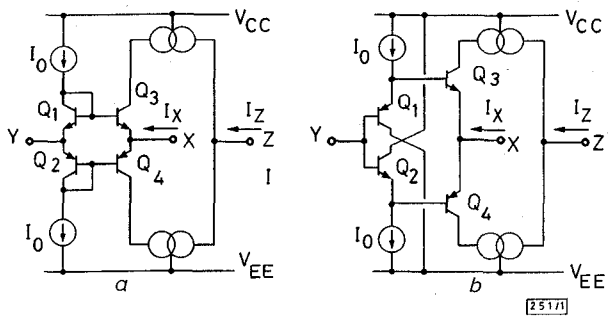

Fig. 1 *Traditional bipolar CCII(s)*
a Input emitter voltage buffer structure (EVB)
b Input base voltage buffer structure (BVB)

Traditional class AB voltage buffers and current conveyors: The two ordinary bipolar second generation current conveyors (CCII) based on traditional voltage buffer [1, 2] are shown in Fig. 1*a* and *b*. The two current mirrors copy the current I_X at node X through the current node Z ($I_Z = I_X$). The voltage buffer is then obtained between nodes Y and X (Y input). A single buffer is achieved by connecting, respectively, the collectors of Q_3 and Q_4 to the supply voltages V_{CC} and V_{EE}. These cells are also used to design the input and output stages of the high-speed current feedback operational amplifier (CFOA) [2].

Assuming that all transistors are in forward active mode, the collector and emitter currents can then be considered to be identical. The output resistance of the two traditional bipolar buffers [2, 4], the base voltage buffer (BVB) and emitter voltage buffer (EVB), is deduced from the transconductance of the output pair Q_3, Q_4:

$$R_x = k\frac{V_T}{I_0} \qquad (1)$$

where V_T is the thermal voltage and I_0 the bias current. $k = 1/2$ for the EVB and $k = (I_{SN}I_{SP})/(I_{SN}^2 + I_{SP}^2)$ for the BVB. I_{SN} and I_{SP} are the saturation currents of the transistors NPN and PNP, respectively. To obtain a low output resistance, a high bias current I_0 must be chosen. Unfortunately, this leads to an increase in power consumption.

Low-output impedance compensated voltage buffer (CVB): The proposed circuit shown in Fig. 2*a* is derived from the BVB shown in Fig. 1*b*. The DC current source I_0 supplies the bias for the diode connected transistors Q_5 and Q_6, and therefore biases all the other transistors in forward active mode [5]. Assuming that all transistors are identical and are operating at the same junction temperature, it follows [5] that