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High Accuracy Class AB CCII-

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Abstract: New CMOS realization of the negative-type second-generation current conveyor (CCII-) suitable for low power applications is presented. A dynamic biasing circuit is used to control the bias currents of the output stage and to provide class AB mode of operation. The proposed CCII- features high voltage tracking accuracy and low input impedance as a consequence of negative feedback. The compensation of the current tracking error between the X and the Z terminals is also introduced.

Keywords: Current conveyor, Voltage offset compensation, Class AB output stage

1. Introduction

The second generation current conveyor (CCII) proposed by Sedra and Smith in [1] has proven to be a useful building block for high frequency current mode applications. It presents an alternative way to implement analog systems, which traditionally have been based on the voltage op-amp (VOA). In many cases, the conveyor based applications feature enhanced performance over the VOA based applications in terms of accuracy and bandwidth. Recently, a great deal of attention has been directed toward designing high-performance current conveyors in terms of gain accuracy, impedance level, voltage and current offset as well as bandwidth [2–8].

Generally, the CMOS realizations used to implement the CCII can be classified onto two categories according to the output current driving capability. The first category comprises class A CCII realizations, which are generally used as input stage of other operational current mode building blocks. In this case, the output of the class A CCII is connected to a high impedance node with no need for high-drive capability [5]. On the other hand, class AB CCII realization with high-drive capability is required when low load resistances are to be used [7].

Recently, a class A CCII- featuring high accuracy voltage and current transfer gains was presented [8]. This realization was based on using the floating current source (FCS) output stage introduced in [9]. Although the output stage used results in high current tracking accuracy, it operates in class A mode of operation which increases the power comsumption and makes the CCII- realization unsuitable for applications requiring high current driving capabilities. In this paper, a new CMOS realization of the CCII- is introduced. Low power consumption is provided by modifying the FCS output stage to operate in Class AB mode of operation. The proposed design features low input impedance as well as high voltage tracking accuracy between the Y and the X terminals. Two compensation techniques are then described in order to cancel the current tracking error between the X and the Z terminals.

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2. The proposed class AB CCII-

2.1 The input stage

The circuit configuration of the proposed class AB realization is shown in Fig. 1. The input stage formed by (M1–M5) is the popular long tail differential pair (LTDP) and it is used to generate a current signal proportional to the voltage difference between the Y and the X terminals. The intermediate gain stage (M6–M10) is used to simultaneously force the output current of the LTDP at a constant voltage level, which is independent of the variations in the input voltage at the Y terminal. Taking the channel length effect into consideration, the voltage offset between the X and the Y terminals can be written as:

$$V_{\text{xoff}} = V_x - V_Y \approx \left(\frac{\lambda_1+\lambda_3}{2}\right)\left(1+\frac{\lambda_3}{4}\sqrt{\frac{I_{D5}}{K_3}}\right) \times \left(\sqrt{\frac{I_{D5}}{K_3}}-\sqrt{\frac{2I_{D6}}{K_6}}\right)\sqrt{\frac{2I_{D2}}{K_2}} \quad (1)$$

Where $K = \mu C_{\text{ox}}\frac{W}{L}$ and λ_i is the channel length modulation parameter of the i^{th} transistor.

From (1), the necessary condition for voltage offset cancellation is given by:

$$\frac{I_{D6}}{I_{D5}} = \frac{K_6}{4K_3} \quad (2)$$

It is seen that the voltage offset between the Y and the X terminals is independent of the input voltage level. Moreover, the current flowing through M3 and M6 are constant bias currents and any mismatch between them will result in a constant voltage offset.

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The proposed CCII- features low input impedance at the X terminal that is given by:

$$r_x = \frac{g_{d10} + \frac{(g_{d1}+g_{d3}+g_{d9})(g_{d6}+g_{d8})(g_{d7}+g_{d10})}{g_{m6}g_{m7}}}{g_{m1}\left(\frac{g_{m11}+g_{m13}}{2} + \frac{g_{d15}+g_{d17}}{4}\right)} \approx \frac{2g_{d10}}{g_{m1}(g_{m11}+g_{m13})} \quad (3)$$

Where g_{mi} and g_{di} are the transconductance and the output conductance of the i^{th} transistor respectively.

As given by (3), r_x can be reduced by increasing the output impedance of M10 this can be achieved by replacing M10 by two cascode transistors.

2.2 Class AB mode of operation

The class AB output stage of the CCII- shown in Fig. 1 is a modified version of the class A FCS stage introduced in [9]. Transistors M11 through M18 and the bias current I_B form the basic FCS. Generally, this output stage provides high current tracking accuracy between the X and the Z terminals as long as the upper and lower bias currents flowing through M15 and M17 are matched. In order to provide class AB mode of operation, the dynamic biasing circuit formed from M19 through M22 is used to control the level of the basic FCS upper and lower bias currents. Assuming that the two CMOS pairs M19–M20 and M21–M22 are matched and neglecting the current offsets of the two current mirrors M16–M15 and M18–M17, the currents flowing through M15 and M17 can be written as follows:

$$I_{D15} \approx I_{D17} = \begin{cases} I_B + \frac{K_{\text{eff }19,20}}{2}\left[V_{G11}^2 + (\nabla V)^2\right] & (4a) \\ \forall\, |V_{G11}| \le \nabla V & \\ I_B + \frac{K_{\text{eff }19,20}}{2}(V_{G11} + \nabla V)^2 & (4b) \\ \forall\, V_{G11} > \nabla V & \\ I_B + \frac{K_{\text{eff }21,22}}{2}(-V_{G11} + \nabla V)^2 & (4c) \\ \forall\, V_{G11} < -\nabla V & \end{cases}$$

where $\nabla V = V_c - V_{\text{Teff}}$, $K_{\text{eff }i,j}$ is the effective transconductance parameter of the CMOS pair formed from the i^{th} and the j^{th} transistors and it is equal to $\frac{\sqrt{K_i}\sqrt{K_j}}{\sqrt{K_i}+\sqrt{K_j}}$, V_c is the control voltage and V_{G11} is the input voltage to the FCS stage and it is approximately related to the input current I_x according to the following relation:

$$I_x \approx \left[\frac{\sqrt{K_{11}I_{D15}} + \sqrt{K_{13}I_{D17}}}{2}\right] V_{G11} \quad (5)$$

From (4) and (5), it is seen that the modified FCS bias currents are proportional to the square of the input current level I_x. If current is withdrawn from the X terminal the gate voltage of M11 and M13 is lowered. Thus, the currents flowing through transistors M11 and M14 decrease while those flowing through M12 and M13 increase. Similarly, if the X terminal is required to sink current, the gate voltage of M11 and M13 is increased causing the currents through transistors M11 and M14 to increase and that through M12 and M13 to decrease. Hence, a push-pull action is provided at the X terminal using transistors M11 and M13. A similar push-pull action is provided by M12 and M14 at the Z terminal.

Assuming equal currents flow through M15 and M17, the summation of the four currents flowing through M11–M14 is constant and equal to zero for any input current value, hence, a negative copy of the input current (I_x) is transferred to the Z terminal. When the input current level is increased (in the inward direction), the drain voltages of M15 and M17 are increased. The maximum input current value in the linear range is reached when the source to drain voltage drop across M17 is less than $V_{SD,Sat}$. In this case, the upper bias current is not correctly transferred to M17 and the condition needed for providing the negative current copy is no longer valid. Similarly, the minimum input current value reached when the drain to source voltage drop across M15 is less than $V_{DS,Sat}$.

From (4) and (5) and assuming that the current mirrors M15–M16 and M17–M18 are matched current mirrors with negligible current offsets, the standby current flowing through the output transistors (M11–M14) at zero

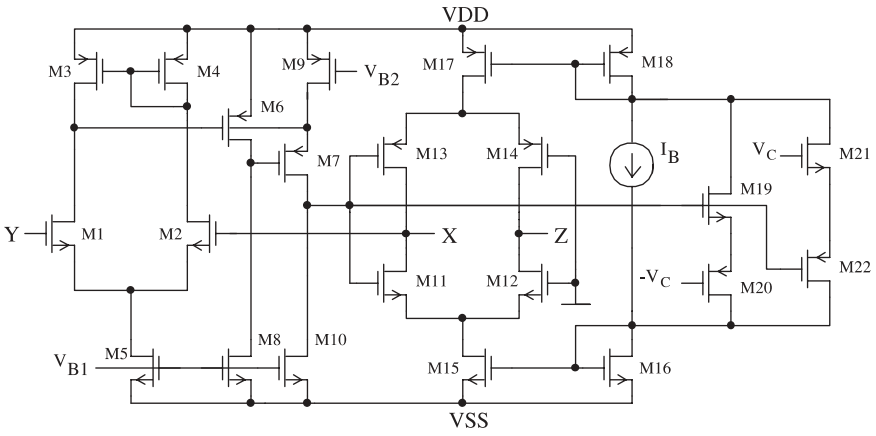


Fig. 1. The proposed class AB CCII- realization.

input current is given by:

$$I_{SB} = \frac{I_B}{2} + \frac{K_{\text{eff }19,20}}{4}(V_c - V_{\text{Teff}})^2 \tag{6}$$

Hence, the standby power dissipation can be controlled using the bias current I_B as well as the control voltage V_c.

2.3 Current transfer gain characteristics

Using small signal analysis, and assuming that M11 and M13 are matched to M12 and M14 respectively, the current transfer gain between the X and the Z terminals can be written as:

$$A_i = \frac{i_Z}{i_X} \approx -\left(\frac{1-\alpha}{1+\alpha}\right) \tag{7}$$

where α is approximately given by:

$$\begin{aligned}\alpha \approx \frac{1}{g_{m11}+g_{m13}} \Bigg\{ & \frac{g_{d15}+g_{d17}}{2} \\ & + \left(\frac{g_{m19}g_{m20}}{g_{m19}+g_{m20}} - \frac{g_{m21}g_{m22}}{g_{m21}+g_{m22}}\right) \\ & \times \left(\frac{g_{m15}}{g_{m16}} - \frac{g_{m17}}{g_{m18}} - \frac{g_{m15}g_{d15}}{g_{m16}g_{m11}} + \frac{g_{m17}g_{d17}}{g_{m18}g_{m13}}\right)\Bigg\}\end{aligned} \tag{8}$$

From (7) and (8), it can be inferred that the output stage used in the proposed CCII- of Fig. 1 results in a current transfer gain very close to unity since the term α is much smaller than unity. As given by (8), the mismatches between M15 and M16 and those between M17 and M18 have negligible effects on the current gain as long as both CMOS pairs M19–M20 and M21–M22 have close effective transconductances. The current tracking error is also affected by the output conductances of M15 and M17. However, errors due to mismatches and finite conductances can be reduced by using large values for g_{m11} and g_{m13}.

In the realization of Fig. 1, the current offset between the input and output currents is dependent on the matching between the lower and upper bias currents flowing through M15 and M17 respectively. When there is a constant offset between these two bias currents, constant offset current results at the output at the CCII- without affecting the linearity of the current transfer gain. However, the presence of an offset current dependent on the input current level affects the linearity of the current transfer gain and hence, increases the distortion in the output current signal.

Referring to the CCII- realization shown in Fig. 1, the current offset between the X and Z terminals can be evaluated as follows:

$$I_{\text{zoff}} = I_z + I_x = I_{11} + I_{12} - (I_{13} + I_{14}) = I_{15} - I_{17} \tag{9}$$

Hence, the output current offset between the X and Z terminals depends on the circuit used to bias the four output transistors (M11–M14). In the realization of Fig. 1, the simple current mirrors used to bias M15 and M17 result in a current offset due to the channel length modulation effect. Assuming that each of the two current mirrors (M15–M16) and (M17–M18) is formed of matched transistors, i.e. $I_{15} = I_{16}$ and $I_{17} = I_{18}$, the output offset current can be written as:

$$\begin{aligned} I_{\text{zoff}} &= I_{15} - I_{16} - (I_{17} - I_{18}) \\ &= I_B[\lambda_{15}(V_{D15} - V_{D16}) - \lambda_{17}(V_{D18} - V_{D17})] \end{aligned} \tag{10}$$

Where V_{Di} is the drain voltage of the i^{th} transistor.

Both V_{D16} and V_{D18} in (10) are constants and independent of the input current level, however, V_{D15} and V_{D17} are related to the input current at the X terminal by the following relation:

$$\begin{aligned} I_x \approx \frac{K_{11}}{2}(V_{G11} - V_{D15} - V_{Tn})^2 - \frac{K_{13}}{2} \\ \times (V_{D17} - V_{G11} - |V_{Tp}|)^2 \end{aligned} \tag{11}$$

From (10) and (11), it is seen that the offset current between the X and Z terminals is dependent of the input current level, hence, resulting in a current tracking error and affecting the linearity of the current transfer gain.

3. Current tracking error compensation

From (10), the current tracking error between the X and Z terminals can be compensated by cancelling the voltage differences $(V_{D15} - V_{D16})$ and $(V_{D17} - V_{D18})$. This can be achieved by modifying the output stage so that the drain voltages of M15 and M17 are transferred with unity gain to the drains of M16 and M18 respectively.

3.1 First current tracking error compensation technique

A possible implementation of this compensation technique is shown in Fig. 2. The unity feedback circuits between the gates and drains of M16 and M18 in Fig. 1 are replaced by high-gain differential amplifiers (M23–M26 and M27–M30) connected in closed loop configurations as shown in Fig. 2. The gates of M16 and M18 are connected to the output nodes of the two amplifier circuits in order to provide the voltage buffering at the drains of M16 and M18. Referring to Fig. 2, the small signal drain voltages of M16 and M18 are given by:

$$\begin{aligned} v_{d16} &= \frac{v_{d15}}{1 + \dfrac{(g_{d16} + g_B \,||\, g_{d18})(2g_{m26}g_{d23})}{g_{m16}g_{m23}(2g_{m26} + g_{d23})}} \\ &\approx \frac{v_{d15}}{1 + \dfrac{g_{d16}g_{d23}}{g_{m16}g_{m23}}} \end{aligned} \tag{12}$$

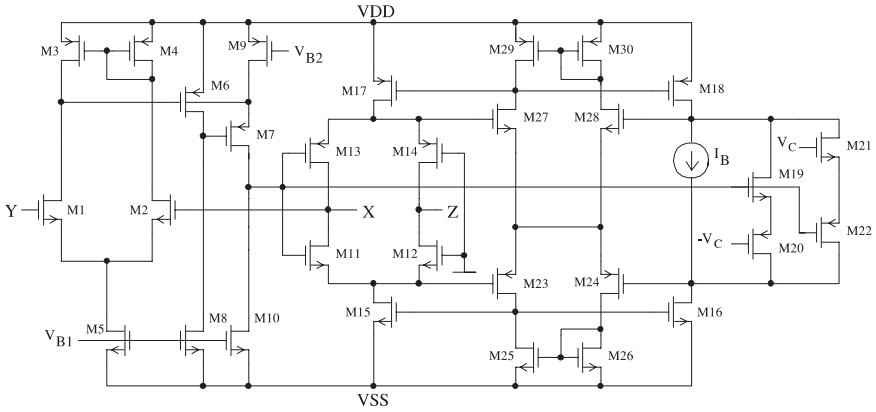


Fig. 2. The class AB CCII- realization using first current tracking error compensation technique.

$$v_{d18} = \frac{v_{d17}}{1+\dfrac{(g_{d18}+g_B \,||\, g_{d16})(2g_{m30}g_{d27})}{g_{m18}g_{m27}(2g_{m30}+g_{d27})}} \approx \frac{v_{d17}}{1+\dfrac{g_{d18}g_{d27}}{g_{m18}g_{m27}}} \tag{13}$$

Where g_B is the output conductance of the bias current I_B in Fig. 2.

From (12) and (13), it is seen that any voltage changes at the drain of M15 and M17 are transferred to the drains of M16 and M18 respectively with voltage gain very close to unity. In this case, the current offset given by (10) can be rewritten as follows:

$$I_{\text{zoff}} = I_B\left[\frac{\lambda_{15}(\lambda_{23}+\lambda_{25})}{2}\left(\sqrt{\frac{I_B}{2K_{16}}}-\sqrt{\frac{I_{D24}}{2K_{24}}}\right) - \frac{\lambda_{17}(\lambda_{27}+\lambda_{29})}{2}\left(\sqrt{\frac{I_{D28}}{2K_{28}}}-\sqrt{\frac{I_B}{2K_{18}}}\right)\right] \tag{14}$$

Where I_{D24} and I_{D28} are given by:

$$I_{D24} = I_{D28} = \frac{K_{\text{eff }28,24}}{2}(V_{D17}-V_{D15}-V_{\text{Teff}})^2 \tag{15}$$

By comparing (10) with (14), it can be easily shown that the offset current is reduced by order of λ over the whole input range. Hence, enhancing the current tracking accuracy and the linearity of the current transfer gain between the X and Z terminals.

3.2 Second current tracking error compensation technique

From (11) and (15) it is can be shown that the currents flowing through the compensation circuit (M23–M30) are dependent on the input current to the X terminal (I_x). In order to overcome this drawback, two independent long tail bias currents (I_{D31} and I_{D32}) are used to bias the two amplifier circuits (M23–M26 and M27–M30) as shown in Fig. 3. In this case, the necessary conditions for current tracking error compensation are given by:

$$\frac{I_{D31}}{I_B} = 2\frac{K_{25}}{K_{15}} \tag{15a}$$

$$\frac{I_{D32}}{I_B} = 2\frac{K_{30}}{K_{17}} \tag{15b}$$

Since, the current flowing through M31 and M32 are constant bias currents, the conditions given by (15a) and (15b) can be satisfied over the whole input current range. Since the power dissipation of the compensation circuit is controlled by the bias currents flowing through M31

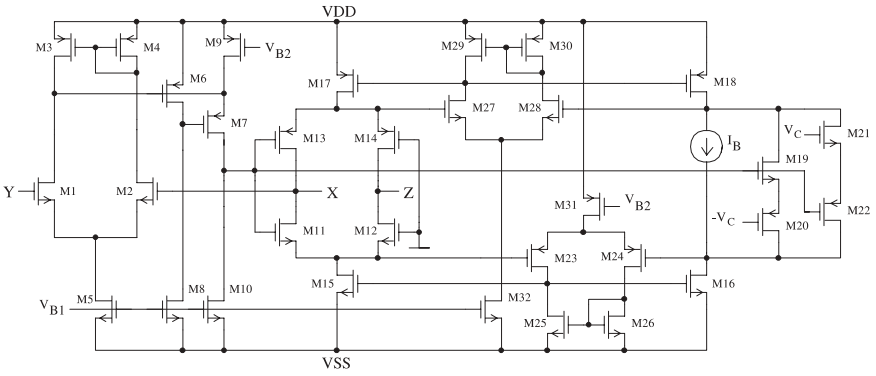


Fig. 3. The class AB CCII- realization using second current tracking error compensation technique.

and M32, it is advantageous to make the ratios K_{25}/K_{15} and K_{30}/K_{17} smaller than unity. In this case, small bias currents can be used to bias M31 and M32 and hence, reducing the power consumption of the CCII- realization of Fig. 3.

4. Simulation results

PSpice simulations are carried out with model parameters of 1.2 μm CMOS process provided by MOSIS (AMI). The supply voltages are equal to ±2.5 V. V_c is set to 2.5 V while I_B is set to 1 μA. V_{B1} and V_{B2} are equal to −1.65 and 1.27 V respectively. The three CCII- realizations of Figs. 1 through 3 are simulated using the dimensions given in Table 1. Simulation results of the CCII- of Figs. 1–3 are given in Table 2.

The standby current flowing through M16 and M18 is equal to 50 μA. The variation of this current with respect to the input current is shown in Fig. 4(a). The push-pull actions provided by M12–M14 and M13–M14 are shown in Figs. 4(b) and 4(c) respectively. Fig. 5(a) shows the offset current variations with respect to the input current I_x for realizations of Figs. 1 through 3 while Fig. 5(b) shows the variations of the current transfer gain (A_i) with respect to the input current (I_x). It is seen that the modified class AB CCII- realizations of Figs. 2 and 3 feature negligible

Table 1. Transistor aspect ratios of the class AB CCII- realizations of Figs. 1–3.

Transistor	W(μm)/L(μm)	Transistor	W(μm)/L(μm)
M1, M2	30 / 3.6	M17, M18	90 / 3.6
M3, M4, M6, M7	90 / 3.6	M19, M21	180 / 2.4
M5	384 / 3.6	M20, M22	120 / 2.4
M8	192 / 3.6	M23, M24	90 / 2.4
M9, M10	18 / 3.6	M25, M26	24 / 3.6
M11, M12	30 / 2.4	M27, M28	30 / 2.4
M13, M14	90 / 2.4	M29, M30	24 / 3.6
M15, M16	240 / 3.6	M31, M32	72 / 3.6

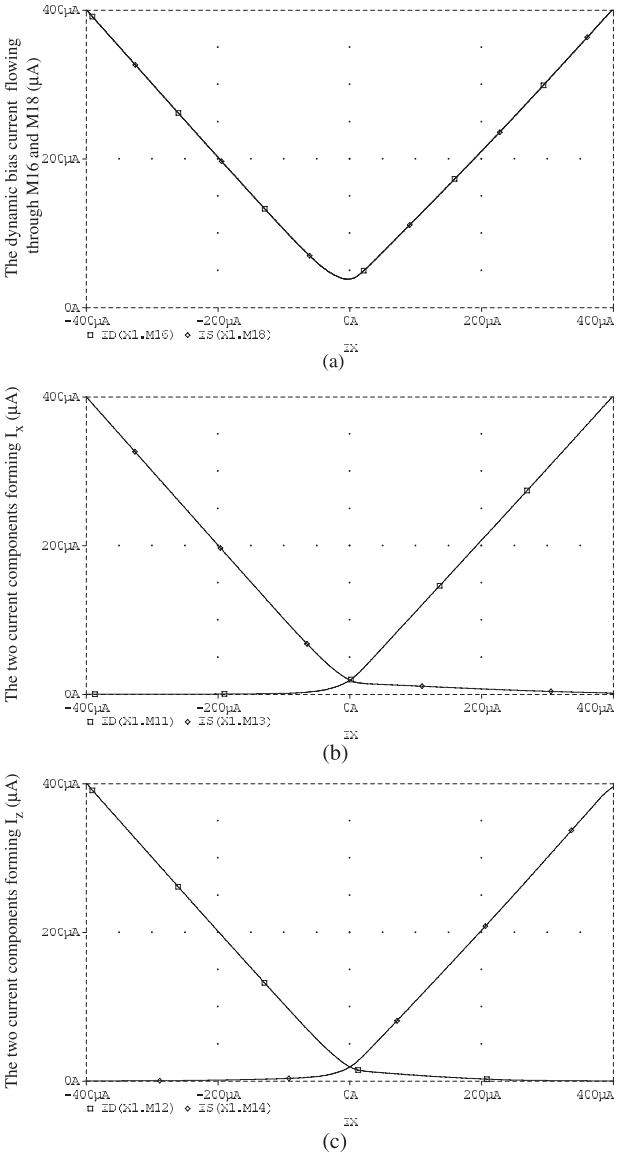
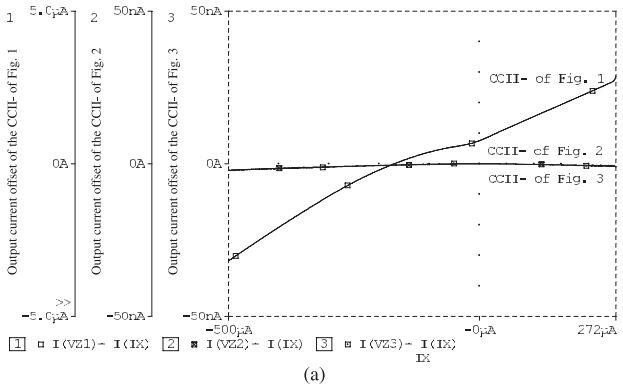


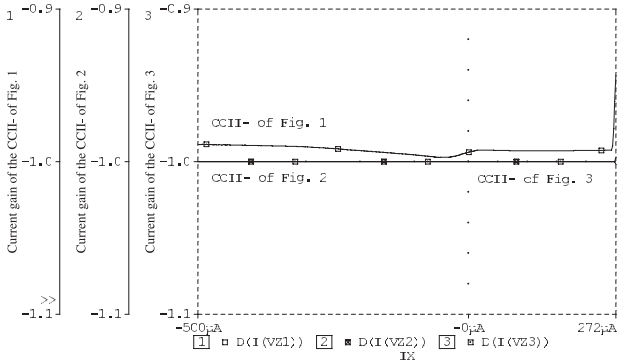
Fig. 4. Variations of the currents flowing through the output stage transistors with respect to the input current I_x for the class AB CCII- of Fig. 1.

Table 2. Simulation results of the class AB CCII- realization of Figs. 1–3.

CCII- Parameter	CCII- of Fig. 1	CCII- of Fig. 2	CCII- of Fig. 3	Unit
A_i	−54	−0.001	0.002	mdB
Input current linear range	−500 to 270	−500 to 270	−500 to 270	μA
I_{zoff}	758	0.09	−0.13	nA
Maximum deviation from I_{zoff}	2.2	0.002	0.002	μA
f_{3db} (for I_z)	58	47	50	MHz
Standby current flowing through M16 and M18	50	50	50	μA
A_v	158	158	158	μdB
Input voltage linear range	−1.8 to 2.1	−1.8 to 2.1	−1.8 to 2.1	V
V_{xoff}	−99	−99	−99	μV
Voltage tracking error compensation range	−0.9 to 2.1	−0.9 to 2.1	−0.9 to 2.1	V
f_{3db} (for V_x)	90	90	90	MHz
r_x	0.35	0.35	0.35	Ω



(a)



(b)

Fig. 5. (a) Variations of the output current offset (I_{zoff}) with respect to the input current (I_x) for the three CCII- realizations of Figs. 1–3. (b) Variations of the current transfer gain (A_i) with respect to the input current (I_x).

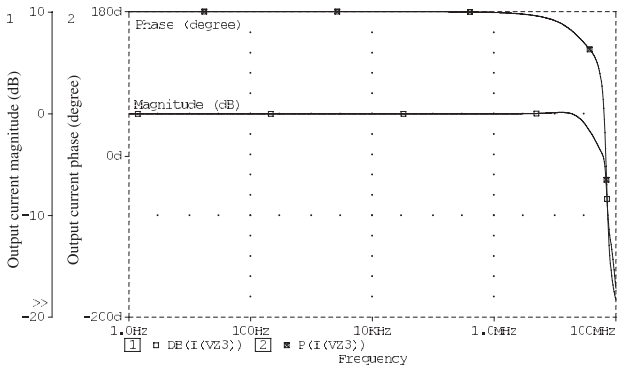


Fig. 6. AC transfer characteristics between the X and Z terminals for the class AB CCII- of Fig. 3.

current offsets and highly linear current gain compared to the uncompensated CCII-. The frequency response of the output current at the Z terminal of the CCII- of Fig. 3 is shown in Fig. 6. The current transfer gain bandwidth is equal to 50 MHz.

The DC voltage transfer characteristics between the Y and X terminals are shown in Fig. 7. Voltage tracking error cancellation is obtained over the range (−0.9 to 2.1 V).

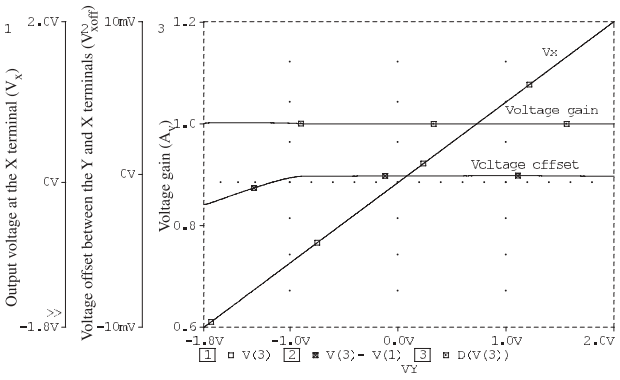


Fig. 7. DC transfer characteristics between the Y and X terminals for the class AB CCII- of Fig. 3.

Table 3. THD percentage values of the output current for the three CCII- realizations with the input current $I_x = 250\,\mu$A.

Frequency	THD (%)		
(kHz)	Fig. 1	Fig. 2	Fig. 3
10	0.1	0.01	0.026
100	0.12	0.01	0.054
200	0.15	0.03	0.09
500	0.26	0.17	0.29
1000	0.66	0.43	0.61

The offset voltage (V_{xoff}) in this range is equal to $-99\,\mu$V. The voltage transfer gain between the Y and X terminal has a bandwidth equal to 90 MHz.

Table 3 shows the THD percentage values obtained when a sinusoidal input signal of 250 μA is applied at the X terminal of each of the three CCII- realizations of Figs. 1–3. The input frequency is varied over a range of 10 kHz to 2 MHz. Realizations of Figs. 2 and 3 feature negligible THD values at low frequencies. The three realizations have THD values smaller than 0.7% at 1 MHz.

5. Conclusions

Novel class AB CCII- realization suitable for low-power applications was presented. The proposed design is based on using dynamic bias currents in the output stage so that the current level in the output transistors is proportional to the level of the input current to the X terminal. The attractive property of the proposed design is that the standby current can be controlled using an external control voltage. Voltage offset cancellation was provided by controlling the ratio between two bias currents. The paper also presented two designs for current tracking error cancellation. The two modified designs are supe-

rior to the basic design in terms of current offset, gain and total harmonic distortion. PSpice simulations were included and showed that the presented CCII- realizations feature high-performance in terms of voltage and current transfer characteristics as well as input impedance level.

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