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Letter

Low-Voltage Low-Power CMOS RF Four-Quadrant Multiplier

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Abstract: This paper describes a CMOS four-quadrant multiplier intended for use in the front-end receiver by utilizing the square-law characteristic of the MOS transistor in the saturation region. The circuit was simulated in standard 0.5 μm CMOS level 3 MOSIS (BSIM3 SPICE-based). The mixer has a third-order inter modulation (IM3) of 34.7 dBmV, a third-order intercept point (IP3) of −5.7 dBm, 1-dB compression (P-1dB) of −10.4 dBm and the power consumption is 1.18 mW from a single 1.5 V power supply. One of the features of the proposed design is using two MOS transistors limitation to reduce the supply voltage, which leads to reduce the power consumption.

Keywords: RF-Mixer, Front-End, GSM, GPS, WLAN

1. Introduction

As wireless products such as cellular phones, global system for mobile communications (GSM), global positioning satellite (GPS), wireless local area network (WLAN) ... etc became an every day part of people's lives. The need for higher performance at low costs and low power consumption becomes even more important. An important block in the receiver and transmitter is the mixer. The nonlinear device in the proposed design is the squarer.

In this paper a full CMOS four-quadrant analog multiplier is presented. It is an important building block in the radio frequency (RF) Front-End. The second section of this paper describes the design of the presented CMOS four-quadrant analog multiplier. The third section of this text describes the Mixer performance. Simulation results are given to verify the theoretical analysis.

2. Mixer design

Recently several multipliers have been presented using bipolar process such as presented in [1–3], using four matched symmetrical junction field-effect transistors (JEFTs) operating in the triode region [4], realized in a BiCMOS process [5], and circuits implemented in CMOS process [6–13]. The proposed circuit was designed aimed on the square-algebraic identity in the MOS transistor as many CMOS analog multiplier, were developed in literature [14–15] and many of mixers summaries on [16].

The proposed multiplier based on the four squarer is shown in Fig. 1, which consists of four pMOS transistors operated in saturation region. The voltage $V_{\mathbf{a}}$ consists of two components DC and AC and the $V_{\mathbf{a}}{}^{-}$ has the same DC component but negative AC and the same thing applies on $V_{\mathbf{b}}$ and $V_{\mathbf{b}}{}^{-}$. The drain current of each transistor can be expressed as

$$I_{D1} = \frac{K_1}{2}\left(V_{DD} - V_a - V_T\right)^2 \tag{1}$$

$$I_{D2} = \frac{K_2}{2}\left(V_{DD} - V_a^- - V_T\right)^2 \tag{2}$$

$$I_{D3} = \frac{K_3}{2}\left(V_{DD} - V_b - V_T\right)^2 \tag{3}$$

$$I_{D4} = \frac{K_4}{2}\left(V_{DD} - V_b^- - V_T\right)^2 \tag{4}$$

Where

$$K_1 = K_2 = K_3 = K_4 = K$$
$$K = \mu C_{OX}\frac{W}{L}$$

And

$$V_a = V_1^+ \_ V_2^-, \qquad V_b = V_1^- \_ V_2^-$$
$$V_1^+ = V_{DC1} + v_1, \qquad V_1^- = V_{DC1} - v_1$$
$$V_2^+ = V_{DC2} + v_2, \qquad V_2^- = V_{DC2} - v_2$$

From Eqn. (1) and Eqn. (2) taking into account the DC biasing

$$\begin{aligned} I_1 &= I_{D1} + I_{D2} \\ &= \frac{K}{2}\Big\{2\,(V_{DD} + V_{DC2} - V_{DC1} - V_T)^2 \\ &\quad + 2{v_1}^2 + 2{v_2}^2 + 4v_1v_2\Big\} \end{aligned} \tag{5}$$

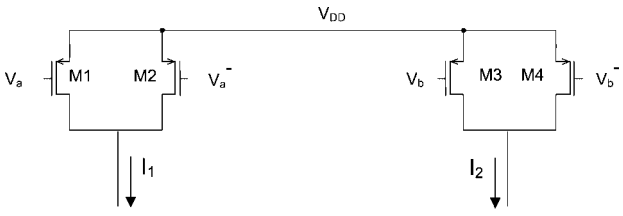

Fig. 1. The Four MOS Transistor Squarer.

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From Eqn. (3) and Eqn. (4)

$$\begin{aligned} I_2 &= I_{D3} + I_{D4} \\ &= \frac{K}{2}\Big\{2\big(V_{DD} + V_{DC2} - V_{DC1} - V_T\big)^2 \\ &\quad + 2{v_1}^2 + 2{v_2}^2 - 4v_1v_2\Big\} \end{aligned} \tag{6}$$

Thus one can obtain the following equation

$$I_1 - I_2 = 4Kv_1v_2 \tag{7}$$

The operation of the proposed four-quadrant multiplier in Fig. 2 is similar to that of the squarer in Fig. 1, where the transistor M9-M10, M11-M12, M13-M14 and M15-M16 are operating in saturation region as subtraction devices.

For transistors M9-M10, M11-M12, M13-M14 and M15-M16 to work in the saturation region the following biasing conditions should be satisfied:

$$V_{DS10} \geq V_2^- - V_{T10} \tag{8}$$

$$V_{DD} - V_{DS10} \geq V_1^- - V_{DS10} - V_{T9} \tag{9}$$

$$V_{DD} + V_{T9} \geq V_1^{\pm} \geq 2V_2^{\pm} - V_{T10} \tag{10}$$

The transistors M5-M6 and M7-M8 works as two linear resistors as described in [17]. Where

$$\begin{aligned} &K_5 = K_6 = K_7 = K_8 = K_R, \\ &V_{T5} = V_{T6} = V_{T7} = V_{T8} = V_{TR} \\ &R = \frac{2}{K_R(V_B - 2V_{TR})} \end{aligned} \tag{11}$$

Then the differential output of the multiplier is

$$V_O = 4RKv_1v_2 \tag{12}$$

The conversion gain is

$$G_C = 4RKv_2 \tag{13}$$

Non-ideal Effect:

1. Body Effect:

The effect of V_{SB} on the channel can most conveniently represented as change in the threshold voltage V_T [18].

$$V_T = V_{T0} + \gamma\left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right] \tag{14}$$

Which will affect only the transistors M9, M12, M13 and M16

For $V_{DS10} < \phi_f$

Then the differential output is

$$V_O = \frac{4RKv_1v_2}{\left(1 + \frac{\gamma}{2\sqrt{2\phi_f}}\right)^2} \tag{15}$$

And the conversion gain is

$$G_C = \frac{4RKv_2}{\left(1 + \frac{\gamma}{2\sqrt{2\phi_f}}\right)^2} \tag{16}$$

For V_2 is the LO frequency equal to 1 GHz-carrier frequency and V_1 the input signal with frequency equal to 75 MHz. The simulation result in the time domain of 1 GHz local oscillator (LO), 75 MHz input signal shown and the mixer output signal, the LO is amplitude modu-

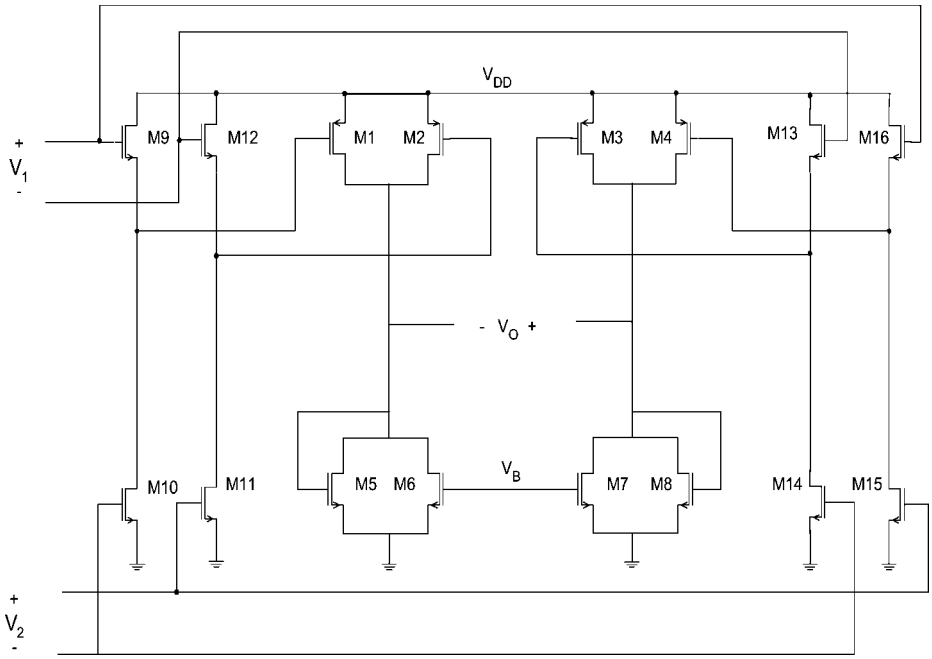

Fig. 2. The Multiplier.

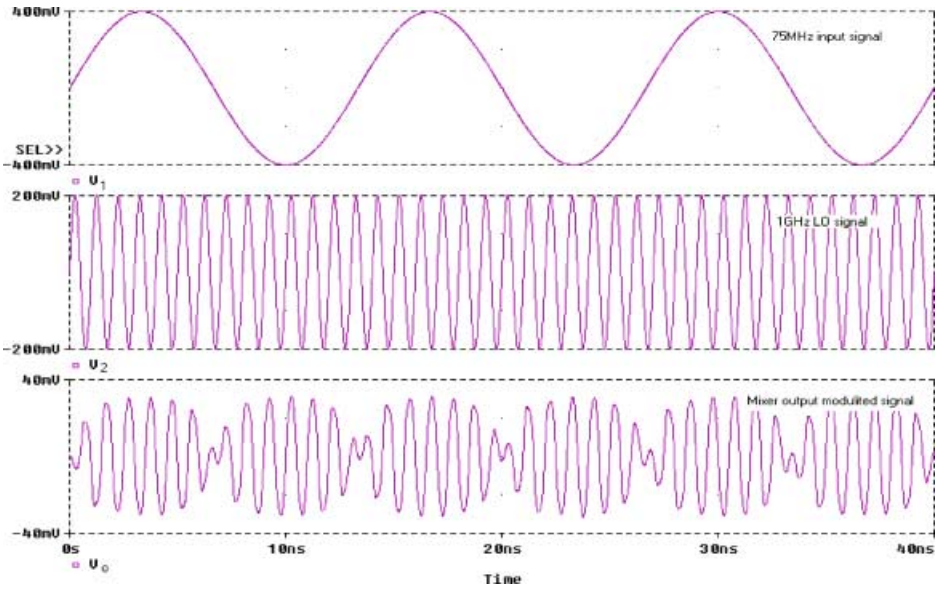

Fig. 3. The Time Domain Simulation.

lated by 75 MHz-shown in Fig. 3. The simulation results are summarized in Table 1 and discussed in detail below. The mixer was simulated in stander 0.5 μm where aspects ration as shown in Table 2.

3. Mixer performance parameter

The parameters that affect the receiver performance can be divided into four categories as presented in [19]. *Sensitivity, Selectivity, Overloading* and *Power consumption* which all depends on the mixer performance parameters. The performance parameters of the presented down-conversion mixer as follows by using SPICE simulator [20] and the curve fitting and extrapolation using MATLAB [21]

Table 1. Simulated parameter.

Supply voltage	1.5 V
Power dissipation	1.18 mW
RF input frequency	975 MHz
LO frequency	900 MHz
1-dB conversion	− 10.4 dBm
Input IP3 (third-order intercept point)	− 5.7 dBm
IM3 (third-order intermodulation)	34.7dB mV

Table 2. Aspect ratio W/L.

Transistor	Aspect ratio μm/μm
M1-M4	18/0.5
M5-M8	5/0.5
M9-M18	10/0.5

A. Gain Compression:

A strong signal can saturate the mixer and reduce its power gain. The input 1-dB compression point ($P_{-\mathbf{1dB}}$) measures the input power level that causes the mixer to deviate from the linear magnitude response by 1-dB [19]. The magnitude response of the presented down-conversion mixer is shown in Fig. 4(b). From simulation, extrapolation and curve fitting the $P_{-\mathbf{1\,dB}} = -10.4$ dBm where "dBm" is the signal power referenced to 1 mW and expressed in dB.

B. Third-Order Intermodulation Distortion:

Due to the odd-order nonlinearity in the transfer function of the mixer, two undesired signals in the adjacent channels generate third-order intermodulation (IM3) products at the output of the mixer one of the IM3 product can corrupt the desired signal if it falls within the desired channel [19]. Fig.4(a) shows the magnitude responses of the desired signal and the IM3 product. The (-o-) lines are the magnitude response of the down-conversion and the (-*-) lines are the IM3 lines. Which simulated by two strong unwanted signals and using extrapolation. The intersection between the two lines determines the input power (the third-order intercept point (IP3)). The third-order intermodulation distortion is used for measure the third-order nonlinearity. IP3 = − 5.7 dBm and the output at this point is IM3 = 34.7 dBmV, where "dBmV" is the signal voltage referenced to 1 mV and expressed in dB. And "dBm" is the signal power referenced to 1 mW and expressed in dB.

Power Consumption:

Today the present goal is to reduce the power consumption, which lead to increase the battery used time and the cost as well [22]. The power consumption reduction is one of the requirements today; one of ways to achieve this is to reduce the supply voltage. In the presented design

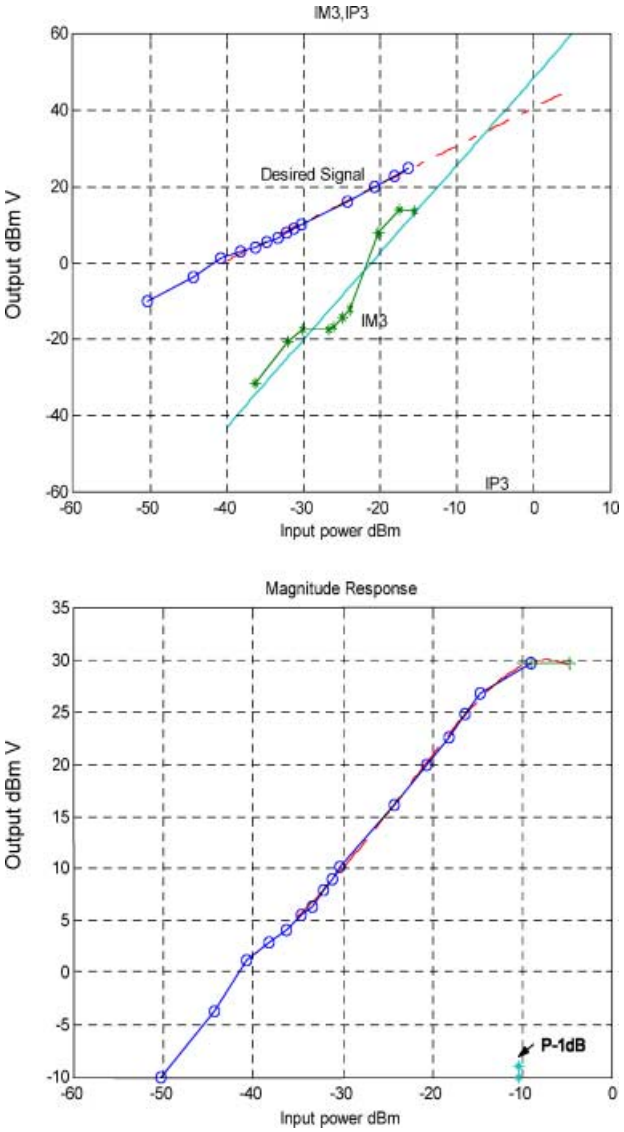

Fig. 4. (a) The Third-Order Intermodulation Distortion. (b) The Magnitude Response.

using the two MOSFET transistors limitation to reduce the supply voltage to 1.5 V that leads to reduce the power consumption and using a battery for long time. The power consumption of the presented down-conversion mixer is 1.18 mW from a 1.5 V single supply.

4. Conclusion

A low voltage CMOS four-quadrant analog multiplier based on square-algebraic identity in the MOS transistor in the saturation region was presented. Using two MOS transistors limitation to reduce the supply voltage that leads to reduce the power consumption, which is essential today to increase the battery life time on most applications. The mixer simulated in standard 0.5 μm. The simulated parameters are shown in Table 1. The mixer parameter was discussed also, and summarized in Table 2. The low voltage Low power CMOS four-quadrant analog multiplier presented here is useful in RF signal processing applications, in the front-end transceiver. The circuit presented here is compared with other circuits in terms of performance and results are summarized in Table 3.

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Table 3. Comparison.

Parameter	Salama and Soliman (Presented)	Crols and Steyaert [10]	Shahani. Shaeffer and T. H. Lee [11]	Meyer and Mack [5]	Sullivan, Xavier and W. H. Ku [23]
Supply voltage	1.5 V	5 V	1.5 V	5 V	3 V
Power dissipation	1.18 mW	1.3 mW	–	–	–
LO frequency	900 MHz	1.5 GHz	1.40042 GHz	900 MHz	1.8 GHz
1-dB conversion	– 10.4 dBm	-	- 5 d B m	–3 dBm	–8 dBm
Input IP3 (Third-order intercept point)	-5.7dBm	45.2dBm	10dBm	-	0dBm
IM3 (Third-order intermodulation)	34.7 dBmV	– 46.4 dB	–	6 dBm	–
Technology	0.5 μm CMOS	1.2 μm CMOS	0.35 μm CMOS	QUBiC BiCMOS 0.8 μm CMOS	0.6 μm CMOS

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