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Generation, modeling, and analysis of CCII-based gyrators using the generalized symbolic framework for linear active circuits

Ramy A. Saad*,† and Ahmed M. Soliman

Electronics and Communications Engineering Department, Cairo University, Giza 12613, Egypt

SUMMARY

In this paper, CCII-based gyrators are synthesized, modeled, and analyzed using the generalized symbolic framework for linear active circuits. The systematic synthesis method using admittance matrix expansion, included in the framework, is applied to generate optimized nullor–mirror descriptions for the gyrator. The resulting CCII-based circuit representations for the gyrators, obtained from mapping nullor–mirror pairs in the ideal realizations with equivalent second-generation current conveyors (CCIIs), can be classified into two topologies according to the type of the CCII terminals handling the gyrator input and output signals. In topology I, the gyrator input and output terminals are CCIIs Y–Z-terminals, whereas in topology II, the gyrator input and output terminals are CCIIs X-terminals. The parasitic components within the synthesized circuits, associated with the actual CCIIs, are modeled and included in their expanded admittance matrices. Exact non-ideal analysis for two circuits belonging to the two topologies, involving the reduction of their expanded admittance matrices to port admittance matrices, is then carried out to investigate the practical functional performance for these circuits at their ports. The non-ideal performance analysis based on the CCII actual parasitic elements indicates that, from a practical perspective, the CCII-based gyrator circuits belonging to topology I are more efficient and suitable for the gyrator applications than those belonging to topology II in terms of bandwidth and operation at high frequencies. SPICE simulations are included to demonstrate the analytical results for the comparison between the practical performances of the two circuit topologies. Copyright © 2007 John Wiley & Sons, Ltd.

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KEY WORDS: gyrator; nullor; pathological element; synthesis; analysis; modeling; current conveyor; simulated inductor

1. INTRODUCTION

In [1–4], the foundations of the generalized framework for linear active circuits used in this paper were laid down. This framework encompasses circuit synthesis, modeling, and ideal and non-ideal

*Correspondence to: Ramy A. Saad, Electronics and Communications Engineering Department, Cairo University, Giza 12613, Egypt.
†E-mail: saad.ramy@gmail.com

analysis. The systematic synthesis method starts from the $p \times p$ port admittance matrix describing a certain circuit function. This port matrix is to be expanded to an $n \times n$ nodal admittance matrix (NAM) describing the circuit to be synthesized, such that $n > p$. The matrix expansion process takes place firstly by applying pivotal expansion [1], which is the reverse operation of the Gaussian elimination, to all matrix elements including products and quotients of admittance terms; until every element in the admittance matrix become a single admittance term representing a single circuit element. Then, extra blank rows and columns, representing internal nodes, are introduced in the resulting matrix, and nullor–mirror elements (shown in Figure 1) are used to move matrix elements to their final locations, correctly describing either floating or grounded passive elements. Thus, the final NAM is obtained including finite elements representing passive circuit components and unbounded elements, the so-called infinity variables, representing nullor–mirror elements.

In the generalized framework, the ideal representation of analog circuits employs nullor–mirror elements to describe active elements [5–7]. Nullor–Mirror elements are pathological elements that possess ideal characteristics and are specified according to the constraints they impose on their terminal voltages and currents. For the nullator $V = I = 0$, while the norator imposes no constraints on its voltage and current. A nullator–norator pair constitutes a universal active element [8] called the nullor (shown in Figure 2), and hence, nullators and norators are called nullor elements. For the voltage mirror $V_1 = -V_2$ and $I_1 = I_2 = 0$, while for the current mirror $I_1 = I_2$ without constraints on the values of the currents or the voltages. Thus, voltage and current mirrors are used to represent the voltage and current mirroring actions, respectively, and hence, they are called mirror elements.

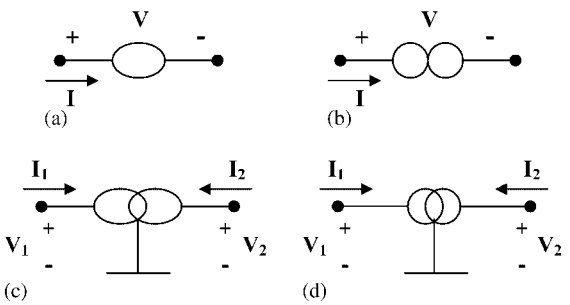

Figure 1. Nullor–mirror elements: (a) nullator; (b) norator; (c) voltage mirror; and (d) current mirror.

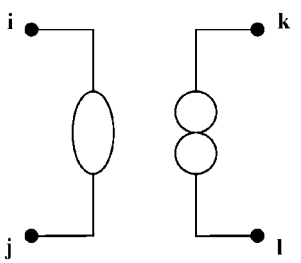

Figure 2. Nullor with a nullator connected between nodes i and j and a norator connected between nodes k and l.

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The attractive feature of the pathological elements is their ability to model active circuits independently of the particular realization of the active devices with the possibility of generating a number of ideally equivalent circuits from which the best practical ones can thereafter be selected [7, 9, 10]. The NAM representation can be easily converted to a symbolic nullor–mirror realization ideally describing the active circuit to be synthesized. In a physically realizable circuit, all the voltages and currents are always uniquely and definitely determined. This in turn implies that in the ideal representation of a physically realizable circuit, the nullator (or the voltage mirror) and the norator (or the current mirror) must occur in a pair. Hence, the nullor–mirror elements in a symbolic ideal description are grouped into pairs, with each one or more pairs describing a certain active device. Then, a synthesized circuit can be obtained by mapping the pathological elements pairs with equivalent actual active devices.

Parasitic elements and non-ideal effects within an active circuit, associated with its components and building blocks, can be modeled and included in the NAM describing the circuit. Non-ideal analysis can thereafter be performed through the reduction of the resulting NAM, using Gaussian elimination, to the port admittance matrix describing the circuit function, and hence, performance measures (like input impedance, voltage gain, and current gain) at the ports of the circuit can be evaluated to investigate the actual performance of the circuit.

The paper is focused on the generation, modeling, and analysis of CCII-based gyrators using this generalized framework for active circuits. The generated CCII-based gyrator circuits can be classified into two topologies according to the type of the CCIIs terminals acting as gyrator input and output. In topology I, the input and output terminals of the gyrator are $Y-Z$-terminals of CCIIs. On the other hand, topology II is characterized by having the gyrator input and output terminals as CCIIs X-terminals. Circuits belonging to the two topologies will be used to obtain grounded inductance simulators. The two topologies will be compared according to the actual performances of their corresponding realized inductors. A detailed non-ideal analysis will be carried out, considering the actual parasitic components of practical CCIIs [11, 12]. SPICE simulations will be performed to demonstrate the difference in performance between the two topologies, and the results will be shown to agree with the analytical conclusions.

In Section 2, two classes of optimized ideal representations for the gyrator using pathological elements are generated, and CCII-based active circuit realizations for the gyrator are then obtained by converting the nullor–mirror pairs in the ideal descriptions into equivalent CCIIs, resulting in two different circuit topologies according to the type of the CCIIs terminals acting as gyrator input and output. The two gyrator circuit topologies are compared through a detailed non-ideal analysis for their performances, considering the CCIIs associated parasitic components, when used to realize grounded inductance simulators, in Section 3. In Section 4, SPICE simulations are used to demonstrate the analytical results deduced in Section 3. Finally, conclusions are drawn in Section 5.

2. SYSTEMATIC SYNTHESIS OF CCII-BASED ACTIVE GYRATORS

The positive impedance inverter (PII), the so-called gyrator, is one of the most useful building blocks of active network synthesis, used to realize grounded and floating inductors. The realization of op-amp gyrators by means of nullors and resistors has been presented in [13–15]. As a current-mode active device, the current conveyor (CC) provides several advantages, such as greater linearity and wider bandwidth, over voltage-mode active devices such as op-amps [16, 17]. There are numerous

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publications on the realization of active gyrators using CCs, for example, [18–21]. In this section, CCII-based gyrator circuit realizations will be generated using the generalized systematic synthesis method for active circuits [1–4].

2.1. Generation of the gyrator nullor–mirror descriptions

It is known that the gyrator can be described by the following transmission relationship between its terminal voltages and currents:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & B \\ C & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{1}$$

This can be easily converted into the following form:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & \pm G_1 \\ \mp G_2 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2}$$

where G_1 and G_2 are transconductance elements. Thus, the two-port admittance matrices for the gyrator are given by

$$Y = \begin{bmatrix} 0 & \pm G_1 \\ \mp G_2 & 0 \end{bmatrix} \tag{3}$$

For the ideal gyrator, which must be lossless, $G_1 = G_2$.

A gyrator port admittance matrix, with positive and negative sign combination taken for the matrix locations of G_1 and G_2, respectively, can be expanded to a NAM, as shown in (4). To reach this expansion for this 2×2 port admittance matrix, blank rows and columns three and four are introduced, then nullor–mirror elements are used to invest their associated equivalence transformations [1, 4]. To get the element G_1 on the diagonal, so that to represent a grounded passive element, a nullator is used to move G_1 to the position 1,3 and a norator is used to move G_1 to the on-diagonal position 3,3. In order to convert the element $-G_2$ in 2,1 to an on-diagonal positive element, a nullator is used to move $-G_2$ to the position 2,4, and a current mirror is used to move $-G_2$ to the on-diagonal position 4,4 and change its sign. Thus, G_2 become a positive element existing on the diagonal. The resulting expanded matrix is shown in (4), with the added nullor–mirror elements represented by bracket notation for nullors and mirrors [1, 4].

$$\begin{bmatrix} 0 & G_1 \\ -G_2 & 0 \end{bmatrix} \equiv \overbrace{\left\{\left[\begin{matrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & -G_2 \end{matrix}\right]\right\}} \tag{4}$$

The nullor–mirror equivalent circuit for the gyrator described by the NAM in (4) is shown in Figure 3(a). Hence, applying all possible combinations of the added nullor–mirror elements, starting from the gyrator port admittance matrices in (3), to realize a gyrator with two different pairs of pathological elements and two grounded resistors, will yield the eight equivalent nullor–mirror

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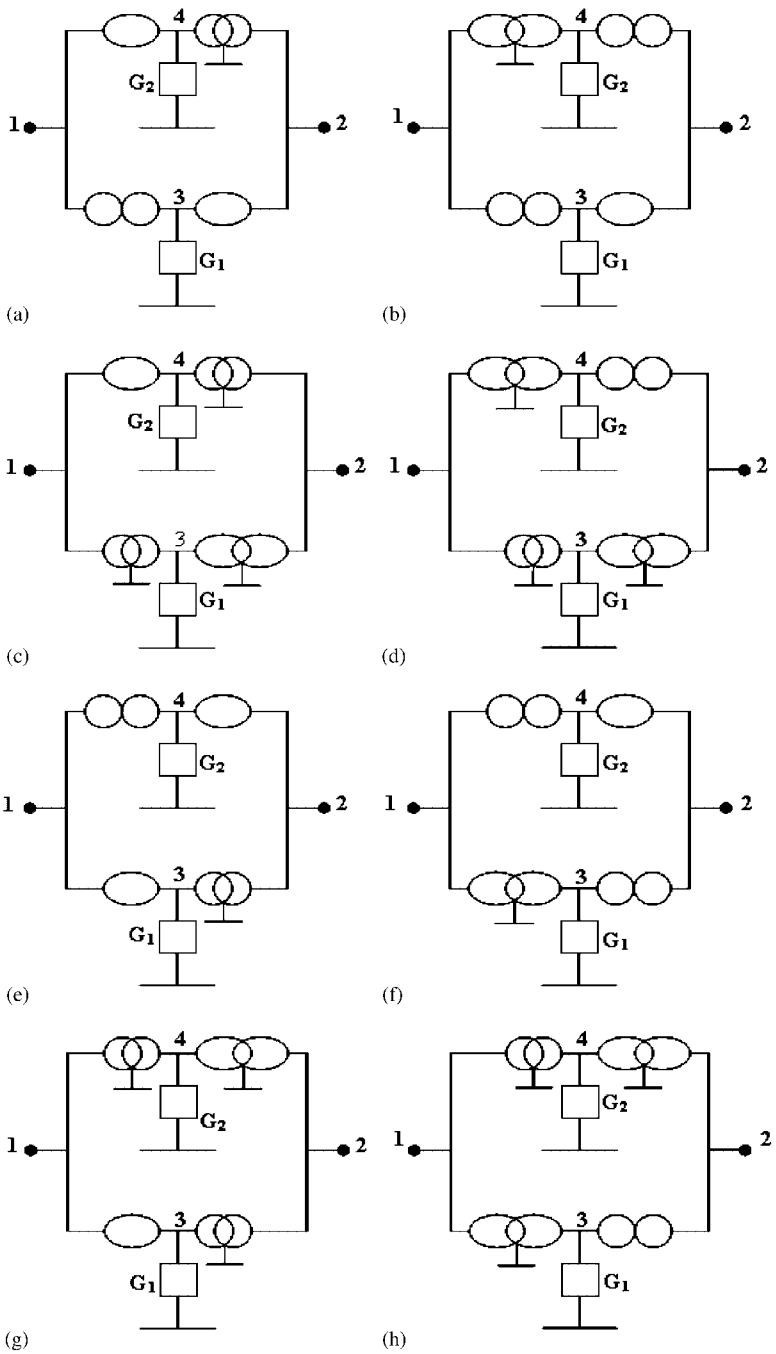

Figure 3. Gyrator nullor–mirror representations with two different pairs of pathological elements and two grounded conductances.

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circuits shown in Figure 3. This class of nullor–mirror gyrator representations offers an optimized realization in terms of the number of active devices. On the other hand, if two active devices are to be used in the actual circuit realization, they must be of different types.

Another class of nullor–mirror realizations for the gyrator, that include three similar pathological pairs, one floating resistor, and one grounded resistor, can be obtained from the admittance matrices in (3) by making more expansion steps. This can be achieved in general by performing the matrix expansion using single type of voltage pathological elements (nullator or voltage mirror) to move elements between columns, and using single type of current pathological elements (norator or current mirror) to move elements between rows. Consider the same gyrator port admittance matrix used in (4), with positive and negative signs combination taken for the matrix locations of G_1 and G_2, respectively. Blank rows and columns 3–5 are introduced. To obtain the element G_1 on the diagonal, so that to represent a grounded passive element, a nullator is used to move G_1 to the position 1,3 and a norator is used to move G_1 to the on-diagonal position 3,3. The negative element $-G_2$ will be employed in the representation of a floating passive element as follows. A nullator is used to obtain the $-G_2$ term from the position 2,1 to the position 2,4. Then a norator is used to move $-G_2$ to the position 4,5. Extra nullator and norator will be used then to retrieve the missing terms from the columns and rows, respectively, corresponding to the ground node. Hence, the resulting $\pm G_2$ terms describe a floating G_2 element. The expanded matrix is shown in (5), with the added nullor elements represented by bracket notation.

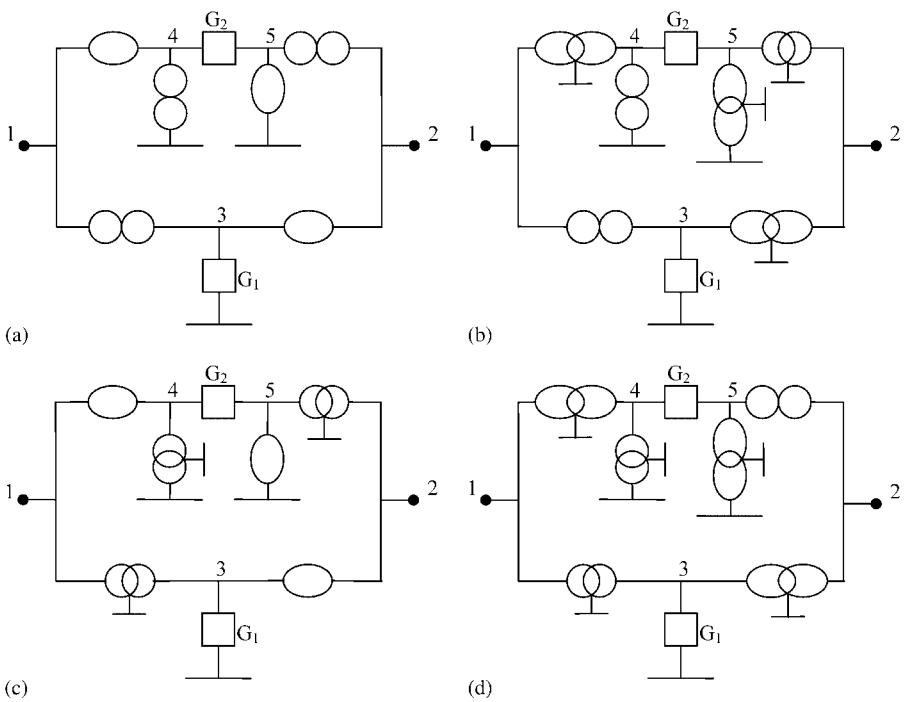

Figure 4. Gyrator nullor–mirror representations with three identical pairs of pathological elements; one grounded conductance and one floating conductance.

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$$\begin{bmatrix} 0 & G_1 \\ -G_2 & 0 \end{bmatrix} \equiv \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1 & 0 & 0 \\ 0 & 0 & 0 & G_2 & -G_2 \\ 0 & 0 & 0 & -G_2 & G_2 \end{bmatrix} \tag{5}$$

The nullor equivalent circuit for the gyrator described by the NAM in (5) is shown in Figure 4(a). It is clear that this ideal description contains similar pathological pairs. Hence, applying all possible combinations of the added nullor–mirror elements, starting from the gyrator port admittance matrices in (3), while maintaining the condition of using single type of voltage pathological

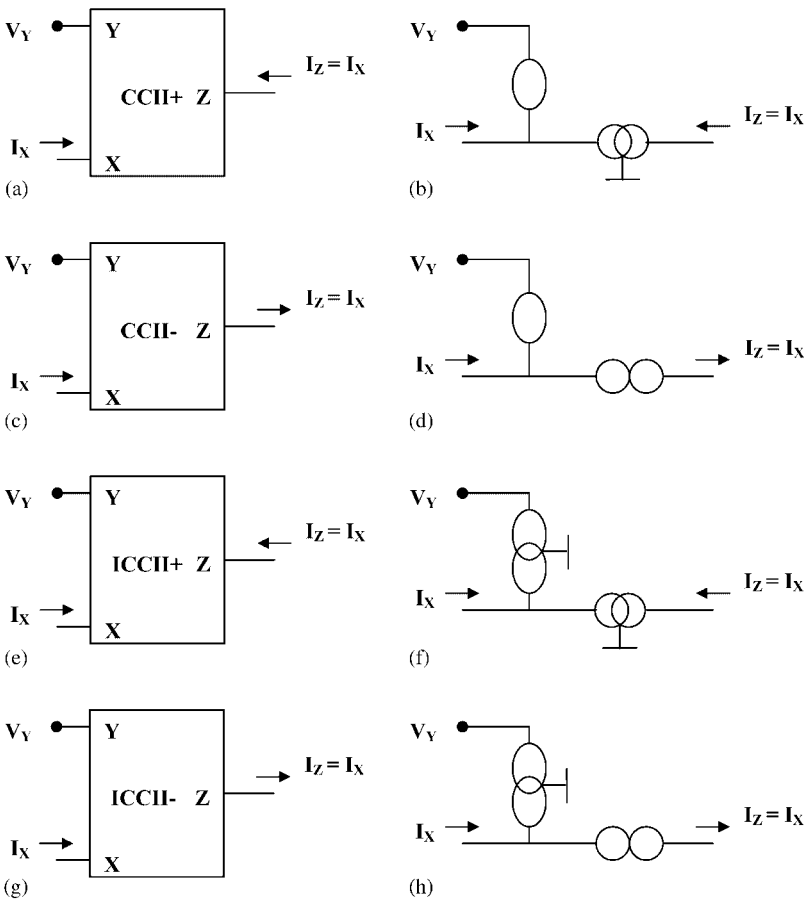

Figure 5. (a) The CCII+ symbol, (b) the CCII+ nullor–mirror representation, (c) the CCII− symbol, (d) the CCII− nullor–mirror representation, (e) the ICCII+ symbol, (f) the ICCII+ nullor–mirror representation, (g) the ICCII− symbol, and (h) the ICCII− nullor–mirror representation.

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elements (nullator or voltage mirror) for moving elements between rows and using single type of current pathological elements (norator or current mirror) for moving elements between rows throughout the expansion, will yield the four equivalent nullor–mirror circuits shown in Figure 4. This class of nullor–mirror gyrator representations offers the option of using similar active devices at the expense of increasing their number by 1. This can be helpful to profit from the characteristics of high-performance active devices by using them to realize the whole circuit. Besides, it can be of great importance when there is a requirement to use a particular component that is commercially available.

2.2. Converting gyrator nullor–mirror realizations into CCII-based circuits

CCIIs with all their types (CCII+, CCII−, ICCII+, and ICCII−) are versatile building blocks, and can be ideally represented using nullor–mirror elements [7, 11]. The symbols and the corresponding nullor–mirror representations for the four types of the CCII are shown in Figure 5 [7]. Hence, the gyrator nullor–mirror circuits in Figures 3 and 4 can be easily converted into equivalent CCII-based circuits, by mapping appropriate pairs of pathological elements with the equivalent CCII devices.

Since in Figures 3 and 4, pathological elements are connected in continuous loops, they can be paired as CCs in two alternative ways, resulting in two circuit topologies for CCII-based gyrators. In topology I, the gyrator input and output terminals are CCIIs Y–Z-terminals, whereas

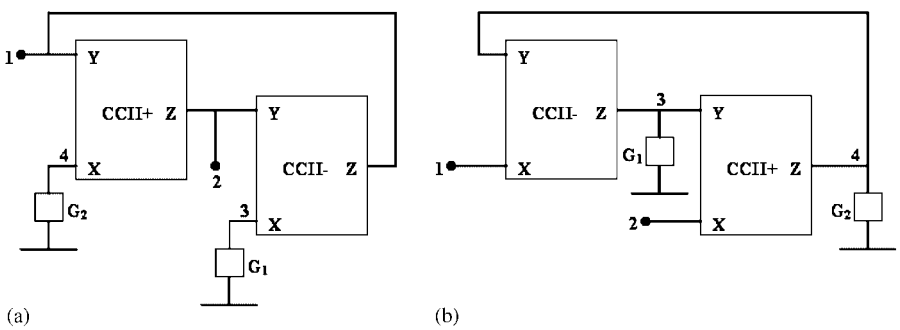

Figure 6. CCII-based gyrators with two different CCIIs and two grounded conductances: (a) Y–Z input/output terminals and (b) X input/output terminals.

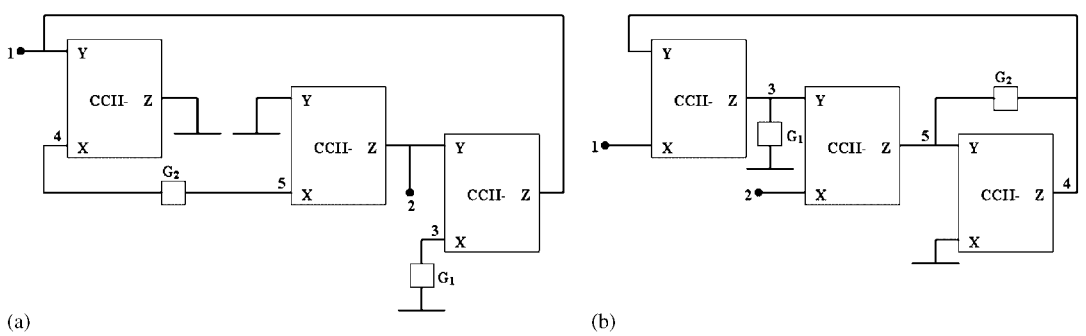

Figure 7. CCII-based gyrators with three similar CCIIs; one grounded conductance and one floating conductance: (a) Y–Z input/output terminals and (b) X input/output terminals.

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in topology II, the gyrator input and output terminals are CCIIs X-terminals. For example, if the gyrator nullor–mirror realization of Figure 3(a) is to be converted into CCII-based active circuit, then the pathological elements can be paired in two ways, resulting in the two CCII-based circuits in Figure 6. Although, these two circuits are ideally equivalent in terms of functional operation, but from a topological perspective, they differ according to the specifications of their input and output terminals. For the circuit in Figure 6(a), the input and output terminals of the gyrator are Y–Z-terminals of the CCIIs, thus they are high impedance terminals. While for the circuit in Figure 6(b), the input and output terminals are X-terminals of the CCIIs, which are low impedance terminals. Besides, the parasitic elements experienced at each type of CCII terminals are different. Similarly, Figure 7 shows the two CCII-based realizations for the nullor-mirror circuit of Figure 4(a), and they are belonging to the two topologies specified above.

In the next two sections, a detailed performance analysis will take place to compare the two gyrator circuit topologies considering the CCII parasitic elements, and the actual operation of the two topologies will be verified using SPICE simulations, to demonstrate the results of the analytical investigation.

3. ACTUAL PERFORMANCE ANALYSIS FOR THE TWO CCII-BASED GYRATOR CIRCUIT TOPOLOGIES

In order to perform analytical performance comparison between the two CCII-based gyrator circuit topologies, circuits that belong to the two topologies and realized using the same CCII types will be used. Consider the two CCII-based gyrator circuits in Figure 6(a) and (b), which belong to topologies I and II, respectively. These two gyrator circuits can be used to realize simulated grounded inductors by connecting a grounded capacitor C at terminal 2 of each gyrator, as shown in Figure 8. The resulting two simulated grounded inductors are ideally equivalent; however, non-ideal effects associated with the actual CCIIs change the impedance of the simulated inductance.

Actual CCIIs possess non-idealities represented in (i) non-unity frequency-dependent voltage and current transfer gains from Y to X and from X to Z, respectively, (ii) offset voltage difference between X and Y terminals, and offset current difference between X and Z terminals, (iii) signaling limitations on voltages and currents at the terminals of the CCII, and (iv) parasitic impedance

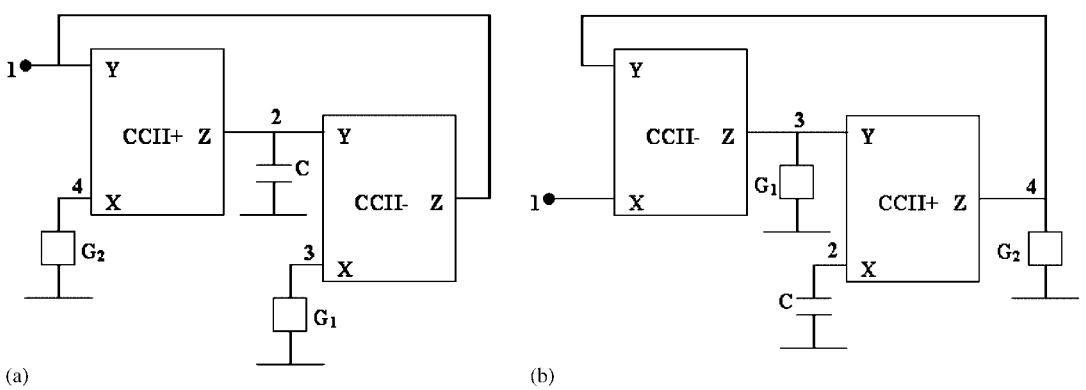

Figure 8. Simulated grounded coils using the CCII-based gyrators in Figure 6.

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components at the CCII terminals. Considering all these CCII non-ideal attributes in analyzing CCII-based circuits provides an accurate prediction for the performance of practical designs. From Figures 6 and 7, it is clear that the CCII-based gyrator circuits belonging to the two topologies have the same direct connections between the terminals of the used CCIIs, and the only difference is in the locations of the gyrator input and output terminals and actual passive components. Therefore, the effect of the non-ideal transfer gains, offsets, and limited signaling at the CCII terminals on the performances of circuits belonging to the two topologies is almost the same, and mainly determined by the CCIIs used in the circuit design. That is, the effect of these non-idealities on the performances of the circuits belonging to the two topologies has a limited sensitivity to the circuit topology. However, the effect of the parasitic impedance components at the CCII terminals on the circuit performance is highly sensitive to the circuit topology. This is because the interconnections between the terminals of the CCIIs and the passive components in the design determine to which extent the actual passive components will absorb the effect of the parasitic components associated with the CCIIs. Since the main concern in this section is the comparison between the performances of two circuit topologies using similar devices, only the parasitic impedances at the CCIIs terminals are to be considered in the following analysis.

3.1. Analysis

The actual CCII parasitic components can be included in the CCII symbolic representation as shown in Figure 9, where the parasitic conductances of the CCII appear in series at the X-terminal and in parallel at the Z-terminal, and the parasitic capacitances appear in parallel at the Y- and Z-terminals. Thus, the simulated grounded inductance circuits in Figure 8, including the CCII parasitic impedance components, become as shown in Figure 10. The significance of node numbering in this diagram is such that newly introduced nodes by the parasitic components are attached to the CCIIs, while the input port and the actual passive elements maintain their original nodes, because these parasitic components are associated with the CCIIs.

In contrast to the infinity variable notation [1, 4], bracket notation is not a mathematical notation and thus it is not suitable for analysis. Hence, the infinity variable notation is used to represent nullor–mirror elements in the NAM throughout the analysis. The parasitic impedance components associated with the CCIIs can be modeled and easily included in the NAM, so that to perform non-ideal analysis for a practical design [2, 3]. Gaussian elimination steps are performed thereafter to reduce the resulting NAM, yielding a final 1×1 port admittance matrix. Thus, the input admittance for a simulated grounded inductor circuit, considering the CCIIs actual parasitic impedances, is obtained.

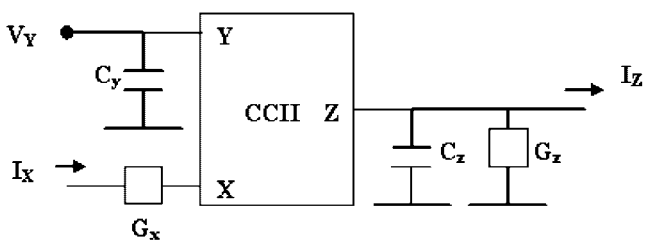

Figure 9. CCII symbolic representation including a modeling for the parasitic impedance components at the CCII terminals.

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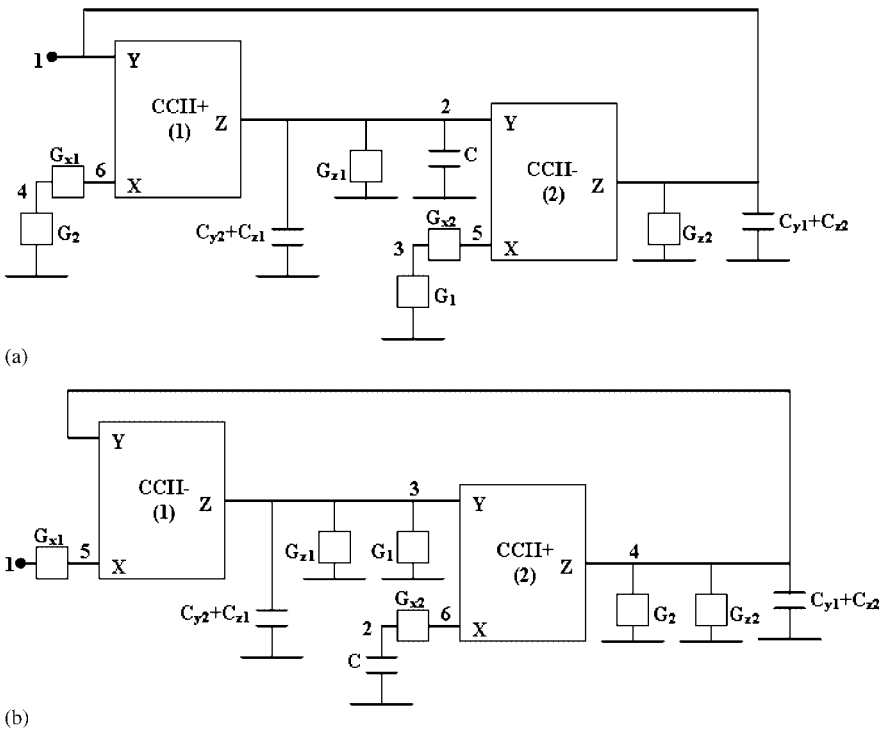

Figure 10. Circuit representation for the simulated grounded coils in Figure 8, including the CCIIs associated parasitic elements.

The two circuits depicted in Figure 10 are basically inherited from the same nullor–mirror realization in Figure 3(a), which is derived from the NAM in (4). On using the infinity variable notation to represent nullor–mirror elements in the NAM, each of the two circuit realizations will have a distinct NAM, according to the grouping of infinity variables to describe pathological pairs representing active devices (CCIIs) as well as the resulting locations of the parasitic elements. The simulated grounded inductor circuit shown in Figure 10(a) can be described using the following NAM:

$$\begin{bmatrix} G_{z2}+s(C_{y1}+C_{z2}) & \infty_2 & 0 & 0 & -\infty_2 & 0 \\ \infty_1 & G_{z1}+s(C+C_{y2}+C_{z1}) & 0 & 0 & 0 & -\infty_1 \\ 0 & 0 & G_1+G_{x2} & 0 & -G_{x2} & 0 \\ 0 & 0 & 0 & G_2+G_{x1} & 0 & -G_{x1} \\ 0 & -\infty_2 & -G_{x1} & 0 & \infty_2+G_{x2} & 0 \\ \infty_1 & 0 & 0 & -G_{x1} & 0 & -\infty_1+G_{x1} \end{bmatrix} \tag{6}$$

where the $\pm\infty_1$ and $\pm\infty_2$ variables are infinity variables that describe the nullator–current mirror pair and nullator–norator pair representing the CCII+ and CCII−, respectively; G_{x1} and G_{x2} are the parasitic series conductances at the X-terminals of the CCII+ and CCII−, respectively; C_{y1} and

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C_{y2} are the parasitic parallel capacitances at the Y-terminals of the CCII+ and CCII−, respectively; C_{z1} and C_{z2} are the parasitic parallel capacitances at the Z-terminals of the CCII+ and CCII−, respectively; and G_{z1} and G_{z2} are the parasitic parallel conductances at the Z-terminals of the CCII+ and CCII−, respectively.

It is known that interchanging rows and columns corresponding to internal nodes in a NAM is equivalent to interchanging only the numbers of internal nodes, while every node is actually kept connected to the same components. As long as this is done between internal nodes only (not port nodes), the reduced port admittance matrix describing the circuit function remains the same, and hence, the function performed by the circuit described by the NAM does not change. It is possible to make use of this fact, to simplify the Gaussian elimination steps needed to reduce a certain NAM. On having a close look at the NAM in (6), it is clear that each of the first two pivots has two lagging elements at its row and two lagging elements at its column, and hence, four operations are needed at each one of their corresponding Gaussian elimination steps. The Gaussian elimination process can be facilitated by interchanging internal nodes 3 and 5 and also 4 and 6 as in (7), resulting in pivots with only one lagging element at the row and column of every pivot. Hence, the total number of operations needed in the Gaussian elimination process is reduced:

$$\begin{bmatrix} G_{z2}+s(C_{y1}+C_{z2}) & \infty_2 & -\infty_2 & 0 & 0 & 0 \\ \infty_1 & G_{z1}+s(C+C_{y2}+C_{z1}) & 0 & -\infty_1 & 0 & 0 \\ 0 & -\infty_2 & \infty_2+G_{x2} & 0 & -G_{x2} & 0 \\ \infty_1 & 0 & 0 & -\infty_1+G_{x1} & 0 & -G_{x1} \\ 0 & 0 & -G_{x2} & 0 & G_1+G_{x2} & 0 \\ 0 & 0 & 0 & -G_{x1} & 0 & G_2+G_{x1} \end{bmatrix} \tag{7}$$

Applying four steps of Gaussian elimination on (7) will result in the following 2×2 reduced matrix for the grounded inductor

$$\begin{bmatrix} G_{z2}+s(C_{y1}+C_{z2}) & \infty_2-\dfrac{\infty_2^2}{\infty_2+G_{x2}-\dfrac{G_{x2}^2}{G_1+G_{x2}}} \\ \infty_1+\dfrac{\infty_1^2}{-\infty_1+G_{x1}-\dfrac{G_{x1}^2}{G_2+G_{x1}}} & G_{z1}+s(C+C_{y2}+C_{z1}) \end{bmatrix}$$

$$\equiv \begin{bmatrix} G_{z2}+s(C_{y1}+C_{z2}) & \dfrac{\infty_2\left(G_{x2}-\dfrac{G_{x2}^2}{G_1+G_{x2}}\right)}{\infty_2+G_{x2}-\dfrac{G_{x2}^2}{G_1+G_{x2}}} \\ \dfrac{\infty_1\left(G_{x1}-\dfrac{G_{x1}^2}{G_2+G_{x1}}\right)}{-\infty_1+G_{x1}-\dfrac{G_{x1}^2}{G_2+G_{x1}}} & G_{z1}+s(C+C_{y2}+C_{z1}) \end{bmatrix} \tag{8}$$

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Now, the limit can be taken for (8), yielding the following matrix in (9):

$$\begin{bmatrix} G_{z2}+s(C_{y1}+C_{z2}) & \left(G_{x2}-\dfrac{G_{x2}^2}{G_1+G_{x2}}\right) \\ -\left(G_{x1}-\dfrac{G_{x1}^2}{G_2+G_{x1}}\right) & G_{z1}+s(C+C_{y2}+C_{z1}) \end{bmatrix} \tag{9}$$

Additional step of Gaussian elimination yields the following 1×1 port admittance matrix for the grounded inductor:

$$\left[G_{z2}+s(C_{y1}+C_{z2})+\frac{\left(\dfrac{G_1G_{x2}}{G_1+G_{x2}}\right)\left(\dfrac{G_2G_{x1}}{G_2+G_{x1}}\right)}{G_{z1}+s(C+C_{y2}+C_{z1})} \right] \tag{10}$$

Replacing the transconductance elements by their resistive counterparts, such that $G_1 = 1/R_1$, $G_2 = 1/R_2$, $G_{x1} = 1/R_{x1}$, $G_{x2} = 1/R_{x2}$, $G_{z1} = 1/R_{z1}$, and $G_{z2} = 1/R_{z2}$, then the input impedance can be written as

$$Z_{\text{in-I}}(s) = \frac{a_1 s + a_0}{b_2 s^2 + b_1 s + b_0} \tag{11}$$

where

$$\begin{aligned} a_0 &= R_{z2}(R_1+R_{x2})(R_2+R_{x1}) \\ a_1 &= R_{z1}R_{z2}(R_1+R_{x2})(R_2+R_{x1})(C+C_{y2}+C_{z1}) \\ b_0 &= R_{z1}R_{z2}+(R_1+R_{x2})(R_2+R_{x1}) \\ b_1 &= (R_1+R_{x2})(R_2+R_{x1})[R_{z1}(C+C_{y2}+C_{z1})+R_{z2}(C_{y1}+C_{z2})] \\ b_2 &= R_{z1}R_{z2}(R_1+R_{x2})(R_2+R_{x1})(C_{y1}+C_{z2})(C+C_{y2}+C_{z1}) \end{aligned} \tag{12}$$

Now, consider the simulated grounded inductor circuit in Figure 10(b). This simulated grounded coil circuit can be described using the following NAM:

$$\begin{bmatrix} G_{x1} & 0 & 0 & 0 & -G_{x1} & 0 \\ 0 & G_{x2}+sC & 0 & 0 & 0 & -G_{x2} \\ 0 & 0 & G_1+G_{z1}+s(C_{y2}+C_{z1}) & \infty_1 & -\infty_1 & 0 \\ 0 & 0 & \infty_2 & G_2+G_{z2}+s(C_{y1}+C_{z2}) & 0 & -\infty_2 \\ -G_{x1} & 0 & 0 & -\infty_1 & \infty_1+G_{x1} & 0 \\ 0 & -G_{x2} & \infty_2 & 0 & 0 & -\infty_2+G_{x2} \end{bmatrix} \tag{13}$$

where the $\pm\infty_1$ and $\pm\infty_2$ variables are infinity variables that describe the nullator–norator pair and nullator–current mirror pair representing the CCII− and CCII+, respectively; G_{x1} and G_{x2}

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are the parasitic series conductances at the X-terminals of the CCII− and CCII+, respectively; C_{y1} and C_{y2} are the parasitic parallel capacitances at the Y-terminals of the CCII− and CCII+, respectively; C_{z1} and C_{z2} are the parasitic parallel capacitances at the Z-terminals of the CCII− and CCII+, respectively; and G_{z1} and G_{z2} are the parasitic parallel conductances at the Z-terminals of the CCII− and CCII+, respectively.

A similar scenario of Gaussian elimination steps, applying limits, and replacing the transconductance elements by their resistive counterparts, will yield the following input impedance for this simulated grounded coil:

$$Z_{\text{in-II}}(s) = \frac{m_3 s^3 + m_2 s^2 + m_1 s + m_0}{n_3 s^3 + n_2 s^2 + n_1 s + n_0} \tag{14}$$

where

$$\begin{aligned}
m_0 &= R_{x1}(R_1 + R_{z1})(R_2 + R_{z2}) \\
m_1 &= C R_1 R_2 R_{z1} R_{z2} + C R_{x1} R_{x2}(R_1 + R_{z1})(R_2 + R_{z2}) \\
&\quad + R_{x1}[R_2 R_{z2}(R_1 + R_{z1})(C_{y1} + C_{z2}) + R_1 R_{z1}(R_2 + R_{z2})(C_{y2} + C_{z1})] \\
m_2 &= R_1 R_2 R_{x1} R_{z1} R_{z2}(C_{y1} + C_{z2})(C_{y2} + C_{z1}) \\
&\quad + C R_{x1} R_{x2}[R_2 R_{z2}(R_1 + R_{z1})(C_{y1} + C_{z2}) + R_1 R_{z1}(R_2 + R_{z2})(C_{y2} + C_{z1})] \\
m_3 &= C R_1 R_2 R_{x1} R_{x2} R_{z1} R_{z2}(C_{y1} + C_{z2})(C_{y2} + C_{z1}) \\
n_0 &= (R_1 + R_{z1})(R_2 + R_{z2}) \\
n_1 &= C R_{x2}(R_1 + R_{z1})(R_2 + R_{z2}) + R_2 R_{z2}(R_1 + R_{z1})(C_{y1} + C_{z2}) \\
&\quad + R_1 R_{z1}(R_2 + R_{z2})(C_{y2} + C_{z1}) \\
n_2 &= R_1 R_2 R_{z1} R_{z2}(C_{y1} + C_{z2})(C_{y2} + C_{z1}) \\
&\quad + C R_{x2}[R_2 R_{z2}(R_1 + R_{z1})(C_{y1} + C_{z2}) + R_1 R_{z1}(R_2 + R_{z2})(C_{y2} + C_{z1})] \\
n_3 &= C R_1 R_2 R_{x2} R_{z1} R_{z2}(C_{y1} + C_{z2})(C_{y2} + C_{z1})
\end{aligned} \tag{15}$$

Regarding that the parasitic capacitances are on the order of femtofarads and R_x is usually few tens of ohms, the second- and third-order terms in (11) and (14) are effective only at very high frequencies and may be ignored for the frequency of our interest. Hence, the input impedances of the simulated grounded inductors in Figure 10(a) and (b) can be approximated as in (16) and (17), respectively:

$$Z_{\text{in-I}}(s) \approx \frac{a_1 s + a_0}{b_1 s + b_0} \tag{16}$$

$$Z_{\text{in-II}}(s) \approx \frac{m_1 s + m_0}{n_1 s + n_0} \tag{17}$$

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3.2. Discussion

The input impedances in (16) and (17) indicate that the operation of the two circuits in Figure 10(a) and (b) as ideal grounded inductors is limited by the conditions $a_0/a_1 \ll \omega \ll 3b_0/b_1$ and $m_0/m_1 \ll \omega \ll n_0/n_1$, respectively; so that to obtain characteristics of ideal grounded inductances with input impedances $Z_{\text{in-I}}(s) \approx a_1 s/b_0$ and $Z_{\text{in-II}}(s) \approx m_1 s/n_0$. Using a factor of 10, the lower and upper frequency limits of the two circuits in Figure 10(a) and (b) due to the parasitic impedance effects can be given as $f_{\text{LP1}} = 10a_0/(2\pi a_1) \leqslant f \leqslant f_{\text{HP1}} = 0.1b_0/(2\pi b_1)$ and $f_{\text{LP2}} = 10m_0/(2\pi m_1) \leqslant f \leqslant f_{\text{HP2}} = 0.1n_0/(2\pi n_1)$, respectively. The comparison between the frequency responses of the two grounded inductance simulators will involve investigating their upper and lower frequency limits and their sensitivities to the values of actual passive components.

From (12), $a_0/a_1 = 1/[R_{z1}(C + C_{y2} + C_{z1})]$. Thus, the lower frequency limit for the simulated grounded inductor circuit in Figure 10(a) is almost sensitive only to the grounded load capacitance connected at terminal 2 of the gyrator. Increasing the grounded load capacitance C reduces, and hence improves, the lower frequency limit for the simulated inductor in Figure 10(a) and *vice versa*. The possibility of improving the lower frequency limit for this circuit is limited by the constraints on the capacitance within the IC, imposed by the fabrication process. From (15), m_0/m_1 is sensitive to the values of all actual passive elements. Increasing R_1, R_2, or C reduces the lower frequency limit for the simulated grounded inductor circuit in Figure 10(b) and *vice versa*. Knowing that R_z is in the order of tens of megaohms, the expressions of m_0 and m_1 in (15) imply that m_0/m_1 can be higher or lower than a_0/a_1, depending on the values of R_1 and R_2. Hence, the simulated grounded inductor circuit in Figure 10(b) offers further controllability on the lower frequency limit. Moreover, for higher values of simulated inductance, the circuit in Figure 10(b) exhibits improvement in its lower frequency limit.

Similarly, the upper frequency limits for the two circuits in Figure 10 can be investigated using the expressions in (12) and (15) to evaluate b_0/b_1 and n_0/n_1, respectively. The measure of the upper frequency limit for the circuit in Figure 10(a), b_0/b_1, is sensitive to the values of all actual passive elements, such that, increasing R_1, R_2, or C reduces b_0/b_1 and *vice versa*. A similar statement applies to the measure of the upper frequency limit for the circuit in Figure 10(b), n_0/n_1, however, the expressions of n_0 and n_1 in (15) indicate that n_0/n_1 is less sensitive than b_0/b_1 to the changes in the values of R_1 and R_2. In the expression of n_1 in (15), the R_{x2} product in the first term causes n_0/n_1 to be much less than b_0/b_1 for similar values of R_1, R_2, and C. Hence, the upper frequency limit for the simulated inductor in Figure 10(b) is mainly degraded due to the unabsorbed parasitic resistance appearing in series with the load capacitance C at the X-terminal of the CCII+.

The expressions in (12) and (15) also imply that b_0/b_1 and n_0/n_1 are much higher than a_0/a_1 and m_0/m_1, respectively, and hence, the bandwidth for the circuits in Figure 10 is mainly determined by their upper frequency limits. Therefore, the bandwidth of the circuit in Figure 10(a) is much wider than that of the circuit in Figure 10(b). The wide bandwidth of operation is an attractive feature for most of the applications using the inductors, like filters and oscillators, which usually involve tunability and high frequencies of operation. Thus, the advantage of the wide bandwidth of operation enables the grounded inductance simulator in Figure 10(a) to offer a better performance than the one in Figure 10(b), in terms of bandwidth and operation at high frequencies, when used in the grounded inductance applications.

From the above analysis considering the parasitic impedance components associated with the CCIIs, the grounded inductance simulator based on the gyrator circuit belonging to topology I

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provides a better frequency response than the grounded inductance simulator based on the gyrator circuit belonging to topology II. Hence, the CCII-based gyrator topology using the CCIIs Y–Z-terminals as input and output terminals is less sensitive to the CCIIs associated parasitic elements, and thus, more efficient than the CCII-based gyrator topology using X-terminals of the CCIIs as gyrator input and output terminals. Simulations are performed in the next section to illustrate the analytical conclusions derived in this section.

4. SIMULATION RESULTS

In this section, SPICE simulations are performed to demonstrate the previously deduced analytical results in comparing the two CCII-based gyrator circuit topologies. The simulated grounded coils shown in Figure 8 are simulated with a symmetrical dc power supply voltages $V_{DD} = -V_{SS} = 1.5\,\text{V}$ in the TSMC 0.25-μm CMOS process provided by MOSIS. The two grounded coil circuits will be simulated using the same active devices and passive elements, to maintain identical conditions needed for a fair comparison. The long tail pair based CCII+ realization in [22] and the floating current source (FCS) based CCII− realization in [23], shown in Figures 11 and 12, respectively; are used in the simulations. For the CCII+, the bias voltages V_B and V_C are $-0.7\,\text{V}$ and $-0.72\,\text{V}$, respectively. The CCII− is biased using a biasing current $2I_B = 100\,\mu\text{A}$, and compensated using a capacitor $C_1 = 1\,\text{pF}$ connected between the gate of M_7 and the drain of M_{10}. The dimensions of the MOS transistors in the CCII− and CCII+ structures are given in Tables I and II, respectively. Level-49 MOS model parameters used for simulations are given in [24].

In order to exhibit the frequency-domain performance of the simulated grounded inductors in Figure 8, three sets of values for the passive elements are selected as $C = 1\,\text{nF}$, $R_1 = 1\,\text{k}\Omega$, and $R_2 = 1\,\text{k}\Omega$; $C = 0.1\,\text{nF}$, $R_1 = 10\,\text{k}\Omega$, and $R_2 = 10\,\text{k}\Omega$; and $C = 1\,\text{nF}$, $R_1 = 10\,\text{k}\Omega$, and $R_2 = 10\,\text{k}\Omega$, which results in $L = 1\,\text{mH}$, $L = 10\,\text{mH}$, and $L = 100\,\text{mH}$, respectively. The magnitude and phase responses for the impedances of these simulated grounded coils compared with ideal ones are depicted in Figure 13. The simulation results are shown to agree with the analytical conclusions

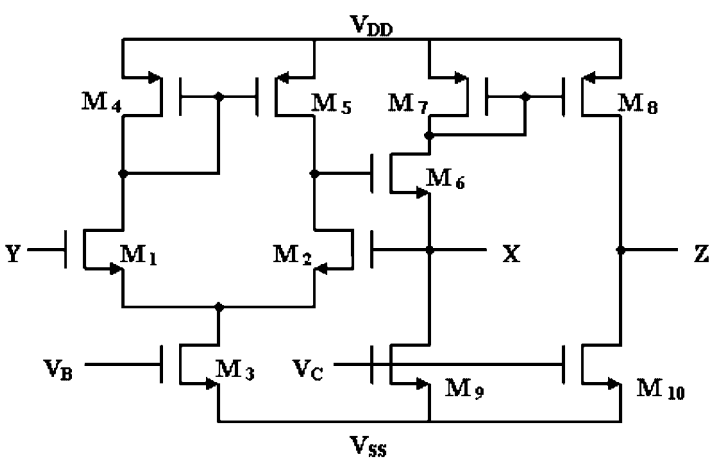

Figure 11. The long tail pair-based CCII+ realization reported in [20].

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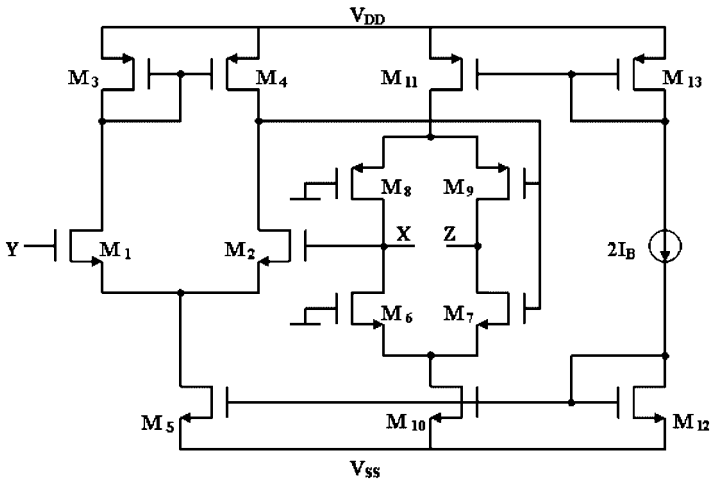

Figure 12. The FCS-based CCII− realization reported in [21].

Table I. Dimensions of the MOS transistors in the CCII+ of Figure 11.

	W (μm)/L (μm)
NMOS transistors	
M_1 and M_2	25/0.5
M_3	8/0.5
M_6	14/0.5
M_9 and M_{10}	4/0.5
PMOS transistors	
M_4, M_5, M_7, and M_8	10/0.5

Table II. Dimensions of the MOS transistors in the CCII− of Figure 12.

	W (μm)/L (μm)
NMOS transistors	
M_1 and M_2	25/0.5
M_5	20/0.5
M_6 and M_7	10/0.5
M_{10} and M_{12}	30/0.75
PMOS transistors	
M_3 and M_4	30/1.5
M_8 and M_9	10/0.5
M_{11} and M_{13}	30/0.75

derived in the previous section. The circuit in Figure 8(b) exhibits a reduced lower frequency limit that is decreasing with the increase in the value of the simulated inductance, while the lower frequency limit for the circuit in Figure 8(a) has been increased, and thus degraded, on decreasing

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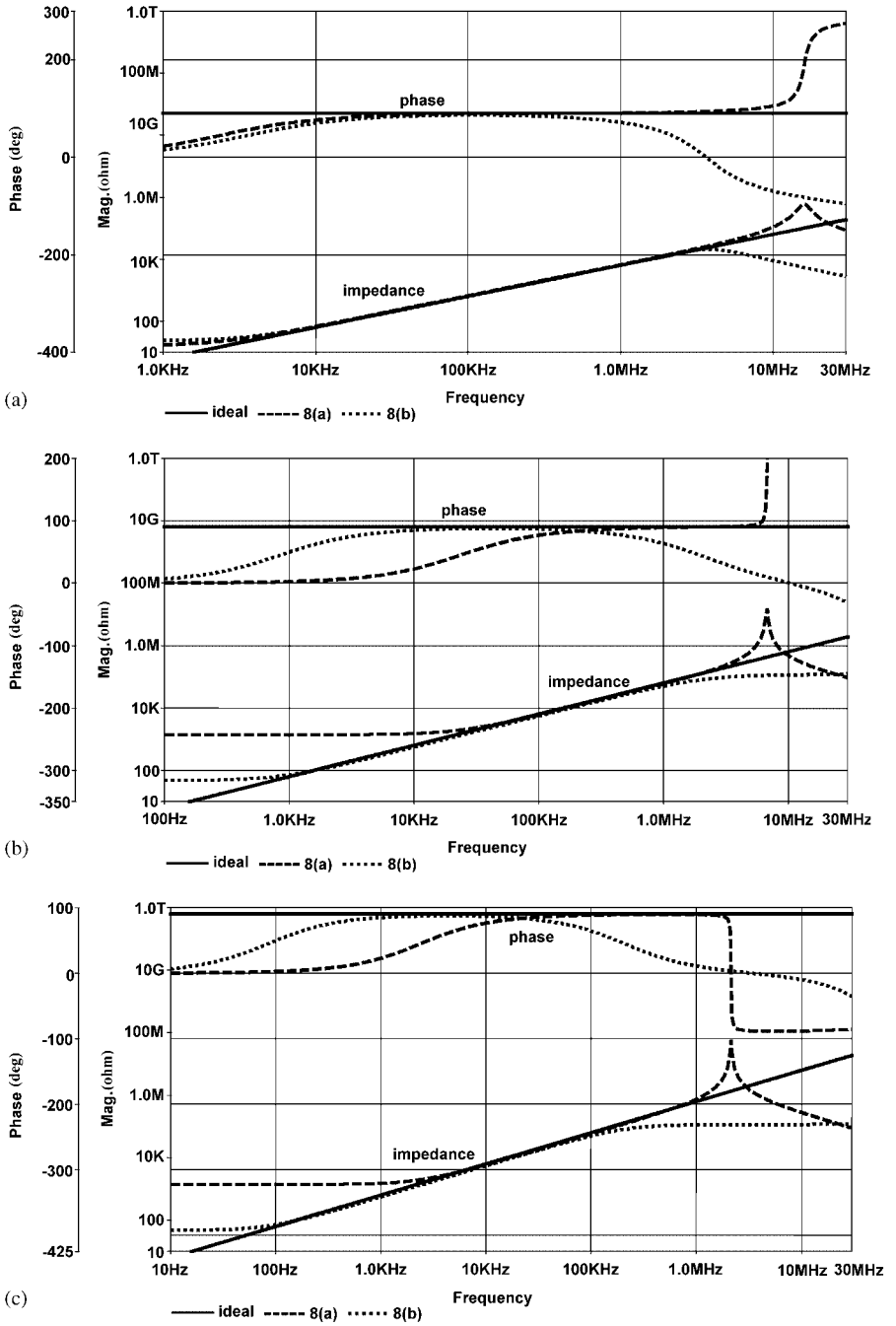

Figure 13. Magnitude and phase responses for the impedance of the simulated grounded inductances in Figure 8 and ideal inductance: (a) 1 mH; (b) 10 mH; and (c) 100 mH.

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the value of the load capacitance C. At high frequencies, where the response of the circuit in Figure 8(b) appears to be much deviating from the response of the ideal inductance, the impedance of the circuit in Figure 8(a) remains close to that of the ideal inductance. The circuit in Figure 8(a) exhibits a better performance at high frequencies and a wider bandwidth than those of the circuit in Figure 8(b).

To further illustrate the difference in performance between the two simulated grounded inductances of Figure 8 at high frequencies, the 1 mH simulated inductances realized above are used to construct the high-pass *RL* section shown in Figure 14, composed of a floating resistor $R_S = 1\,\text{k}\Omega$ and a grounded inductance simulator $L_P = 1\,\text{mH}$. The frequency responses for gains of the resulting high-pass *RL* sections are depicted in Figure 15. Simulation results show that at high frequencies, the *RL* section constructed using the simulated grounded coil in Figure 8(b) suffers from a poor response much deviating from the response of the *RL* section using an ideal coil,

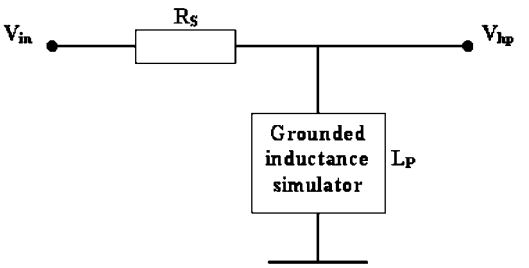

Figure 14. High-pass *RL* section with a floating resistance R_S and a grounded inductance simulator L_P.

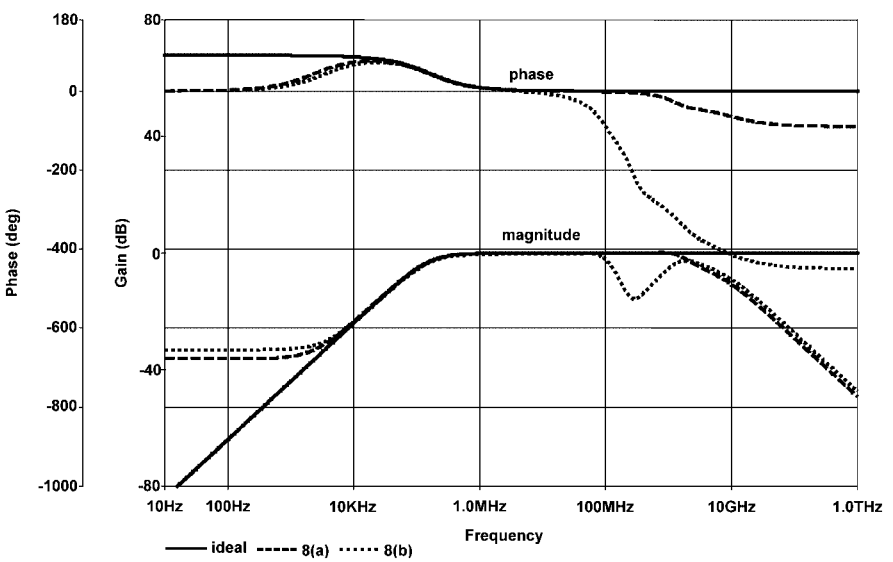

Figure 15. Magnitude and phase responses for the gain of the high-pass *RL* section in Figure 14 constructed using the simulated grounded inductances in Figure 8 and ideal inductance.

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while the *RL* section constructed using the simulated grounded coil in Figure 8(a) maintains high performance with a response close to the ideal one for a wider band.

Hence, on using two gyrators belonging to the two CCII-based gyrator circuit topologies to realize grounded inductance simulators, under the same conditions and using identical resources, the circuit built using the gyrator belonging to topology I exhibits recognizable performance advances, in terms of bandwidth and operation at high frequencies, over the circuit built using the gyrator belonging to topology II. Thus, according to the simulation results, the CCII-based gyrator topology with input and output terminals as CCIIs $Y-Z$-terminals is better and more efficient than the other topologies employing CCIIs X-terminals as gyrator inputs and output terminals.

5. CONCLUSION

In this study, the generalized symbolic framework for linear active circuits has been employed in the synthesis, modeling, and non-ideal analysis of CCII-based gyrators. Various nullor–mirror ideal representations for the gyrator were generated using the generalized approach for analog active circuit synthesis by admittance matrix expansion. The synthesized CCII-based gyrator circuits have been classified into two topologies according to the type of the CCII terminals handling the gyrator input and output. A detailed analytical comparison between the actual performances of the two topologies was performed, in which it was deduced that the CCII-based gyrator topology with inputs and outputs as CCIIs $Y-Z$-terminal is less sensitive to CCIIs associated parasitic elements; and hence, more efficient than the other topology using CCIIs X-terminals as gyrator input and output terminals. SPICE simulations have demonstrated the results derived in the analytical investigation.

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