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A Tunable Square Root Domain Oscillator

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Abstract. This letter presents a square root domain oscillator; which inherits the tunability, linearity, and frequency response of square root domain filters. The oscillator is based on an extreme case of a second order bandpass filter with quality factor set to infinity. The oscillator function is demonstrated analytically and by simulation.

Key Words: square root domain, oscillators

1. Introduction

Square root domain filters constitute an emerging family of externally linear internally nonlinear (ELIN) circuits. As part of ELIN circuits they enjoy a very good bandwidth-linearity compromise, as well as demonstrating intrinsic tunability [1–3]. In the coming sections a proposal for a square root domain oscillator is presented. Section 2 presents the oscillator circuit and explains its derivation as a special case of a second order square root domain filter. Section 3 introduces the choice of building blocks used. Section 4 demonstrates the oscillator through time domain and frequency domain simulations.

2. From Second Order Bandpass to Oscillator

Square root domain filters are commonly designed using a transformed state space [3]. If a second order filter is designed using a direct programming state space, the results can be translated into a circuit as in Fig. 1 [4]. Square root domain filters use two current mode nonlinear building blocks, the first is called a geometric mean cell and it realizes the relation $I_{\text{geomean}} = \sqrt{I_{\text{in}\,1} I_{\text{in}\,2}}$. The second block is called squarer divider and as the name suggests it realizes $I_{\text{sqdiv}} = I_{\text{in}\,1}^2 / I_{\text{in}\,2}$. A cascade of these two blocks is traditionally called a "square root transconductor". The filter in Fig. 1 is originally designed to obtain a low pass response at I_1, but by observation or a quick derivation it can be shown that the response at I_2 is:

$$\frac{I_2}{I_{\text{in}}} = \frac{\frac{\sqrt{2K_2 I_A}}{C_2} s}{\frac{\sqrt{4K_1 K_2 I_B I_D}}{C_1 C_2} + \frac{\sqrt{2K_2 I_C}}{C_2} s + s^2} \tag{1}$$

Where $K_i = \mu_n C \frac{W_i}{L_i}$ and i refers to the corresponding expanding transistor M_i.

This is the response of a bandpass filter with:

$$Q = \sqrt{\frac{C_2}{C_1}} \sqrt[4]{\frac{K_1}{K_2}} \frac{\sqrt[4]{4 I_B I_D}}{\sqrt{2 I_C}} \tag{2}$$

$$\omega_o = \sqrt{\frac{\sqrt{4 K_1 K_2 I_B I_D}}{C_1 C_2}} \tag{3}$$

One problem of this filter is its limited quality factor. Examination reveals that the independent geometric mean cell in Fig. 1 functions as a negative feedback block. Raising the current of this block causes the poles to shift to the left hand side, conversely reducing this current causes poles to approach the imaginary axis (and the quality factor to rise). Reducing or raising the current is as simple as reducing or raising the aspect ratios of output mirrors in the building block, the quality factor changes proportionately.

Taking this approach to the extreme one may reduce this current to zero, in effect removing the geometric mean cell altogether. This essentially raises the quality

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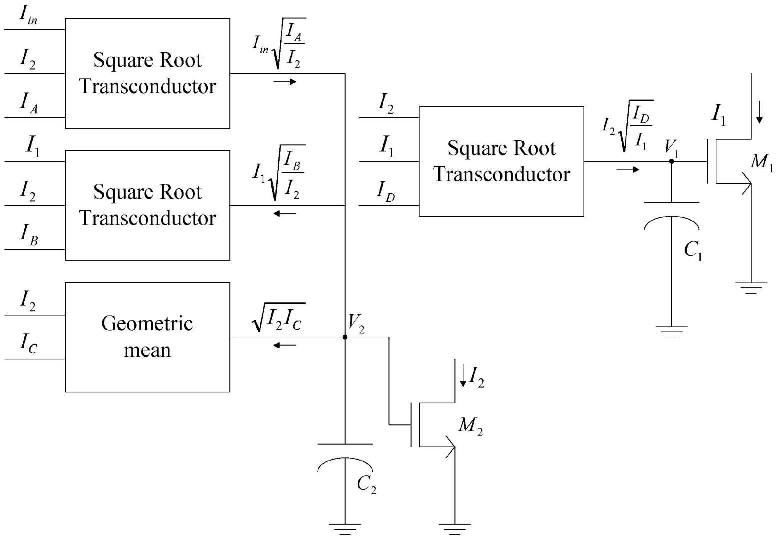

Fig. 1. Second order square root domain filter.

factor to infinity, placing the poles on the imaginary axis. If the input current is also replaced by a DC current, and the circuit is modified to provide DC paths as in Fig. 2, the circuit reduces to an oscillator. The circuit equations are:

$$I_{\mathrm{DC}}\sqrt{I_F} = \frac{C_2\dot{I}_2}{\sqrt{2K_2}} + I_1\sqrt{I_B} \tag{4}$$

$$I_{\mathrm{DC}}\sqrt{I_E} + \frac{C_1\dot{I}_1}{\sqrt{2K_1}} = I_2\sqrt{I_D} \tag{5}$$

Differentiating Eq. (5) yields:

$$\frac{C_1}{\sqrt{2K_1I_D}}\ddot{I}_1 = \dot{I}_2 \tag{6}$$

Substituting (6) in (4):

$$I_1 = \frac{I_{\mathrm{DC}}\frac{\sqrt{4K_1K_2I_DI_F}}{C_1C_2}}{s^2 + \frac{\sqrt{4K_1K_2I_BI_D}}{C_1C_2}} \tag{7}$$

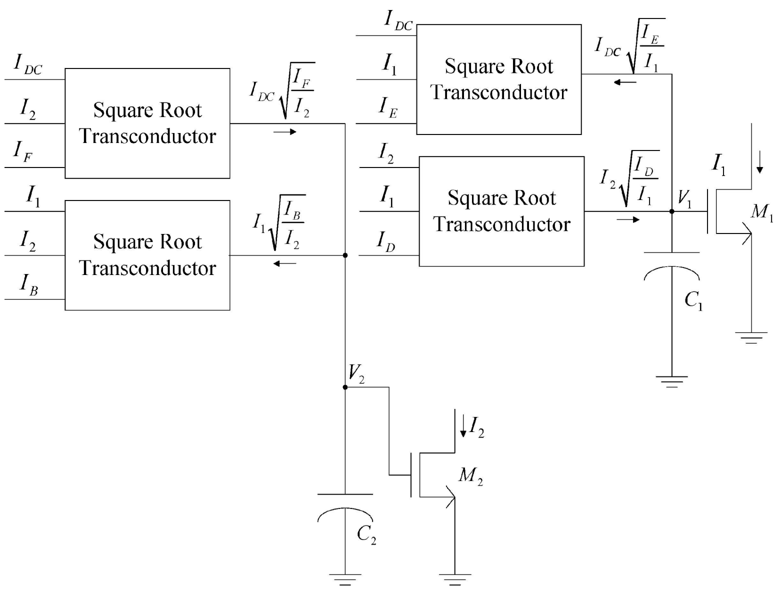

Fig. 2. Square root domain oscillator.

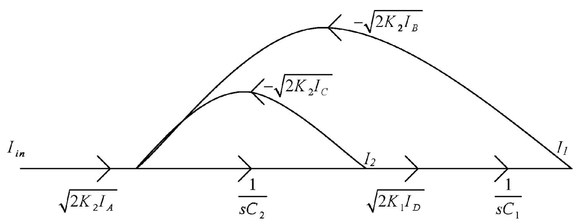

Fig. 3. Signal flow graph of second order filter.

And from (6):

$$I_2 = \frac{s I_{\mathrm{DC}} \frac{\sqrt{2K_2 I_F}}{C_2}}{s^2 + \frac{\sqrt{4K_1K_2I_BI_D}}{C_1C_2}} \tag{8}$$

Therefore the output currents are single tones with frequencies identical to (3). Tuning is maintained through current sources $I_{B,D}$.

Although square root domain filters are internally nonlinear, the oscillatory behavior may be tentatively explained in terms of feedback. The loop feedback in Fig. 1 is achieved through both the independent geometric mean cell and the square root transconductor. Figure 3 shows a signal flow graph of a linearized version of the filter. The signal flow graph is derived from the state equations of the circuit. The state equations for the circuit in Fig. 1 are:

$$\frac{C_1}{\sqrt{2K_1I_D}}\dot{I}_1 = I_2 \tag{9}$$

$$\frac{C_2}{\sqrt{2K_2}}\dot{I}_2 = I_{\mathrm{in}}\sqrt{I_A} - I_1\sqrt{I_B} - I_2\sqrt{I_C} \tag{10}$$

Identification of feedback is straightforward from Fig. 3. The feedback gain is:

$$-\frac{\sqrt{4K_1K_2I_BI_D}}{s^2C_2C_1} - \frac{\sqrt{2K_2I_C}}{sC_2} \tag{11}$$

One way in which (11) can satisfy an oscillatory condition is if the second term vanishes, which is equivalent to removing the geometric mean cell in Fig. 1. Under this condition positive feedback is established and the oscillation frequency is found to be equal to (3).

3. Building Blocks

Operation of the oscillator will be limited by the accuracy of building blocks. In particular the shape of the resultant waveform will suffer greatly from secondary effects common in traditional square root domain building blocks. Early simulations showed that channel length modulation in particular can be detrimental to proper operation. Square root domain building blocks are based on a MOS translinear loop with special mirroring conditions. A typical example is the geometric mean cell from [3] which is based on a stacked MOS translinear loop. This circuit was modified to reduce channel length modulation, resulting in Fig. 4. The main loop responsible for basic operation is formed by deeply saturated transistors M_{1-4}. The modification is presented through transistor M_7 which cascodes the output transistor, thus immunizing it from channel length modulation, and also M_5 which reduces channel length modulation on M_4. The squarer divider used was adapted from the geometric mean cell. If one of the inputs of a geometric mean cell is exchanged with the output the result is a squarer divider. The squarer divider used is presented in Fig. 5. The main MOS translinear loop is still represented by transistors M_{1-4}. The remaining transistors are responsible for modifying impedances at the input and output to accommodate the exchange of ports. The aspect ratios used are shown in Table 1.

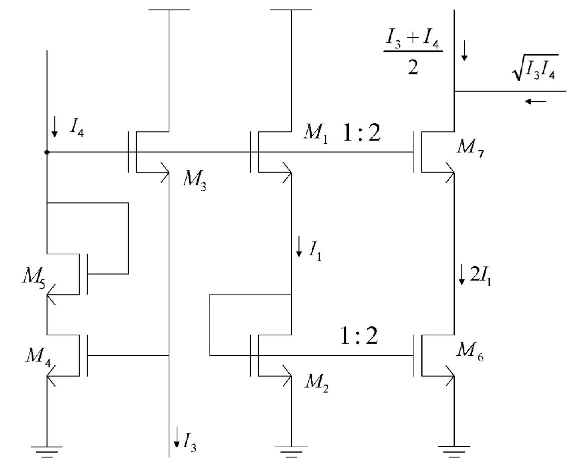

Fig. 4. Modified geometric mean cell.

Table 1. Transistor aspect ratios.

Circuit/transistors	W/L in μm/μm
Modified geometric mean Fig. 4. M_{1-5}	2/1
Modified geometric mean Fig. 4. $M_{6,7}$	1/2
Modified squarer divider Fig. 5. All transistors	1/1

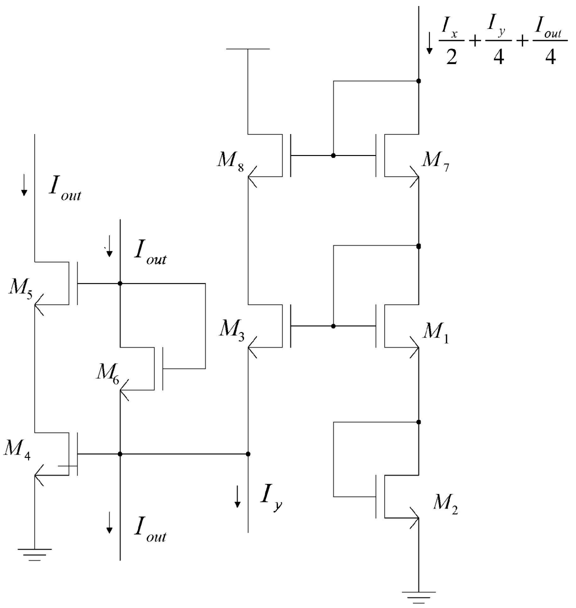

Fig. 5. Squarer divider cell.

4. Simulation Results

The circuit in Fig. 2 was simulated using HSPICE and a BISIM 3v3 0.5 μm model. Figure 6 shows frequency domain response for the circuit. The effect of tuning is clear since the three curves with different centre frequencies correspond to bias currents of 2, 3, 4 μA. Time domain response of the oscillator is shown in Fig. 7.

Waveform shaping is left to the building blocks, the feedback provided by the squarer divider blocks ensures that currents do not rise or fall beyond limits predicted by equations. The resulting shape depends greatly (as mentioned above) on the quality of building blocks used. However, this very basic amplitude limiting method will fail if the designed amplitude is outside the range of the building blocks, or if the poles are pushed to the right hand side too deeply. In which case a wave more akin to square waves is observed. Shifting to the right hand side can result from block inaccuracies or because onset of oscillation may require poles to be pushed slightly to the right. This can be achieved by maintaining the geometric mean cell but reversing its direction, thus causing the s-term in (1) to become negative.

The method described in Section 2 can be extended to any topology (not only bandpass filters) by identifying the negative feedback path and modifying it in the way suggested above. Resulting oscillators will have current mode outputs and will be compatible with square root domain circuits. In addition they inherit the advantages of square root domain filters: They can provide relatively high oscillation amplitudes, they are tuneable, and they work at relatively high frequencies [1–3].

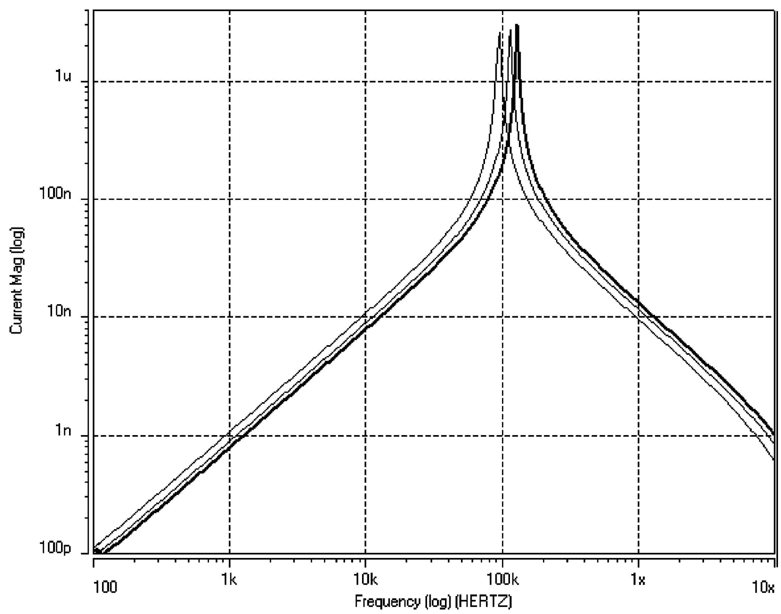

Fig. 6. Magnitude response of the oscillator showing tuning action.

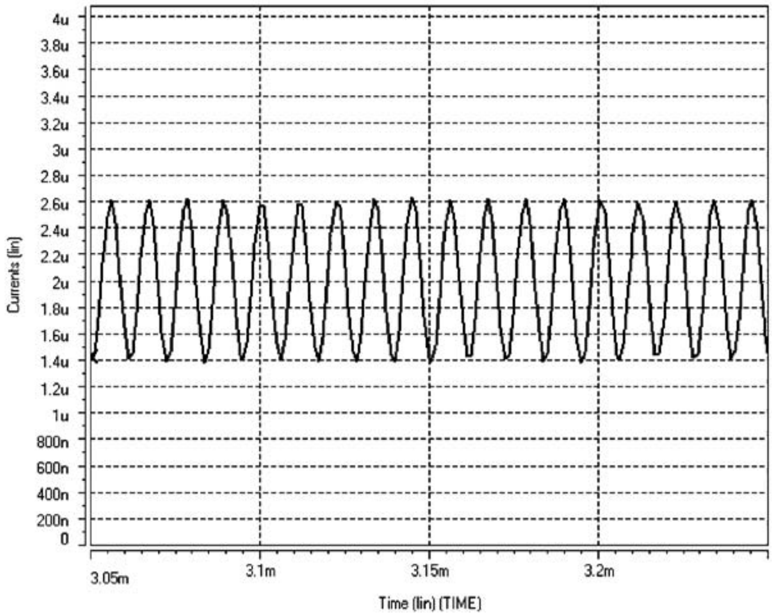

Fig. 7. Time domain response of the oscillator.

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