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Low Voltage Digitally Controlled CMOS Current Conveyor

Ahmed A. El-Adawy, Ahmed M. Soliman and Hassan O. Elwan

Abstract **In this paper, a digitally controlled current conveyor (DCCC) is presented. The proposed DCCC is based on rail-to-rail folded cascode implementation with a current division network (CDN). The CDN is used to provide control on the current gain of the DCCC. The CDN uses a novel current division technique based on differential pairs. The proposed DCCC can operate from ± 1.5 V supply voltages. Applications of the proposed DCCC such as variable gain amplifiers (VGA) and digitally tuned filters have been investigated. PSpice simulations based on the AMI 1.2 μm N-well level 3 parameters are in agreement with the presented work.**

Keywords **CMOS Current Conveyor, Filters**

1. Introduction

Programmable characteristic of an analog cell is a key feature that is used in so many useful applications. Temperature and process variations are the main limiting problems in the field of analog VLSI. To compensate for these variations, analog or digital tuning of the parameters of an analog cell is employed. However, in low voltage applications, there is a limitation on the allowable range of the analog tuning voltage. Hence, in these applications, digital control is more attractive. Another example is the variable gain amplifier (VGA) which is used in many applications in order to maximize the dynamic range of the overall system by varying the gain of the VGA. Hearing aids [1], disk drives [2, 3], and wireless communications are examples of such systems [4]. In modern wireless systems, all of the baseband signal processing is implemented digitally by a digital signal processor. Hence, a primary requirement of the VGA is to be digitally controlled. Another requirement of the VGA is that the gain should be independent of the bandwidth of the VGA. Traditional structures using the operational amplifiers may not be useful.

In this paper, a low voltage digitally controlled current conveyor is presented. The DCCC is a versatile analog building block described symbolically as shown in Fig. 1(a) and mathematically by the following matrix equation:

$$\begin{pmatrix} V_X \\ I_Z \\ I_Y \end{pmatrix} = \begin{pmatrix} 0 & 0 & 1 \\ -\alpha & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} I_X \\ V_Z \\ V_Y \end{pmatrix} \quad (1)$$

Where α is the digitally controlled current gain parameter. Precise gain control is achieved using a novel current division technique which gives wide control range with no component spreading.

2. The DCCC

The circuit realization of the proposed DCCC is shown in Fig. 1(b). It consists of three stages. The input stage is a complementary differential pair to provide rail-to-rail input range. The next stage is a folded cascode gain stage which is followed by a class AB output stage. This three stage amplifier is connected in a unity feedback configuration so that the output voltage (V_X) follows the input voltage (V_Y) in almost the whole supply voltage range. The operation of the class AB output stage could be described as follows: if a current is withdrawn from the X terminal, the gate voltage of M24 decreases. By the action of the level shift transistor M22 the gate voltage of M25 decreases as well. Thus, the current through M24 decreases while the current in M25 increases. The level shift voltage is used to adjust the standby current of the loop. At standby mode, when no current flows in or out of the X terminal, the current flowing in M24 and M25 is equal to I_{SB}. The X terminal current is mirrored to the Z terminal using supply-sensing technique and is digitally controlled by the current division network (CDN). The output current I_Z is obtained by mirroring the currents in the transistors M24 and M25, dividing the mirrored currents using CDN_N and CDN_P and mirroring the divided currents again by the current mirrors (M27 and M31) and (M29 and M30) respectively. The two current division blocks CDN_N and CDN_P are controlled digitally by the same digital input word α. The operation of these blocks is described in the following section.

3. The CDN

The block diagram of the proposed CDN_N is shown in Fig. 2. It consists of current division cells (CDC). Each cell has three output currents whose relations with the in-

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Ahmed A. El-Adawy, Ahmed M. Soliman, Electronics and Communications Engineering Department, Cairo University, Egypt.
E-mail: asoliman@idscl.gov.eg
Hassan O. Elwan, Department of Electrical Engineering, The Ohio State University, Columbus, OH 43210, USA
Correspondence to A. M. Soliman.

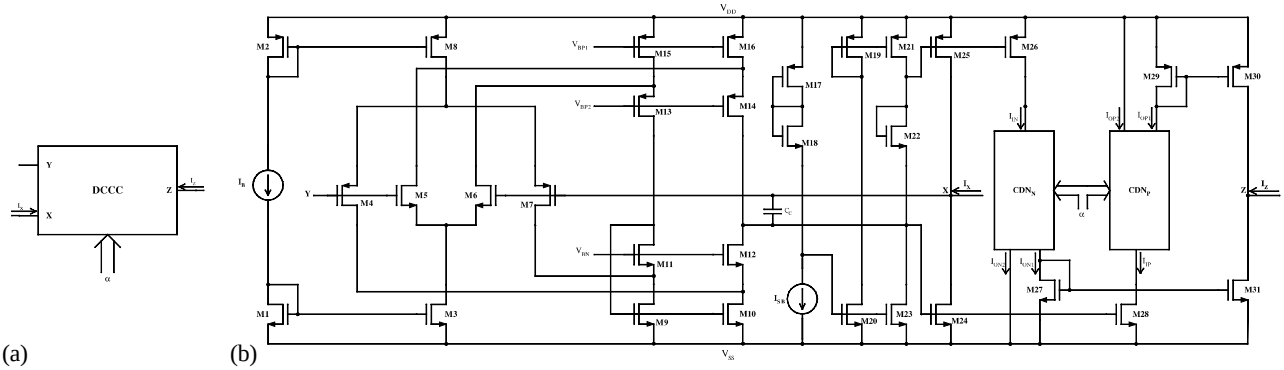

Fig. 1. The DCCC (a) symbol (b) circuit realization.

put current are expressed as:

$$I_{O1i} = a_i \frac{I_{Ii}}{2} \tag{2}$$

$$I_{O2i} = \overline{a_i} \frac{I_{Ii}}{2} \tag{3}$$

$$I_{O3i} = \frac{I_{Ii}}{2} \tag{4}$$

Where the suffix i denotes the order of the cell. From Fig. 2, we can write:

$$I_{I(i-1)} = I_{O3i} \tag{5}$$

From equations (2) through (5), the following equations can be derived:

$$I_{O1} = I_{O3} + \sum_{i=0}^{i=n-1} I_{O1i} = \frac{1}{2^n}\left(1 + \sum_{i=0}^{i=n-1} 2^i a_i\right) I_I \tag{6}$$

$$I_{O2} = \sum_{i=0}^{n-1} I_{O2i} = \frac{1}{2^n}\left(\sum_{i=0}^{n-1} 2^i a_i\right) I_I \tag{7}$$

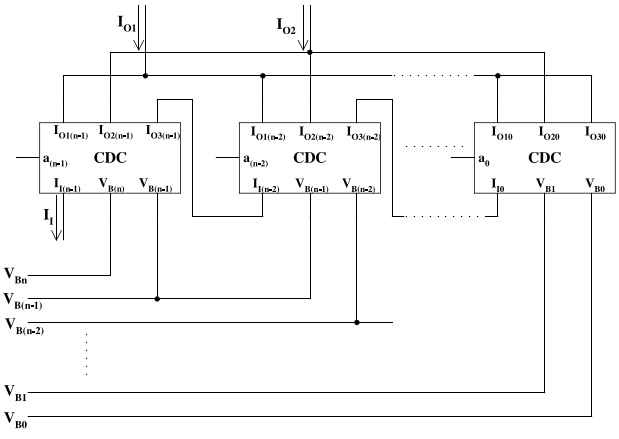

Fig. 2. The CDN block diagram.

$$\alpha = \frac{I_{O1}}{I_I} = \frac{1 + \sum_{i=0}^{n-1} 2^i a_i}{2^n} \tag{8}$$

Hence, the current gain of the proposed CDN is digitally controlled. The traditional approach to implement the CDN is to use the well-known resistive R-2R ladder circuit. For proper operation, all the resistances in the ladder must be matched. This may be very difficult to achieve in practice specially when number of bits increases. Furthermore, the switches which are used to switch the current either to the I_{O1} or I_{O2} branches are usually implemented using MOS transistors which have finite on resistances. These finite resistances affect the accuracy of current division. Another drawback is that the output resistance of this CDN is small. This means that the output nodes I_{O1} or I_{O2} should be at virtual ground voltages. This prevents the use of this circuit in the applications where the input resistance of the stage next to the CDN is finite. In the DCCC, the output current of the CDN is mirrored using MOS transistors which have finite input resistances. Hence, a resistive ladder CDN can not be used in this application. Also, the resistive ladder has a finite input resistance, hence to achieve high current levels in low voltage applications, it is necessary to reduce the value of R. However, this reduction results in a smaller output resistance and puts a stringent requirement on the next stage input resistance. Hence there is a trade off between the input and output resistances by choosing the value of R.

A better approach to implement the CDC is to use of MOS ladder circuit. Although the structure of this circuit is similar to the classical resistor based R-2R ladder; the transistors do not have to emulate identical resistor values. It can be shown that in spite of the nonlinear relationship between current and voltage of an MOS transistor, the current division function is inherently linear. The CDN is based on the linear current division principle, the basic circuit of which is depicted in Fig. 3 [5]. Voltage V is a dc voltage and may have any value as long as the transistors are in the on state. The input current is divided into two currents, I_{d1} and I_{d2}. The ratio of the two currents is given

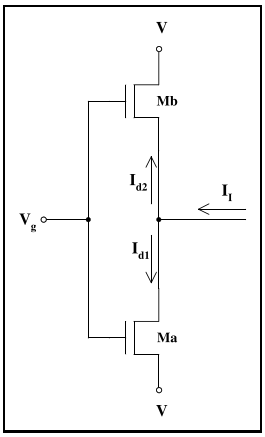

Fig. 3. The current division principle.

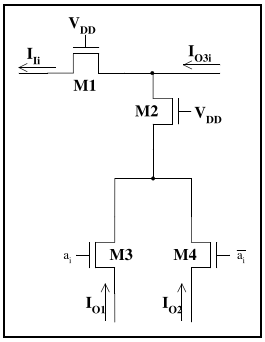

Fig. 4. The MOS ladder based CDC cell.

by:

$$\frac{I_{d1}}{I_{d2}} = \frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}} \tag{9}$$

This ratio is independent of the value of I_I, implying low distortion. Also, it is independent of the values of V_g and V. Finally, it is insensitive to second order effects like mobility degradation and body effect and independent of the operation region of the two MOS transistors. The MOS ladder based CDC is shown in Fig. 4. This CDC has an advantage over its resistor-based counterpart that the MOS transistors are used as switched and as resistive elements. That the MOS switch is a part of the network, while in the resistive ladder the MOS transistor is used only for switching the current and its resistance should be minimized as possible. Furthermore, in order to have finite input resistance, the MOS transistors should not operate in the saturation region. However, MOS ladder CDN still suffers from the drawbacks of the resistive ladder stated above such as the finite output resistance and the need for matching all the transistors in the circuit.

The proposed CDC is shown in Fig. 5. It is based on the differential pair instead of the ladder circuit. All transistors in the CDC are assumed to operate in the saturation or the off region. The transistor MA3 is always on while one of the transistors MA1 and MA2 is on and the other is off depending on the digital input a_i. The transistors MA4 and MA5 operate as the cascode transistors of the MA1 and MA2 respectively. The aspect ratios of the transistors MA4 and MA5 are assumed double that of the transistors MA1, MA2 and MA3 so that all the cascode transistors have the same aspect ratio and the channel length modulation effect is minimized. The differential pair of the next cell acts as the cascode transistor of MA3 except for the last cell (cell 0) in which a cascode transistor has to be added to the transistor MA3. Since the output currents are drawn from the drain of the transistors, the output resistance is very high. Hence, there is no need for virtual ground nodes. Consequently, the aspect ratios of the transistors can be chosen arbitrary to achieve the required current level without putting stringent requirement on the stage next to the CDN. Besides, only the transistors inside each CDC are required to be matched rather than matching all the transistors in the entire CDN. Hence the matching requirements are relaxed. Since the transistors are assumed to operate in the saturation region, higher current drive capability is expected than in the case of MOS ladder for the same aspect ratios of the transistors. Finally the circuit is independent of the body effect as sources of the transistors MA1, MA2 and MA3 are connected. Also the transistors M4 and M5 and the differential pair of the next CDC have the same gate voltage and the same current (while conducting), hence these transistors will have the same source voltages. The biasing voltages V_{Bi} ($i = 0, 1, 2, \ldots, n$) are generated from the circuit shown in Fig. 6. Where I_M is the maximum current that can flow in the CDN. The aspect ratio of the diode connected transistor MBi is given by:

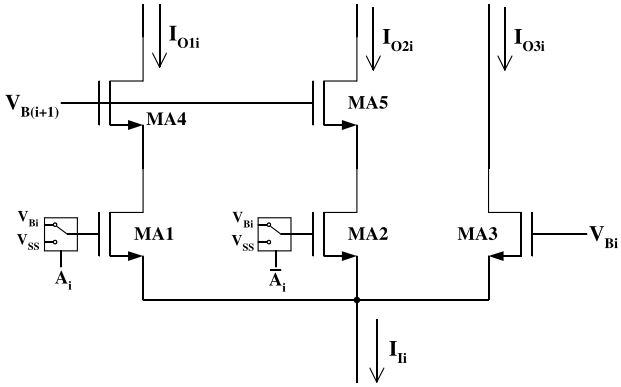

Fig. 5. The proposed CDC cell.

$$\frac{W_i}{L_i} = \frac{1}{\left(\sqrt{\frac{L_{i-1}}{W_{i-1}}} + \sqrt{\frac{L}{2W}}\right)^2} \tag{10}$$

This relation guarantees that the all the transistors in the CDN will remain in the saturation region as long as the current flowing in the CDN is less than I_M. A similar cir-

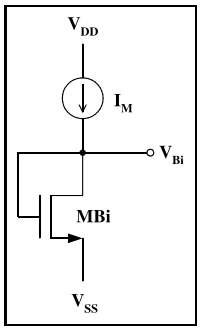

Fig. 6. The biasing circuit of the CDC cell.

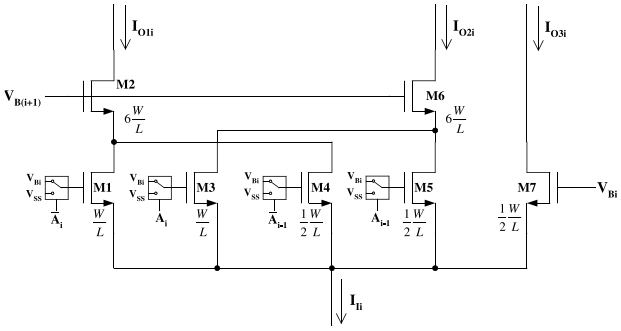

Fig. 7. 2-bit CDC cell.

cuit for the CDN$_P$ is realized using PMOS transistors. All simulations are preformed using $n = 6$. As n increases, V_{B0} increases and approaches the supply voltage. The minimum compliance voltage for proper operation of the CDN is given by:

$$V_{min} = \sqrt{\frac{I_I}{\mu C_{ox}\frac{W}{L}}}\left[\frac{1-\left(\frac{1}{\sqrt{2}}\right)^n}{1-\frac{1}{\sqrt{2}}}\right] \qquad (11)$$

To avoid this problem, wider transistors can be used in the CDC. A better solution is to use multi-bit CDC instead of the single-bit CDC proposed here. For example, a 2-bit CDC can be implemented as shown in Fig. 7. In this case the number of CDCs will be halved while the size of the CDC will be increased to more than double the original size. Hence the overall size of the CDN increases for the same n (total number of bits), however only half the original number of biasing voltages are required. Hence, up to 12 bits CDN can be obtained with supply voltages as low as ± 1.5 V. As the number of bits per CDC cell increases, the overall size of CDN increases dramatically as well as the number of transistors to be matched in each CDC cell. The proposed DCCC circuit has been simulated with PSpice using the AMI 1.2 µm CMOS technology provided by MOSIS. The aspect ratios of the transistors are given in Table 1. Supply voltages are ± 1.5 V and $n = 6$. Simulation is performed with the bodies of all transistors connected to the appropriate supply

Table 1. Values of α_1 and the corresponding digital inputs.

Transistors	Aspect ratios (W/L)
M1, M3	12/4.8
M2, M8	48/4.8
M5, M6	12/2.4
M4, M7	24/2.4
M9, M10, M11, M12	12/2.4
M13, M14, M15, m16	48/2.4
M17, M25, M26, M29, M30	120/2.4
M18, M24, M27, M28, M31	360/2.4
M20, M22, M23	4.8/4.8
M19, M21	12/4.8
MA1, MA2, MA3	120/4.8
MA4, MA5	240/4.8

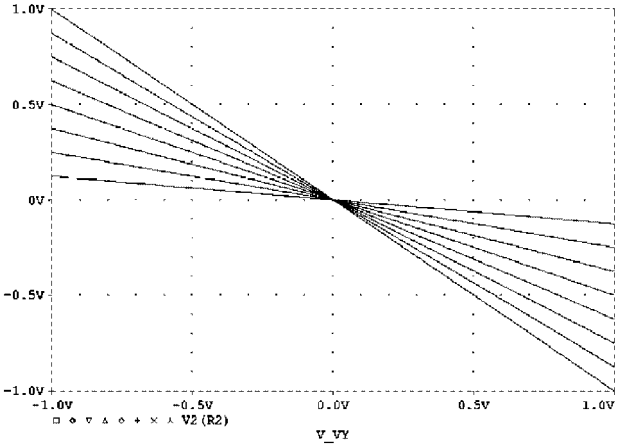

Fig. 8. Z terminal voltage for different values of α when $R_X = R_Z = 10\,\text{k}\Omega$.

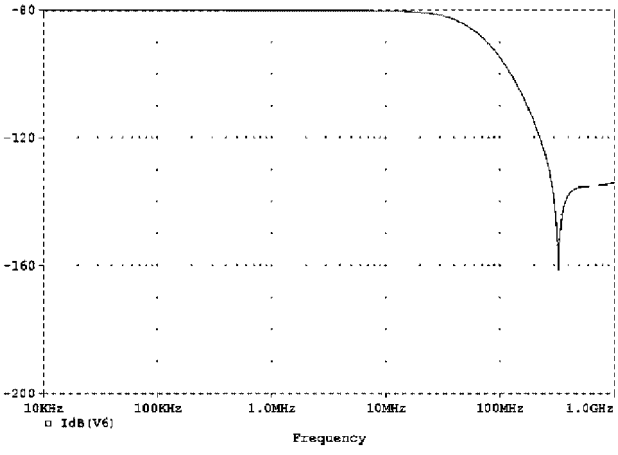

Fig. 9. Frequency response of the Z terminal current when $R_x = 10\,\text{k}\Omega$.

voltage. Fig. 8 shows the Z terminal voltage when V_Y is swept from -1 to 1 V and $R_X = R_Z = 10\,\text{k}\Omega$ for different values of the digitally controlled current gain parameter a ranging from 0.125 to 1 in steps of 0.125. The Z termi-

nal current frequency response is shown in Fig. 9 when $R_X = 10\,\text{k}\Omega$ and $a = 1$ from which it is seen that the bandwidth is about 40 MHz.

4. DB-Linear VGA

The DCCC can be used to implement a digitally controlled dB-linear variable gain amplifier (VGA) as shown in Fig. 10. The voltage gain is given by:

$$20\log\left(\frac{V_O}{V_I}\right) = \alpha_1|_{dB} - \alpha_2|_{dB} \tag{12}$$

A fully differential version of the proposed VGA is shown in Fig. 11. The differential mode gain is the same as that given by equation (12). To obtain fine gain control, a_1 is controlled from -5.25 to 0 dB with 0.75 dB step. a_2 is coarse controlled from 0 to -30 dB with 6 dB step. Hence the overall gain is controlled from -5.25 to 30 dB with 0.75 dB step. Tables (2) and (3) show the possible values of a_1 and a_2 and the corresponding digital inputs. As there are 48 step in the control range, only 6 control bits are required. The three least significant bits are used to control the value of a_1 while the three most significant bits are used to control the value of a_2. Two decoders can be used to decode the input gain control to the required control words given by tables 2 and 3. The proposed structure has the advantage that no common mode feedback is required. The gain of the VGA versus the input digital control word is shown in Fig. 12. The maximum gain error is less than 0.1 dB. The two balanced outputs of the proposed VGA are shown in Fig. 13 versus the differential input voltage when the gain is maximum (36 dB).

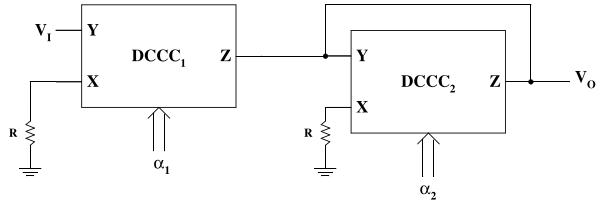

Fig. 10. The proposed digitally controlled VGA.

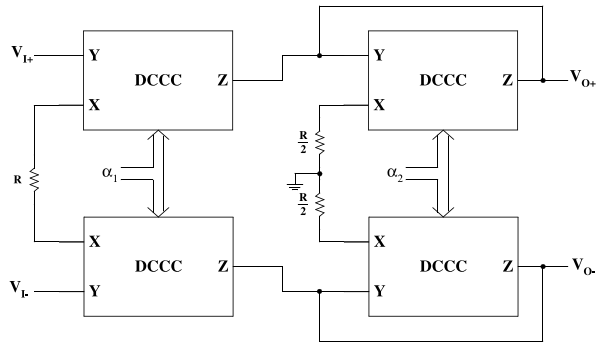

Fig. 11. Fully differential digitally controlled VGA.

Table 2. Values of α_1 and the corresponding digital inputs.

$\alpha_1\|_{dB}$	a5	a4	a3	a2	a1	a0
0	1	1	1	1	1	1
−0.75	1	1	1	0	1	0
−1.50	1	1	0	1	0	1
−2.25	1	1	0	0	0	0
−3.00	1	0	1	1	0	0
−3.75	1	0	1	0	0	1
−4.50	1	0	0	1	0	1
−5.25	1	0	0	0	1	0

Table 3. Values of α_2 and the corresponding digital inputs.

$\alpha_1\|_{dB}$	a5	a4	a3	a2	a1	a0
0	1	1	1	1	1	1
−6	0	1	1	1	1	1
−12	1	0	1	1	1	1
−18	1	0	0	1	1	1
−24	1	0	0	0	1	1
−30	1	0	0	0	0	1
−36	1	0	0	0	0	0

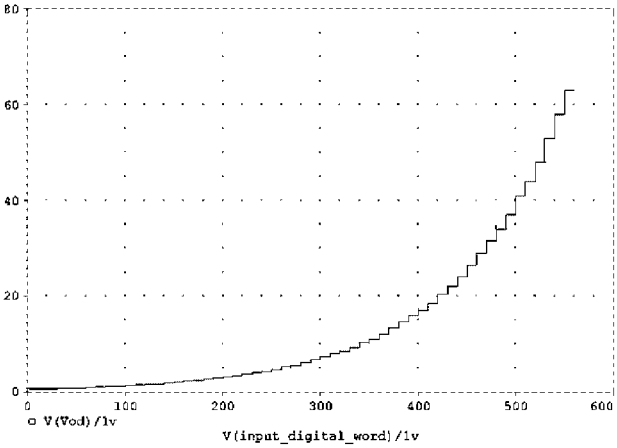

Fig. 12. Gain of the fully differential VGA versus input digital control word.

5. Digitally controlled impedance converter

Grounded digitally controlled impedance converter (DCIC) can be built from the proposed DCCC as shown in Fig. 14(a). The input impedance from the Y terminal is expressed as:

$$Z_I = \frac{Z}{\alpha} \tag{13}$$

Hence the input impedance is increased by a factor $1/\alpha$. A floating DCIC can be implemented as shown in Fig. 14(b). The expression of the input impedance is the

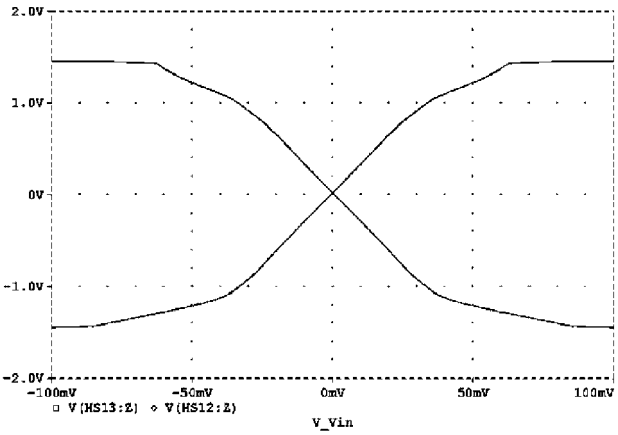

Fig. 13. The balanced output of the differential VGA versus the differential input at the maximum gain (36 dB).

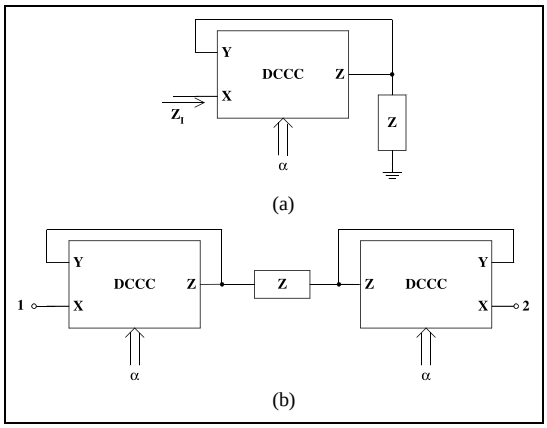

Fig. 14. Realization of DCIC (a) Grounded DCIC (b) Floating DCIC.

same as that given by equation (13). Another implementation of the impedance converter is shown in Fig. 15(a). The expression of the input impedance is given by:

$$Z_I = \alpha Z \tag{14}$$

Therefore the input impedance is decreased by a factor α. Similarly, a floating DCIC can be built as shown in Fig. 15(b).

6. Digitally tuned filters

Integrated active-RC filters offer much higher linearity than G_m-C filters. However, active-RC filters are not tunable; therefore, process and temperature variations in the values of R and C can not be compensated. Hence accurate frequency response characteristics can not be obtained. Switched-C filters can achieve this required linearity and accuracy, but suffer from increased power dissipation as frequency increases. This limits the use of these

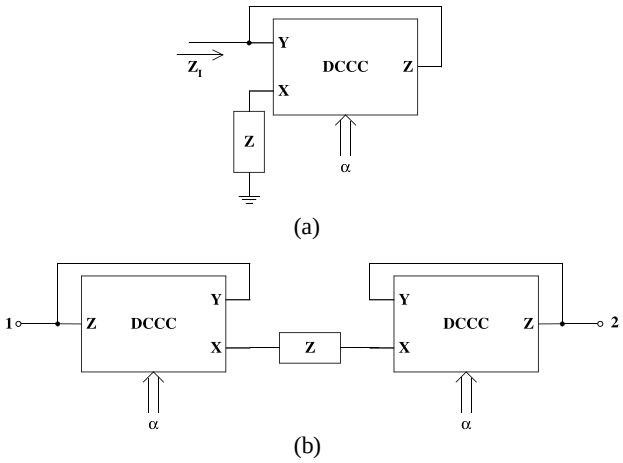

Fig. 15. Another realization of DCIC (a) Grounded DCIC (b) Floating DCIC.

filters to low frequencies. To achieve the required linearity and accuracy at high frequencies, the DCCC can be used together with the integrated resistors and capacitors. Temperature and process variations in the values of R and C can be compensated by choosing the current gain parameter α. Fig. 16 shows a second order filter. The transfer functions are given by:

$$\frac{V_{BP}}{V_I} = \frac{-\frac{\alpha_1(1-\alpha_4)}{C_1 R_3}s}{D(s)} \tag{15}$$

$$\frac{V_{LP}}{V_I} = \frac{\alpha_1\alpha_2(1-\alpha_4)C_1C_2R_2R_3}{D(s)} \tag{16}$$

where:

$$D(s) = s^2 + \frac{\alpha_1\alpha_3}{C_1R_1}s + \frac{\alpha_1\alpha_2(1-\alpha_4)}{C_1C_2R_2R_3} \tag{17}$$

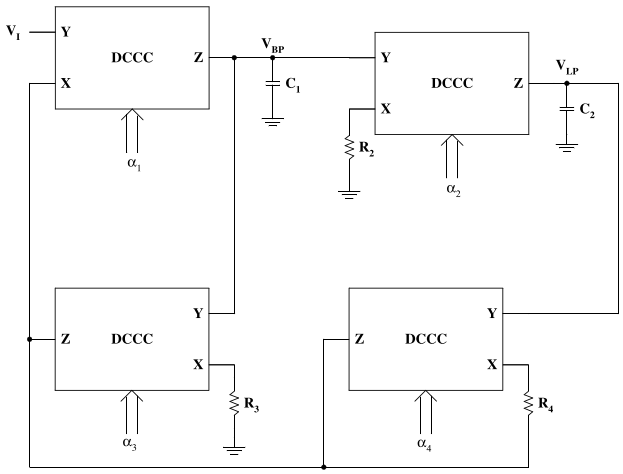

Fig. 16. The proposed digitally tuned filter.

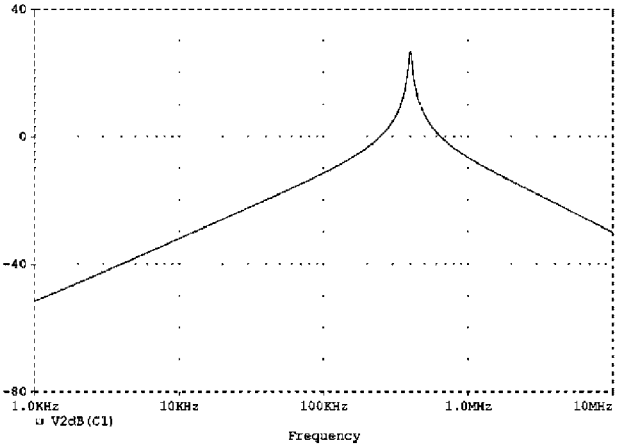

Fig. 17. Bandpass frequency response (Q=64).

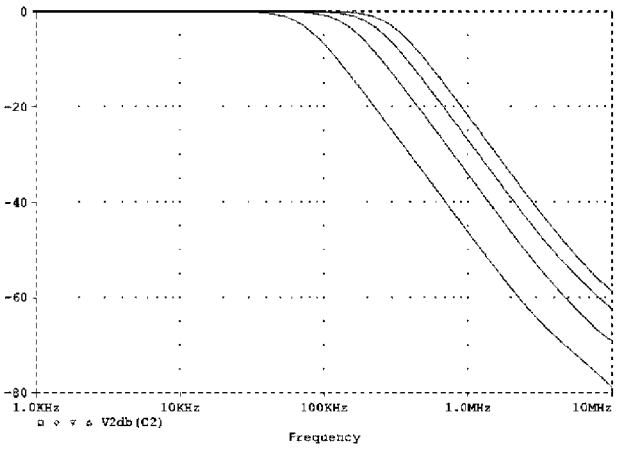

Fig. 18. Lowpass frequency responses for different cut-off frequencies.

then:

$$\omega_0 = \sqrt{\frac{\alpha_1\alpha_2(1-\alpha_4)}{C_1C_2R_2R_3}} \tag{18}$$

and:

$$Q = \sqrt{\frac{\alpha_2(1-\alpha_4)}{\alpha_1\alpha_3^2}\frac{C_1R_1^2}{C_2R_2R_3}} \tag{19}$$

Using equal R equal C design and choosing $\alpha_1 = \alpha_2 = \alpha$:

$$\omega_0 = \frac{\alpha\sqrt{1-\alpha_4}}{RC} \tag{20}$$

$$Q = \frac{1}{\alpha_3}\sqrt{1-\alpha_4} \tag{21}$$

Hence, independent control on ω_0 and Q is achieved. Where α controls the bandwidth, while α_3 controls the quality factor independently. The proposed filter has been simulated using $R = 20\,\text{k}\Omega$ and $C = 20\,\text{pF}$. Fig. 17 shows the bandpass frequency response when $\alpha_1 = \alpha_2 = 1$ and $\alpha_3 = \alpha_4 = 0.015625$. Hence a quality factor of about 64 is obtained with no spreading in the component values. Frequency response of the lowpass output is shown in Fig. 18 when $\alpha_3 = 1$, $\alpha_4 = 0.5$, $\alpha_1 = \alpha_2 = 0.25$ to 1 in steps of 0.25.

7. Conclusion

This paper presents a novel digitally controlled current conveyor (DCCC). The proposed block has been implemented using a folded cascode voltage follower with supply sensing technique to mirror the X terminal currents. A novel current division technique has been proposed to provide control on the current gain. To investigate the versatility of the proposed block, applications such as variable gain amplifiers, digitally tuned filters, and digitally controlled impedance converters have been presented.

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Ahmed A. El-Adawy was born in Cairo, Egypt, in 1974. He received the B.Sc. degree with honors in electronics and communications in 1997, andthe M.Sc. degree in 1999, both from Cairo University, Cairo, Egypt. His research interests include current-mode, mixed-mode signal processing, RF circuits, and wireless system design.

Ahmed M. Soliman was born in Cairo Egypt, on November 22, 1943. He received the B.Sc. degree with honors from Cairo University, Cairo, Egypt, in 1964, the M.S. and Ph.D. degrees from the University of Pittsburgh, Pittsburgh, PA., U.S.A., in 1967 and 1970, respectively, all in Electrical Engineering. He is currently Professor and Chairman Electronics and Communications Engineering Department, Cairo University, Egypt. From 1985–1987, Dr. Soliman served as Professor and Chairman of the Electrical Engineering Department, United Arab Emirates University, and from 1987–1991 he was the Associate Dean of Engineering at the same University. He has held visiting academic appointments at San Francisco State University, Florida Atlantic University and the American University in Cairo. He was a visiting scholar at Bochum University, Germany (Summer 1985) and with the Technical University of Wien, Austria (Summer 1987). In 1977, Dr. Soliman was decorated with the First Class Science Medal, from the President of Egypt, for his services to the field of Engineering and Engineering Education.

Hassan O. Elwan was born in Cairo, Egypt, in 1971. He received the B.Sc. degree (Honors) from the Electronics and Communication Department, Cairo University, Cairo, Egypt, in 1994. He received the M.Sc. degree in 1996 from the same university. He received the Ph.D. degree from Ohio State University, Columbus, OH, in 2001. Dr. Elwan's research interests include current-mode circuit design, filtering, mixed-mode systems, and wireless communications.