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New Wide Band Low Power CMOS Current Conveyors

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Abstract. New Class-A second-generation CMOS current conveyor (CCII) suitable for high frequency applications is proposed. It provides low input impedance and accurate voltage and current tracking. Targeting low power dissipation, the Class-AB version of the proposed Class-A architecture is introduced as well. Simulation results are included.

Key Words: wide band, low power, CMOS current conveyors, analog circuits

1. Introduction

In 1968 Smith and Sedra introduced the first generation current conveyor (CCI) [1] and in 1970 the second generation current conveyor (CCII) was proposed by the same two authors [2]. Since then, CCII has proved to be functionally flexible and versatile, rapidly gaining acceptance as both a theoretical and practical building block [3, 4]. The demand for accurate CMOS current conveyors suitable for high frequency applications has led analog designers to do extra efforts in finding CCII realizations that meet these requirements. Some of these realizations are proposed in [5–9]. Other realizations target higher accuracy but lose bandwidth in return [10].

In this paper, a new wide band CMOS CCII is proposed. The proposed realization is based on a new block diagram. Its voltage follower section is based on a cascade of two voltage followers. The first one is the flipped voltage follower proposed in [11]. Unfortunately, this voltage follower while standing alone suffers from a large voltage offset. By cascading another voltage follower to this one, this voltage offset is cancelled. Another advantage of the proposed CCII is that the voltage following is independent of the mismatches between the transistors. This is not the case in the differential pair based CCII realizations proposed in [5–8] which are affected by any mismatches in the differential pair transistors. The current following stage of the proposed CCII is made up of class-A branches and resembles that of Surakampontorn CCII proposed in [5] (Fig. 1). One more advantage of the proposed CCII is that it achieves wider voltage and current transfer bandwidths while keeping all other parameters as accurate as Surakampontorn CCII.

The demand for ever smaller and cheaper electronics systems has led manufacturers to integrate entire systems on a single chip. Therefore, systems employing digital and analog circuits on the same chip are common [12]. Analog cells used with digital systems must dissipate as little power as possible. The main reason behind this requirement is the large number of digital gates employed in most of today's integrated circuits applications.

Hence, the low power version of the proposed wide band CCII is presented in this paper. The power saving strategy is based on using low bias currents as well as using class-AB current following stage. The circuit dissipates very small standby power. At the same time, the circuit exhibits very wide open circuit voltage transfer bandwidth as well as comparable accuracy to its class-A counterpart and Surakampontorn CCII.

For all the circuits examined in this paper, the supply voltages are 1.5 and -1.5 V. TOP SPICE simulations were carried out with model parameters of 0.5 μm CMOS process provided by MOSIS (AGILENT).

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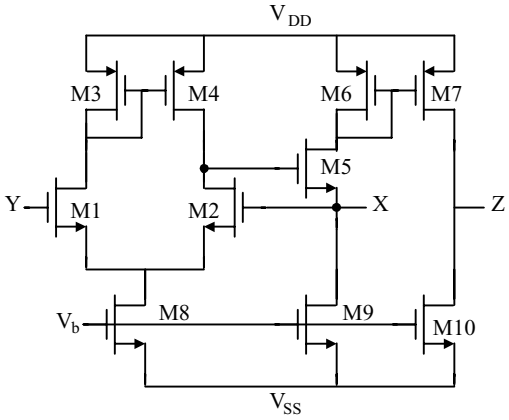

Fig. 1. Surakampontorn CCII realization [5].

2. New Wide Band CCII

2.1. Circuit Description

The CMOS realization of the proposed wide band CCII is shown in Fig. 2. The groups of the transistors (M_1 and M_2), (M_3 and M_4), (M_6 and M_7) as well as (M_9 and M_{10}) are matched. Assuming that all the transistors operate in their saturation regions, the operation of the circuit can be explained as follows. M_3, M_4, M_9, M_{10} and M_{12} serve as DC current sources holding equal currents of I_B. The circuit utilizes a differential pair (M_1 and M_2) to transfer V_Y to V_X. The voltage transfer occurs because the source terminals of M_1 and M_2 are at the same potential and they are biased by equal currents I_B.

The idea can be explained as follows. Figure 3(a) shows the flipped voltage follower proposed in [11].

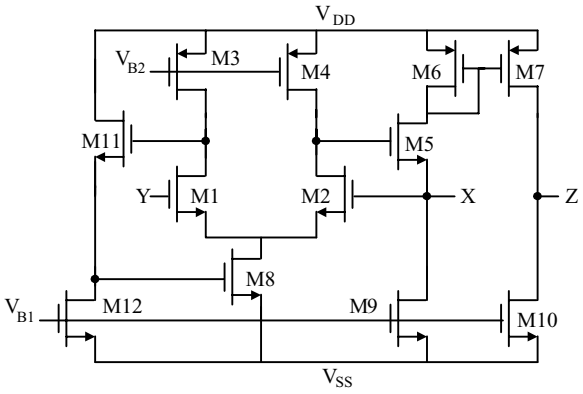

Fig. 2. The proposed wide band CCII.

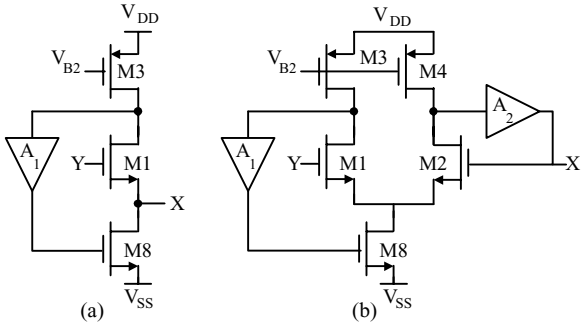

Fig. 3. (a) The flipped voltage follower. (b) The proposed voltage follower.

The circuit exhibits low input resistance at node X of about $1/(A_1 g_{m1} g_{m8} r_{ds3})$. However, there is a large voltage offset between the Y and X terminals that slightly exceeds one threshold voltage. This large offset can be compensated by adding another voltage follower in cascade as shown in Fig. 3(b).

A class-A CCII based on the voltage buffer shown in Fig. 3(b) is presented in Fig. 2. The gain A_1 is taken unity and is implemented by the source follower transistor M_{11}. Similarly, the gain A_2 is taken unity and is implemented by the source follower transistor M_5. A current mirror comprising M_6 and M_7 is added to convey the X terminal current to the Z terminal.

The equation of the voltage transfer gain is approximately given by:

$$\frac{v_x}{v_y} \approx \frac{1 + \frac{g_{d2}}{g_{m2}}}{\left(1 + \frac{g_{d1}}{g_{m1}}\right)\left(1 + \frac{g_{d2}+g_{d4}}{g_{m2}A_2}\right)} \tag{1}$$

It can be seen that the voltage transfer gain is very close to unity and independent of the mismatches between M_1 and M_2. However, when equal currents are used to bias M_3 and M_4, the matching between M_1 and M_2 is necessary to cancel the DC voltage offset between the Y and the X terminals.

The input resistance at terminal X is approximately given by:

$$r_x \approx \frac{r_{o2}(g_{d2} + g_{d4})}{g_{m2}A_2} \tag{2}$$

where r_{o2} is the output resistance of the amplifier A_2.

Table 1. Transistor aspect ratios of the circuit shown in Fig. 2.

Transistor	W (μm)/L (μm)
M_1, M_2	60/1
M_3, M_4	100/2.5
M_5, M_{11}	20/0.5
M_6, M_7	100/2.5
M_8	100/2.5
M_9, M_{10}, M_{12}	50/2.5

2.2. *Simulation Results*

The reference DC current source I_B is taken 100 μA. Transistors aspect ratios are reported in Table 1. The circuit is compensated by using capacitors $C_1 = 1.5$ pF (connected between the drain of M_2 and terminal X) and $C_2 = 5$ pF (connected between the drain of M_1 and V_{SS}). Simulation results are tabulated in Table 2 and shown in figures numbered from 4 to 7. These results can be described as follows. The input voltage range is from -0.63 to 0.25 V. The average value of the open circuit voltage transfer gain equals 0.99385. The voltage offset varies from -5.8 to 2.54 mV within the input voltage range. The open circuit voltage transfer bandwidth exhibits a 3-dB frequency of 1150 MHz (Fig. 4). The input current range equals 200 μA. The average value of the short circuit current transfer gain equals to 1.0037. The current offset varies from -1.04 to -0.023 μA within the input current range. The short

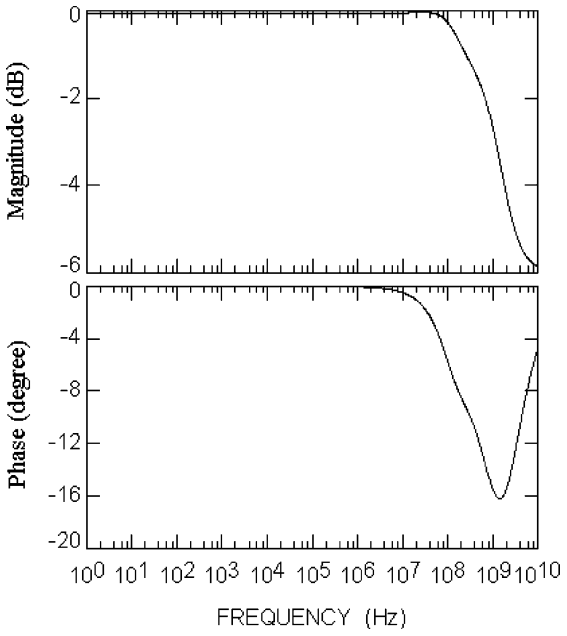

Fig. 4. Frequency characteristics of the open circuit voltage transfer gain between Y and X (V_X / V_Y) for the circuit shown in Fig. 2.

circuit current transfer bandwidth exhibits a 3-dB frequency of 76 MHz (Fig. 5). The input resistance at terminal X at D.C equals 5.9 Ω. Finally, the total harmonic distortion (THD) for an input sinusoid of frequency 100 kHz and amplitude 0.5 V p-p is 0.0919%.

To ensure the stability of the proposed architecture, the open loop circuit is simulated and the phase margin is calculated. The loop is opened by breaking the unity

Table 2. Parameters of the circuits shown in Figs. 1 and 2.

Parameter	Unit	Surakampontorn CCII [5]	Proposed wide band CCII
Input voltage range	V	-0.73 to 0.2	-0.63 to 0.25
A_v (average value)	–	0.99385	0.99385
Maximum deviation from A_v	–	0.5%	0.5%
Voltage offset variation	mV	-4.52 to 2.27	-5.8 to 2.54
F_{3db} of open circuit voltage transfer gain	MHz	776	1150
Input current range	μA	-100 to 100	-100 to 100
A_i (average value)	–	1.0037	1.0037
Maximum deviation from A_i	–	2.24%	1.96%
Current offset variation	μA	-1.04 to -0.0006	-1.04 to -0.023
F_{3db} of short circuit current transfer gain	MHz	66	76
R_x	Ω	5.9	5.9
THD for a sinusoid of 100 kHz 0.5 V p-p	–	0.09003%	0.0919%

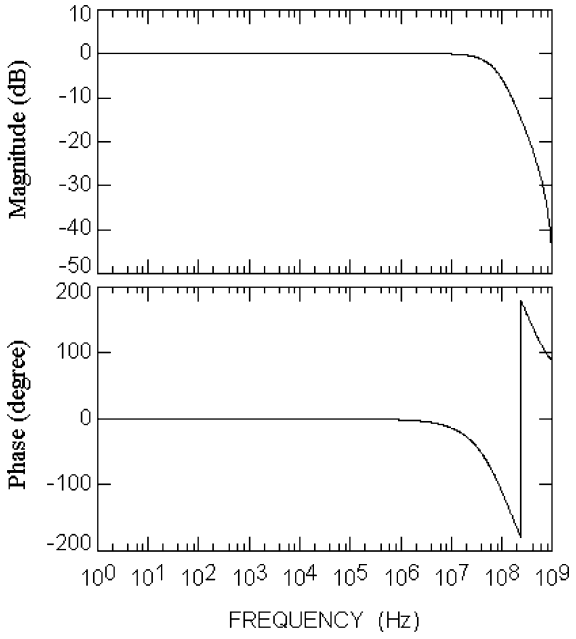

Fig. 5. Frequency characteristics of the short circuit current transfer gain between X and Z^+ (I_Z^+/I_X) for the circuit shown in Fig. 2.

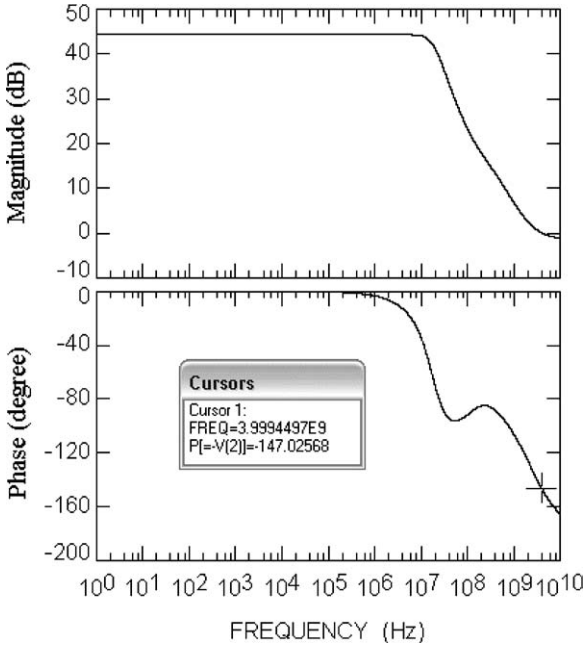

Fig. 6. Open Loop frequency response of the circuit shown in Fig. 2.

shunt feedback that exists from the X terminal to the gate of M_2. A test signal (V_T) is put on the gate of M_2. The gate of M_1 which is the Y terminal is shunted to ground. The open loop gain is $-V_X/V_T$. Figure 6 shows the open loop frequency response of the circuit. The cursor indicates a phase margin of 33 degrees.

Also, the transient response of the closed loop circuit is simulated for an input square wave at terminal Y. The input square wave has 0.8 V peak to peak amplitude, 1 MHz fundamental frequency and 1 ns rise/fall times. The output at terminal X is shown in Fig. 7. It can be noticed that it represents a faithful replica of the input square wave with no overshoots or oscillations.

The strength of the proposed wide band CCII is proved by the following comparison. The proposed CCII and Surakampontorn CCII are designed such that a fair comparison can be held between them. For the two circuits, supply voltages are the same (1.5 and −1.5 V), aspect ratios of equivalent transistors are equal and equivalent current sources are identical. By examining Table 2, one can easily notice what follows. The proposed CCII exhibits more open circuit voltage transfer bandwidth than Surakampontorn CCII. The open circuit voltage transfer 3-dB frequency increased from 776 MHz to 1150 MHz. It also features a short circuit current transfer bandwidth that slightly exceeds that of

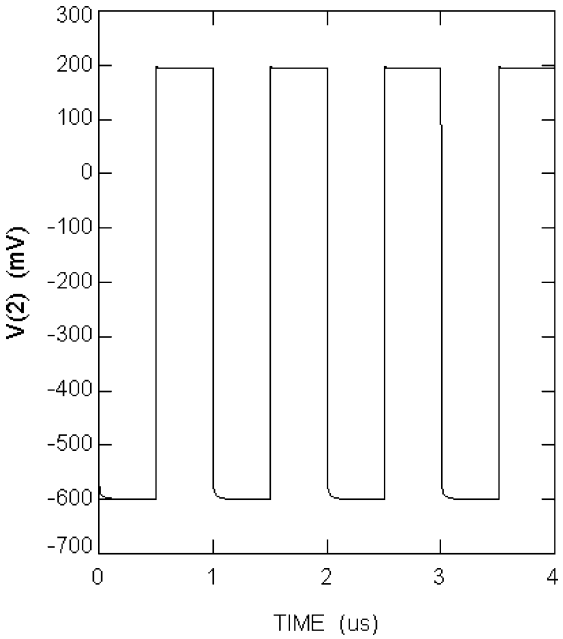

Fig. 7. The transient response of the circuit shown in Fig. 2.

Surakampontorn CCII. The short circuit current transfer 3-dB frequency increases from 66 to 76 MHz. At the same time, the proposed CCII showed almost the same results regarding all other aspects of comparison.

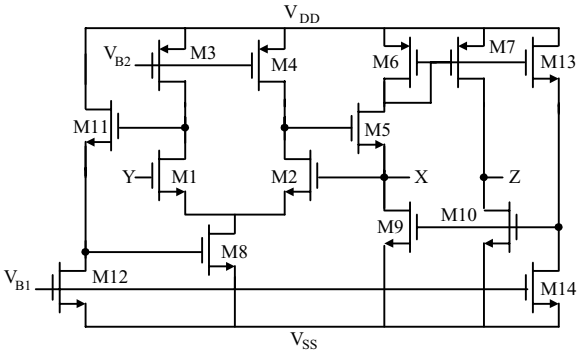

Fig. 8. Low power version of the new wide band CCII.

3. Low Power Version of the New Wide Band CCII

3.1. Circuit Description

The proposed CCII shown in Fig. 2 withdraws large standby currents. This is due to the class-A mode of operation where the constant current sources formed from M_9 and M_{10} result in unnecessary power dissipation in the standby mode. Figure 8 represents the proposed class-AB CCII circuit. The approach of converting a class-A CCII to its class-AB version was used by Elwan and Soliman in [12]. The same approach is adopted here. (M_6 and M_9) form the push-pull X terminal stage while (M_7 and M_{10}) form the push-pull Z terminal output stage. Transistors M_{13} and M_{14} form a level shifting stage that provides proper biasing for M_9 and M_{10}. If current is withdrawn from the X terminal then the gate voltages of M_6 and M_9 are lowered. Thus, the current through M_6 increases while that through M_9 decreases. Similarly, if the X terminal is required to sink current, then the gate voltages of M_6 and M_9 increase causing the current through M_6 to decrease and through M_9 to increase. This push-pull action of transistors M_6 and M_9 help in reducing the power dissipation. To prevent cross-over distortion both transistors M_6 and M_9 must remain ON when no current is drawn from the X terminal (standby), yet this current should be small to decrease the standby power dissipation. This is achieved by proper design of the level shifting stage (M_{13} and M_{14}). The circuit is biased by the DC current sources implemented by M_3, M_4, M_{12} and M_{14}. M_3, M_4 and M_{12} hold I_B each, while M_{14} holds $2I_B$. Although M_{12} and M_{14} are biased by the same DC voltage (V_{B1}), a separate circuit can be used to bias M_{14}. This technique supported by detailed analysis of the biasing circuit and the standby current is reported by Elwan and Soliman in [12].

3.2. Simulation Results

To minimize the power dissipation, the reference DC current I_B is taken 10 μA. Transistors aspect ratios are reported in Table 3. The circuit is compensated by using capacitors $C_1 = 1$pF (connected between the drain of M_2 and terminal X) and $C_2 = 5$pF (connected between the drain of M_1 and V_{SS}). Simulation results are tabulated in Table 4 and shown in figures numbered from 9 to 13. These results can be described as follows. The input voltage range is from -0.63 to

Table 3. Transistor aspect ratios of the circuit shown in Fig. 8.

Transistor	W (μm)/L (μm)
M_1, M_2	60/1
M_3, M_4	10/2.5
M_5, M_{11}	4/0.5
M_6, M_7	100/2.5
M_8	5/2.5
M_9, M_{10}	50/2.5
M_{12}	5/2.5
M_{13}	2.5/2.5
M_{14}	10/2.5

Table 4. Parameters of the circuit shown in Fig. 8.

Parameter	Unit	Results
Input voltage range	V	-0.63 to 0.34
A_v (average value)	–	0.99437
Maximum deviation from A_v	–	0.5%
Voltage offset variation	mV	-5.1 to 1.22
F_{3db} of open circuit voltage transfer gain	MHz	>10,000
Input current range	μA	-100 to 100
A_i (average value)	–	1.006
Maximum deviation from A_i	–	0.5%
Current offset variation	μA	-0.94 to -0.01
F_{3db} of short circuit current transfer gain	MHz	32
R_x	Ω	15
THD for a sinusoid of 100 kHz 0.5 V p-p	–	1.34%

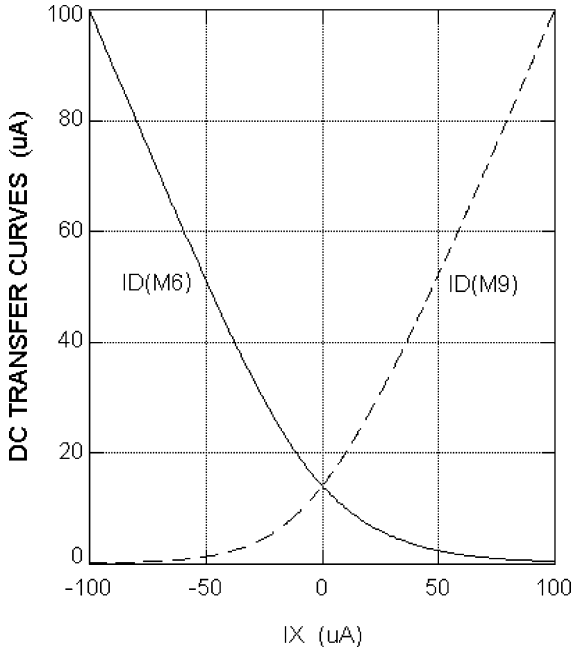

Fig. 9. The currents through M_6 and M_9 (push-pull).

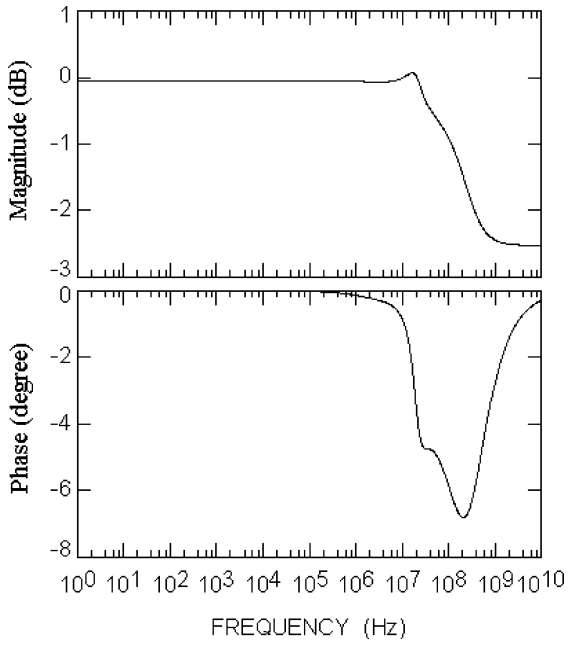

Fig. 10. Frequency characteristics of the open circuit voltage transfer gain between Y and X (V_X/V_Y) for the circuit shown in Fig. 8.

0.34 V. The average value of the open circuit voltage transfer gain equals 0.99437. The voltage offset varies from -5.1 to 1.22 mV within the input voltage range. Figure 9 shows the push-pull action of the class-AB operation. The circuit is designed to feature a standby current of 14 μA. The open circuit voltage transfer bandwidth exhibits a 3-dB frequency of more than 10 GHz (Fig. 10). The input current range equals 200 μA. The average value of the short circuit current transfer gain equals to 1.006. The current offset varies from -0.94 to -0.01 μA within the input current range. The short circuit current transfer bandwidth exhibits a 3-dB frequency of 32 MHz (Fig. 11). The input resistance at X at D.C equals 15 Ω. Finally, THD for an input sinusoid of frequency 100 kHz and amplitude 0.5 V p-p is 1.34%.

The stability of the proposed architecture is examined by simulating the open loop circuit. Figure 12 shows the open loop frequency response. The cursor indicates a phase margin of 89 degrees.

Moreover, the transient response of the closed loop circuit is simulated for an input square wave at terminal Y. The input square wave has 0.9 V peak to peak amplitude, 1 MHz fundamental frequency and 1ns rise/fall times. Figure 13 shows the output at terminal X. The

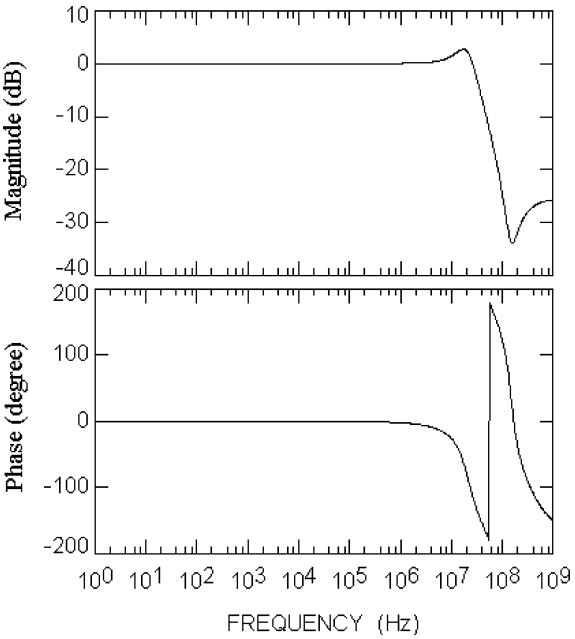

Fig. 11. Frequency characteristics of the short circuit current transfer gain between X and Z^+ (I_Z^+/I_X) for the circuit shown in Fig. 8.

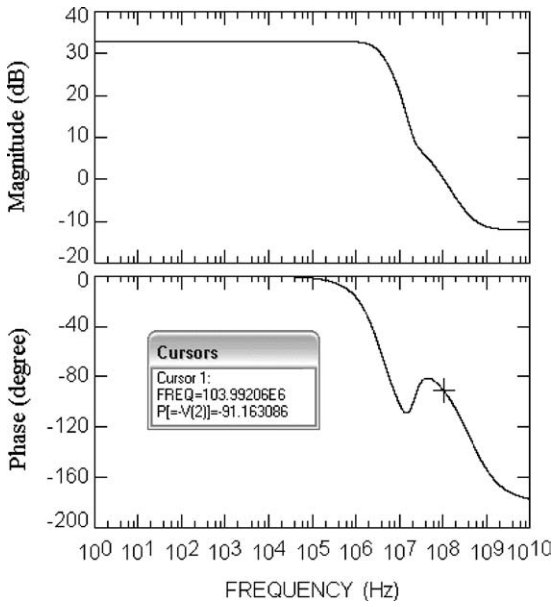

Fig. 12. Open Loop frequency response of the circuit shown in Fig. 8.

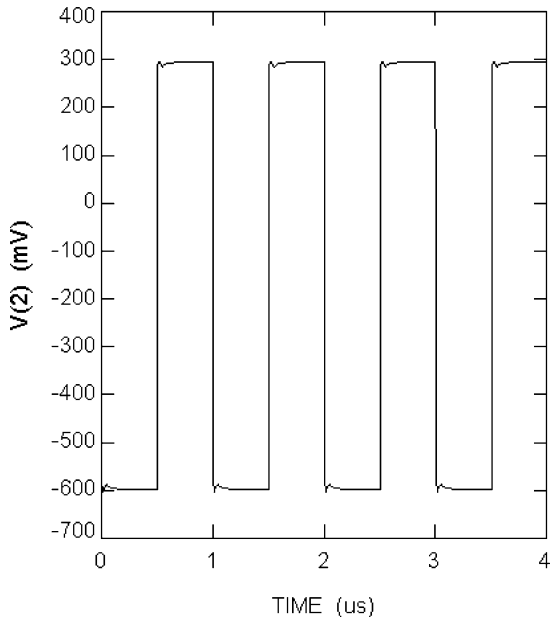

Fig. 13. The transient response of the circuit shown in Fig. 8.

output follows the input square wave with no significant overshoots or oscillations.

To conclude, the proposed circuit shows a very wide open circuit voltage transfer bandwidth. Moreover, it dissipates very low standby power of only 0.234 mW while its class-A version dissipates a standby power of 1.5 mW.

4. Conclusions

New class-A CMOS CCII suitable for high frequency applications was presented in this paper. Simulations results and a fair comparison between the proposed CCII and Surakampontorn CCII proved the strength of the proposed realization. Targeting a remarkable reduction in power dissipation, the low power version of the proposed wide band CCII was introduced as well. Simulation results showed the robustness of the introduced low power CCII.

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