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Low voltage fully differential CMOS voltage mode digitally controlled variable gain amplifier

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Abstract

In this paper, a voltage mode variable gain amplifier (VGA) is presented. A fully differential implementation is used to suppress the common mode noise and increase the dynamic range. The gain of the proposed VGA can be digitally controlled from 0 to 53 dB, with a 1 dB resolution. The gain control is performed in two stages; coarse control with a 6 dB resolution and fine control with a 1 dB resolution. Simulation shows that the bandwidth is about 15 MHz at the maximum gain (53 dB). The differential output third intercept point (OIP3) is 4 V. © 1999 Elsevier Science Ltd. All rights reserved.

Keywords: Voltage mode variable gain amplifier; Gain control; Differential output third intercept point

1. Introduction

Variable gain amplifiers (VGAs) are used in many applications in order to maximize the dynamic range of an overall system. Hearing aids [1], disk drives [2,3], and wireless communications are examples of such systems [4]. In a wireless communication system, the portability of the terminal implies that the received signal has a very wide dynamic range. This necessitates the use of an automatic gain control (AGC) circuit to automatically control the gain of the receive path so that the signal processed by the baseband circuitry appears to be of a constant power. The AGC contains two blocks: a variable gain amplifier (VGA) and the power detector which feeds back the control signal used to adjust the gain of the VGA. In modern wireless systems, all of the baseband signal processing is implemented digitally by a DSP processor. Hence, a primary requirement of the VGA is to be digitally controlled. Another requirement is that the gain should increase linearly on the decibel scale in order to achieve a wide gain control.

2. Circuit description

The block diagram of the proposed VGA is shown in Fig. 1. It consists of three stages: the input stage; the gain stage; and the output stage. The function of the input stage is to convert the differential input voltage into a differential current. This differential current is amplified by the gain stage where the gain is controlled from 0 to 48 dB in a 6 dB step via the digital control inputs D_0 through D_n. Finally the differential output current of the gain stage is converted back into the differential voltage through the output stage. The gain of the output stage can be controlled from 0 to 5 dB with a 1 dB step.

2.1. The input stage: voltage to current converter

The circuit schematic of the input stage is shown in Fig. 2. By applying KCL at node *a*,

$$I_1^+ = I_{M2} - I_{M3} = I_{M6} - I_{M4} = I_{R_1}. \tag{1}$$

Similarly

$$I_1^- = I_{M13} - I_{M12} = I_{M7} - I_{M9} = -I_{R_1}. \tag{2}$$

Because of the feedback loop formed from the transistor M5 and the transconductance amplifier A_1, the voltage V_a is equal to V_I^+. Similarly the voltage V_b is equal to V_I^-. Then,

$$I_{R_1} = \frac{V_a - V_b}{2R_1} = \frac{V_{Id}}{2R_1} \tag{3}$$

$$I_{1d} = I_1^+ - I_1^- = \frac{V_{Id}}{R_1} \tag{4}$$

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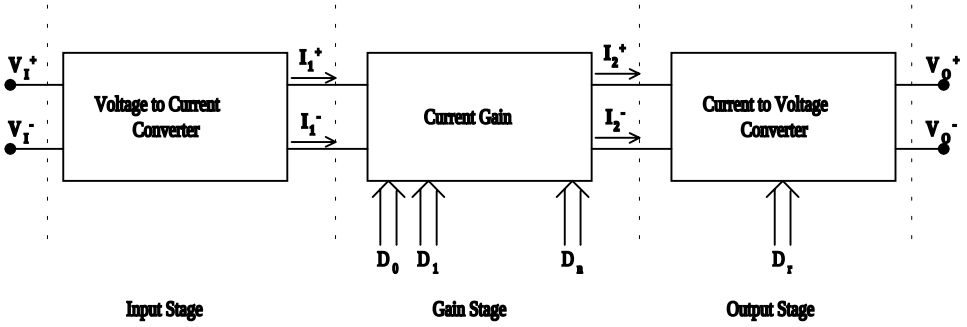


Fig. 1. The block diagram of the proposed VGA.

$$R_1 = R_{P1} + R_{M10} \quad (5)$$

where R_{P1} is the polysilicon resistor and R_{M10} the equivalent large signal resistance of the transistor M10. The purpose of adding this resistance is to obtain a gain which is independent of the process and temperature variations as explained in Section 2.3.

The transconductance amplifiers A_1 and A_2 are implemented using the traditional differential pair with an active load as shown in Fig. 3. The gain of the amplifier is given by:

$$\text{Voltage gain} = g_{M16}(r_{o16} // r_{o18}) \quad (6)$$

where g_{M16} is the transconductance of the transistor M16, r_{o16} and r_{o18} are the output resistances of the transistors M16 and M18, respectively. This voltage gain is high enough to make the two input voltages virtually at the same potential as assumed in Eq. (3).

2.2. The gain stage

In this stage, the differential currents I_1^+ and I_1^- are amplified using current mirrors. The gain stage consists of n current gain cells. Fig. 4 shows the circuit schematic of one such cell. The relative aspect ratios are shown beside each transistor. Cascode transistors are used to increase the output resistance and reduce the gain error. This allows us to use transistors with smaller L and hence reducing its effective capacitance and increasing the bandwidth. Also, cascode transistors are used for switching the current.

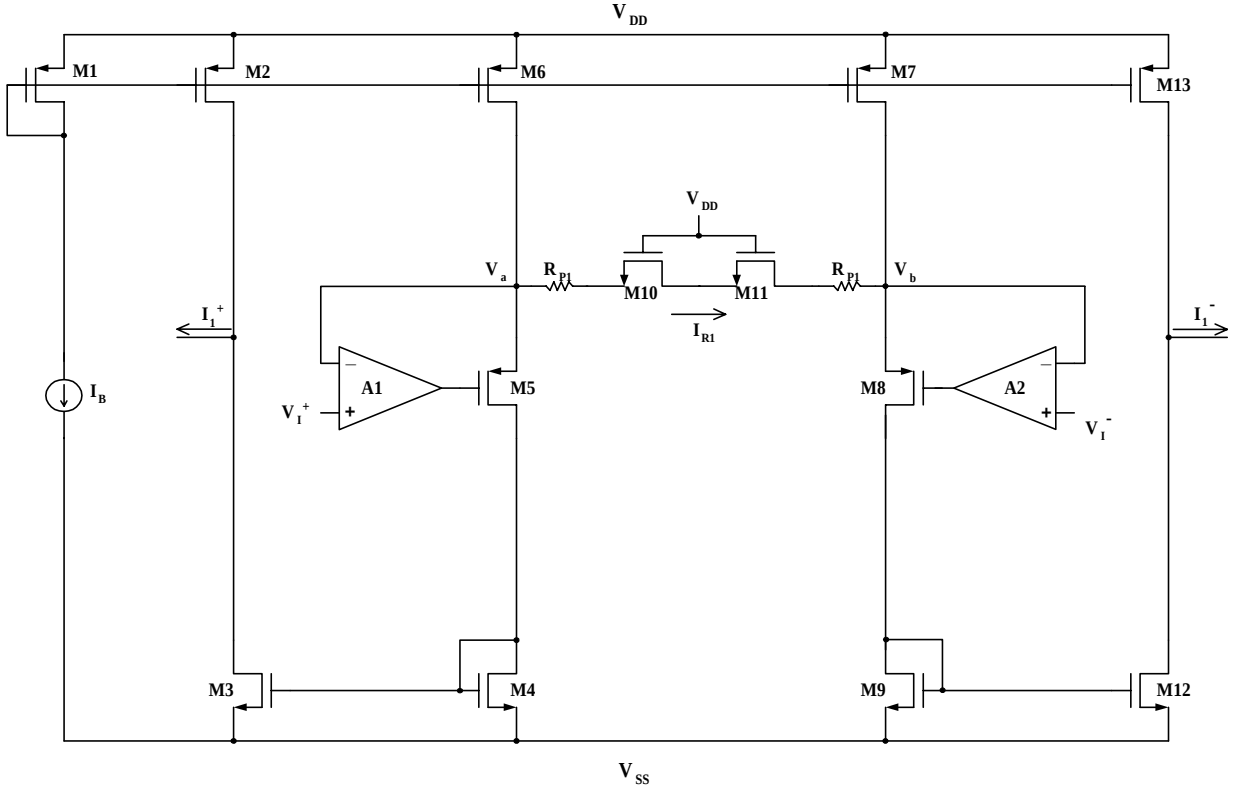


Fig. 2. The input stage (voltage to current converter).

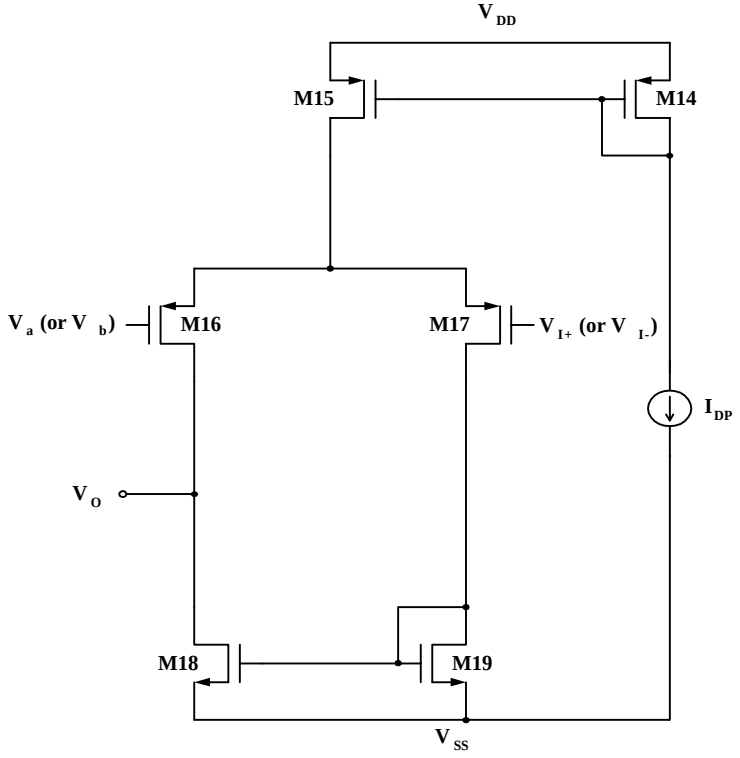


Fig. 3. The differential amplifier A_1 (or A_2) used in the input stage.

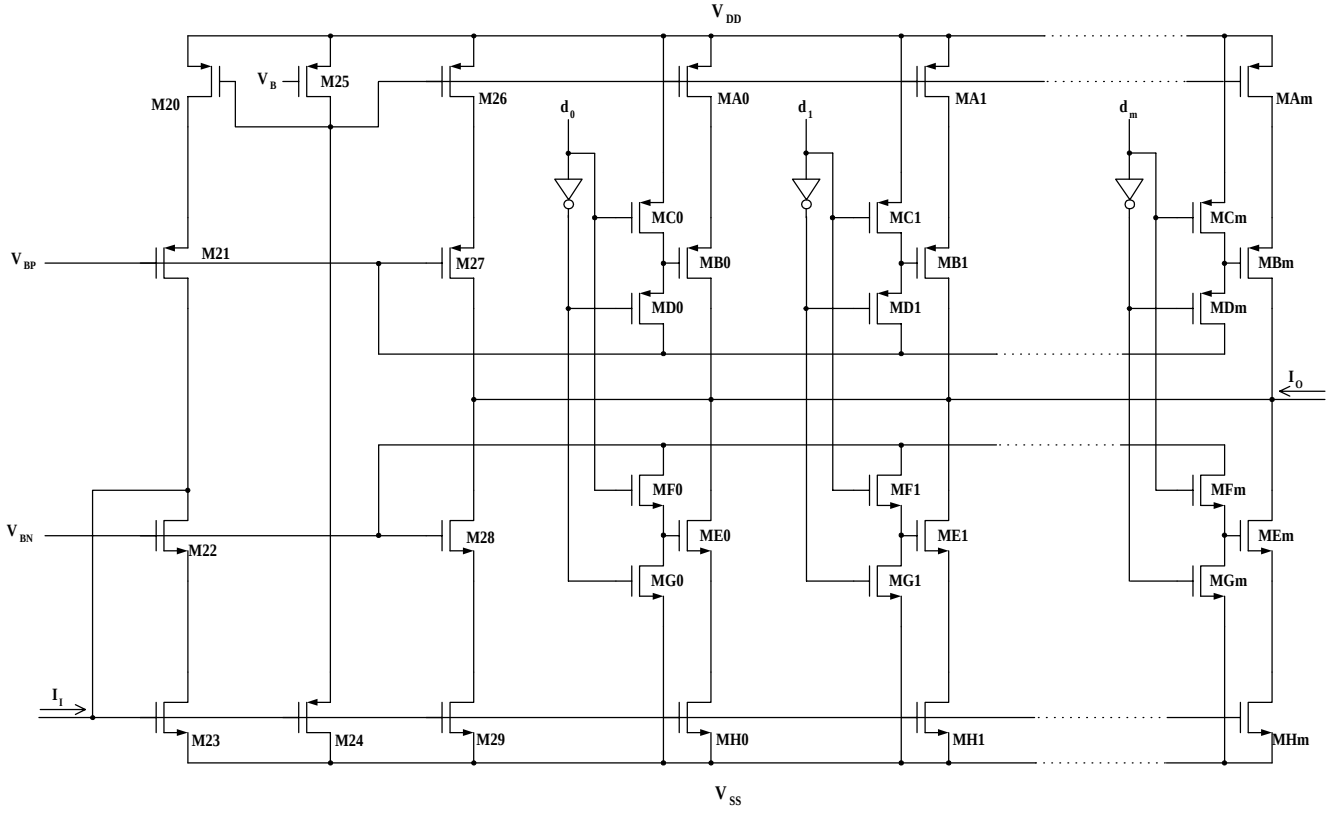


Fig. 4. The digitally controlled current amplifier (DCCA).

Table 1
Gains and the corresponding digital inputs of the DCCA ($m = 1$)

Gain (dB)	d_0	d_1
0	0	0
6	1	0
12	1	1

When the voltage at the gate of the NMOS (PMOS) cascode transistor is V_{BN} (V_{BP}) (i.e. $d_i = 1$), then the current is added to the output current, and when this voltage is V_{SS} (V_{DD}) (i.e. $d_i = 0$), then the current is switched off. Switching between V_{BN} (V_{BP}) and V_{SS} (V_{DD}) is achieved using NMOS (PMOS) transistors.

Hence,

$$I_O = I_I(1 + d_0 + 2d_1 + \cdots + 2^m d_m). \tag{7}$$

The maximum gain is obtained when $d_0 = d_1 = \cdots = d_m = 1$

$$\text{Max. gain/cell} = 2^{(m+1)} = 6(m + 1)\ \text{dB}. \tag{8}$$

Since the gain is controlled digitally, this circuit is called a Digitally Controlled Current Amplifier (DCCA).

Table 1 shows the possible gains and the corresponding digital inputs when $m = 1$. The complete schematic diagram of the gain stage that is used for each branch of the differential path is shown in Fig. 5. It consists of n cascaded current gain cells.

It is evident that the gain stage is inverting or noninverting if n is odd or even, respectively. Hence the output current is given by

$$I_{2d} = I_2^+ - I_2^- = (-1)^n D_1 D_2 \cdots D_n I_{1d}$$

$$= (-1)^n D_1 D_2 \cdots D_n \frac{V_{Id}}{R_1} \tag{9}$$

where

$$D_i = 1 + d_{i0} + 2d_{i1} + \cdots + 2^m d_{im} \qquad \text{for } i = 1, 2, \ldots, n. \tag{10}$$

From Eqs. (8) and (9), the maximum overall gain of the current gain stage is given by

$$\text{Max. gain} = 6n(m + 1)\ \text{dB}. \tag{11}$$

Thus for a given required overall gain, several values of m and n can be selected. This degree of freedom of selecting m and n can be used to optimize the performance, such as to increase the bandwidth, decrease the power consumption, or decrease the input referred noise. In the present case, an overall gain of 48 dB is required. Simulations showed that the bandwidth is maximized by choosing $n = 4$ and $m = 1$. Considering the power dissipation in the gain stage, it can be shown that the stand by current in the gain stage (neglecting the current flowing through the transistors M24 and M25) is expressed as

$$I_{SB} = \frac{n(\text{Max. gain})^{\frac{1}{n}}}{\left(\frac{1}{\sqrt{K_{20}}} + \frac{1}{\sqrt{K_{23}}}\right)^2}(V_B - V_{T23} - |V_{T20}| - V_{SS})^2. \tag{12}$$

It can be shown that the optimum noninteger value of n (to minimize I_{SB}) is given by

$$n_{\text{opt.}} = \ln(\text{Max. gain}). \tag{13}$$

In the present case, a maximum gain of 256 (48 dB) is required, hence the optimum theoretical value of n is 5.55. The value of n that is nearest to the optimum theoretical value given by Eq. (13) and results in an integer value of m from Eq. (11) is 4, hence $m = 1$. Fortunately, these are the same values that are used to maximize the bandwidth.

An significant issue is how to divide the required gain among the current gain cells. To minimize the input referred noise, it is better to increase the gain of the first cell until it reaches its maximum gain, then increase the gain of the second cell, and so on.

2.3. The output stage: current to voltage converter

The circuit schematic of the third stage is shown in Fig. 6.

$$V_{Od} = V_O^+ - V_O^- = (I_2^+ - I_2^-)R_2 = (-1)^n D_1 D_2 \ldots D_n \frac{R_2}{R_1} V_{Id} \tag{14}$$

$$\text{Gain} = (-1)^n D_1 D_2 \ldots D_n \frac{R_2}{R_1} \tag{15}$$

where R_2 is used to fine control the overall gain. Thus, the output stage adds to the gain of the VGA. The maximum gain of the output stage is 5 dB and the gain is digitally

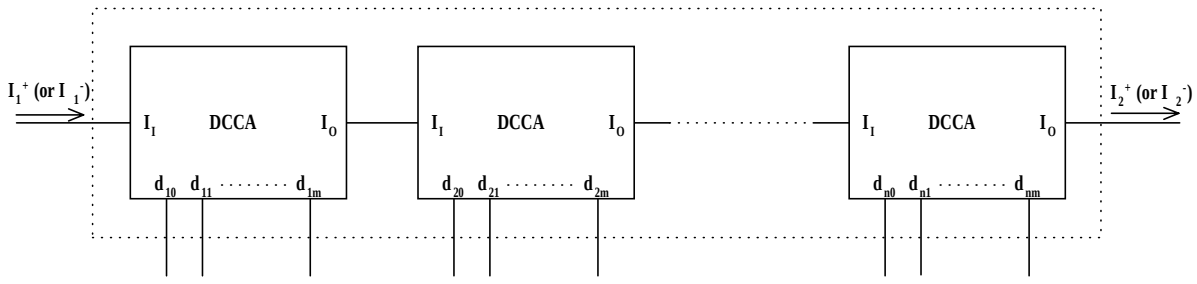


Fig. 5. The current gain stage.

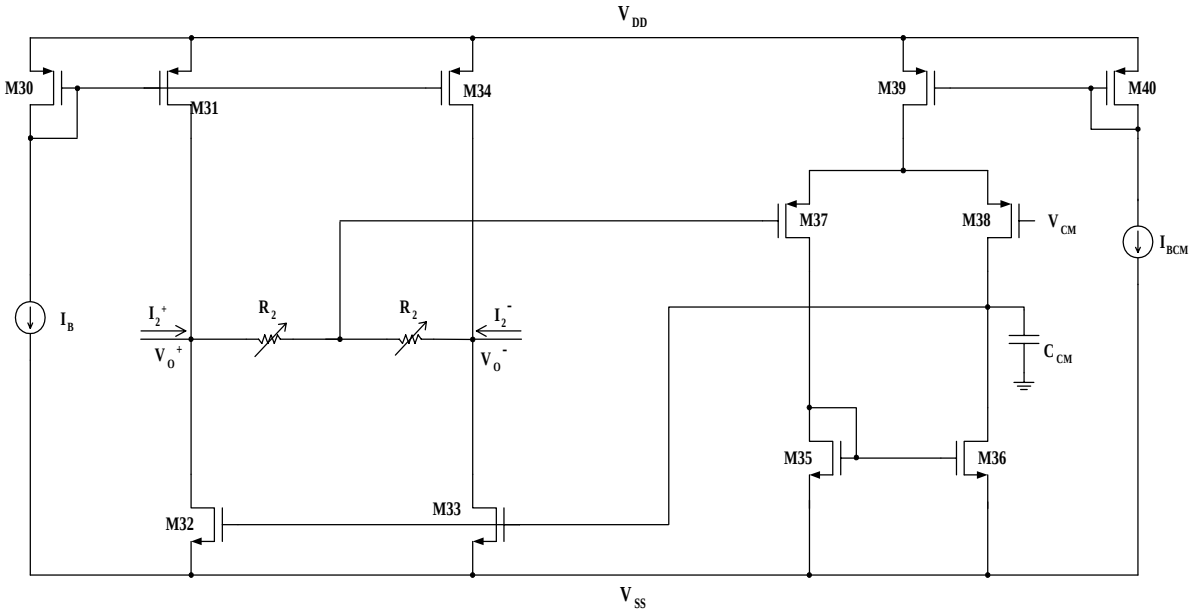
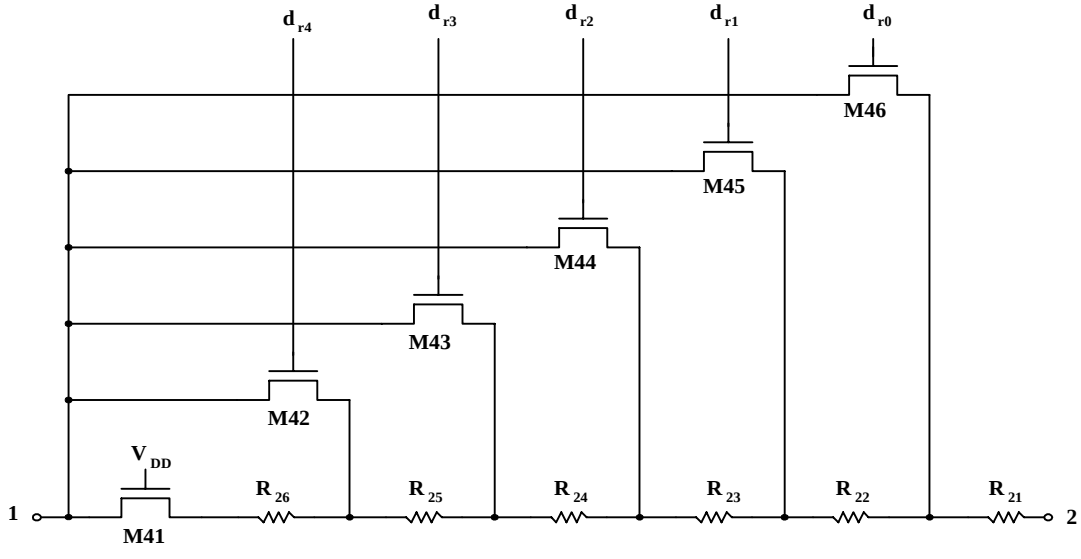


Fig. 6. The output stage.

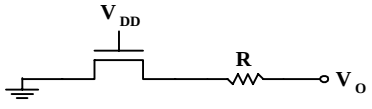
controlled with a 1 dB step via R_2 as shown in Fig. 7(a). The total resistance observed between the two nodes 1 and 2 is given by

$$R_2 = R_{21} + \bar{d}_{r0}(R_{22} + \bar{d}_{r1}(R_{23} + \bar{d}_{r2}(R_{24} + \bar{d}_{r3}R_{25}))) \quad (16)$$

where R_{2i} ($i = 1, 2, \ldots, 5$) are polysilicon resistors and d_{ri} are the digital inputs that control the value of R_2. Table 2 shows the values of these resistors in terms of R_1. The digital inputs and the corresponding gains are shown in Table 3. From this table, it is clear that the circuit shown in Fig. 7(a) reduces to



(a)



(b)

Fig. 7. (a) The digitally controlled resistor; and (b) simplified circuit for analyzing the equivalent resistance.

Table 2
Values of the resistors used to control R_2

Resistor	Value
R_{21}	R_1
R_{22}	$0.122R_1$
R_{23}	$0.137R_1$
R_{24}	$0.154R_1$
R_{25}	$0.172R_1$
R_{26}	$0.193R_1$

a resistor in series with an MOS transistor as shown in Fig. 7(b). This simplified circuit can be used to analyze the effect of the nonlinear MOS transistor as follows.

The equivalent input resistance that is seen from the V_O port is given by

$$R_{eq} = R + \frac{1}{K(V_{DD} - V_T)} + \frac{V_O}{2K(V_{DD} - V_T)^2(1 + KR(V_{DD} - V_T))^2} \quad (17)$$

$$R_{eq} = R(0) + \Delta R(V_O). \quad (18)$$

The first two terms in Eq. (17) represent the linear part of the equivalent resistor $R(0)$. The third term represents the nonlinear part because it depends on the applied voltage V_O. It can be shown that the maximum percentage nonlinearity (when $V_O = V_{DD}$) is given by

$$\text{Max. nonlinearity} = \frac{\Delta R(V_{DD})}{R(0)} = \frac{V_{DD}}{2(V_{DD} - V_T)(1 + KR(V_{DD} - V_T))^2}. \quad (19)$$

The presence of the quadratic term in the denominator makes it possible to achieve nonlinearity less than 0.01 with reasonable values of R and K. The value of K also affects the linear part of the resistor as shown in Eq. (17). This means that its value has to be taken into account in the gain calculations. In order to prevent the gain from process and temperature variations, two MOS transistors (M10 and M11) are added to the resistor R_1 as shown in Fig. 2. Although these transistors are never switched off, they are added to reduce the sensitivity of the gain to the process and temperature variations.

Table 3
Digital inputs and the corresponding gains of the output stage

Gain (dB)	d_{r0}	d_{r1}	d_{r2}	d_{r3}	d_{r4}
0	1	0	0	0	0
1	0	1	0	0	0
2	0	0	1	0	0
3	0	0	0	1	0
4	0	0	0	0	1
5	0	0	0	0	0

Table 4
Aspect ratios of the transistors

Transistor	Aspect ratio (W/L)
M1, M2, M6, M7, M13	48/4.8
M5, M8	192/4.8
M3, M4, M9, M12	48/4.8
M10, M11	48/1.2
M14, M15	96/2.4
M16, M17	48/2.4
M18, M19	24/2.4
M20, M21, M26, M27	96/2.4
M24, M25	4.8/4.8
M22, M23, M28, M29	24/2.4
M30, M31, M34	48/4.8
M32, M33	48/4.8
M35, M36	12/4.8
M37, M38, M39, M40	12/4.8
M41	27/1.2
M42	30/1.2
M43	34.2/1.2
M44	38.4/1.2
M45	42.6/1.2
M46	48/1.2

The transconductance amplifier (M35 through M40) and the feedback transistors M32 and M33 provide a common mode control. The time constant of the feedback loop is determined by the biasing current I_{BCM} and the capacitance C_{CM}.

3. Simulation results

The proposed VGA circuit was simulated with PSpice using the AMI 1.2 μm CMOS technology provided by MOSIS. The aspect ratios of the transistors are given in Table 4. Supply voltages are ± 1.5 V. Simulations are performed with the bodies of all transistors connected to the appropriate supply voltage, except for the transistors M5, M8 and M24 in which the body is connected to the corresponding source. This is applicable in an *N*-well technology. The biasing currents and voltages, the digital inputs, and the other parameters used in the simulation are shown in

Table 5
Different parameters used in the simulation

Parameter	Value
I_B	50 μA
I_{DP}	50 μA
R_1	4 kΩ
n	4
m	1
V_B	0.367 V
V_{BP}	− 0.408 V
V_{BN}	0.404 V
V_{CM}	0 V
C_{CM}	10 pF
I_{BCM}	0.1 μA

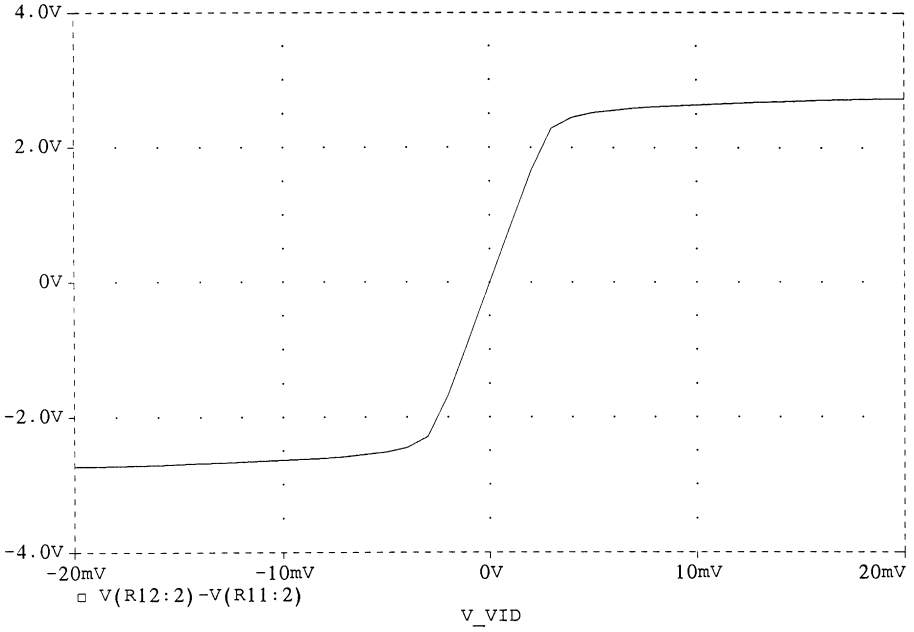


Fig. 8. The differential output voltage V_{Od} versus the differential input (gain = 53 dB).

Table 5. Fig. 8 shows the differential output voltage when the differential input is swept from − 20 to 20 mV, and the gain is 53 dB. Frequency response of the VGA is shown in Fig. 9, from which it is seen that the bandwidth is about 15 MHz for all gain values ranging from 5 to 53 dB with a 12 dB step. The simulated equivalent input density of white noise is 18 nV/$\sqrt{\text{Hz}}$ at the maximum gain (53 dB). The total power dissipation is 2.8 mW and the differential OIP3 is 4 V.

4. Conclusion

A 53 dB variable gain amplifier with a 1 dB step is designed. The overall gain is controlled in two steps: coarse gain control in the gain stage; and then the gain is fine controlled in the final output stage. The 3 dB bandwidth is about 15 MHz for the maximum gain. The proposed VGA consumes about 2.8 mW power and its equivalent input noise is 18 nV/$\sqrt{\text{Hz}}$ and has an OIP3 of 4 V.

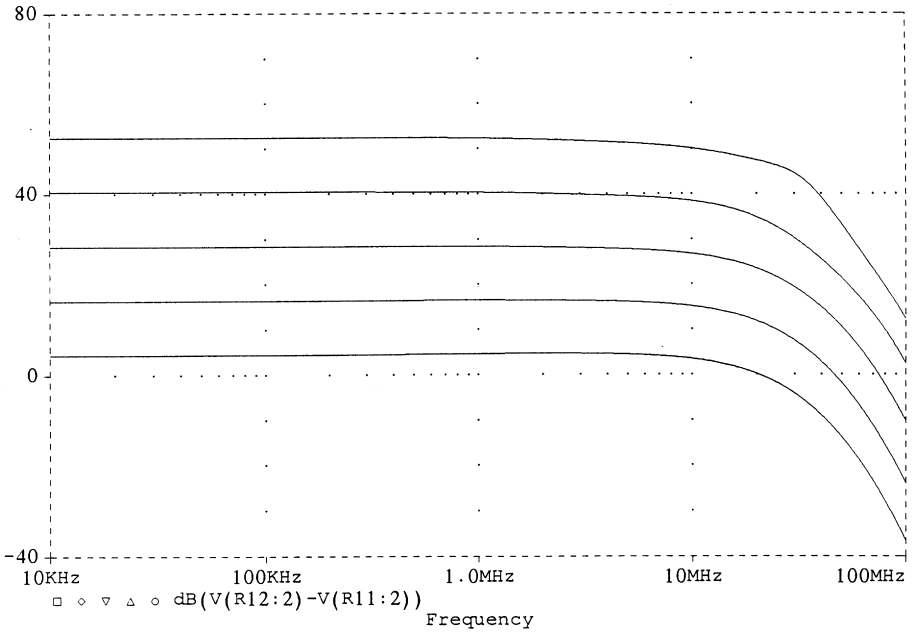


Fig. 9. The frequency response of the VGA with different gains (from 5 to 53 dB with a 12 dB step).

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