Analog Integrated Circuits and Signal Processing, 40, 75–82, 2004

A New CMOS Rail-to-Rail Low Distortion Balanced Output Transconductor

MOHAMED A. YOUSSEF AND AHMED M. SOLIMAN

Department of Electronics and Communication, Faculty of Engineering, Cairo University, Giza, Egypt
E-mail: asoliman@idsc.net.eg

Received August 3, 2002; Accepted February 24, 2003

Abstract. This paper presents a new CMOS transconductor providing low distortion for rail-to-rail signals. The circuit is based on using the anti-phase common source topology with the floating current source to extend its linearity range. The difference in the biasing currents of the floating current source is compensated to maintain the two output currents balanced by subtracting it at the output nodes. The proposed transconductor is suitable for applications requiring wide dynamic ranges. Rail-to-rail operation is achieved with THD less than −37 dB. The bandwidth achieved by the transconductor is 67.5 MHz using a supply voltage of ±1.5 V.

Key Words: transconductor, linearization, floating current source, anti-phase common source, low distortion, rail-to-rail

1. Introduction

Transconductors or linear voltage-to-current transformation circuits are one of the most important building blocks used for analog signal processing. They have received great attention since they are suitable for integration and can usually operate at high frequencies. Transconductors have a variety of applications such as: continuous time filters and four-quadrant multipliers [1, 2]. Many implementations have been reported in the literature in order to obtain a highly linear transconductor. Among them, the realizations based on the differential pair have received a great interest since they offer a relatively low level of distortion due to second order effects such as body-effect and mobility degradation [1–7].

In a new approach to design balanced output transconductors with extended linearity, the present techniques applied to linearize the transconductors based on the differential pair can be modified to extend the linearity of the floating current source (FCS) [8]. The dynamic biasing technique was applied to the FCS in [9] and [10] and rail-to-rail operation with total harmonic distortion (THD) less than −31 dB was reported. In this work, the new realization of the low distortion CMOS transconductor is based on the anti-phase common source topology, this technique offers the minimum THD resulting from second order effects (mainly body-effect and mobility degradation) [11].

The paper organization is as follows: Section 2 reviews the floating current source, then Section 3 describes how the input common mode is used to linearize the floating current source. In Section 4, simulation results are presented to demonstrate the wide linear range of the proposed circuit, and it is compared to the linear range of the FCS.

2. The Floating Current Source

The floating current source shown in Fig. 1 [8] provides two balanced output currents. This is always valid in order to satisfy Kirchoff's current law.

$$\begin{aligned} I_T &= I_T + I_{o1} + I_{o2} \\ I_{o1} &= -I_{o2} \end{aligned} \tag{1}$$

This circuit can be viewed as two differential pairs connected in parallel; an NMOS pair and a PMOS pair. For the NMOS pair assuming that M_1 and M_2 are matched and operate in the saturation region, it can be shown that:

$$I_1 - I_2 = v_d \sqrt{K_n} \sqrt{I_T - \frac{K_n v_d^2}{4}} \tag{2}$$

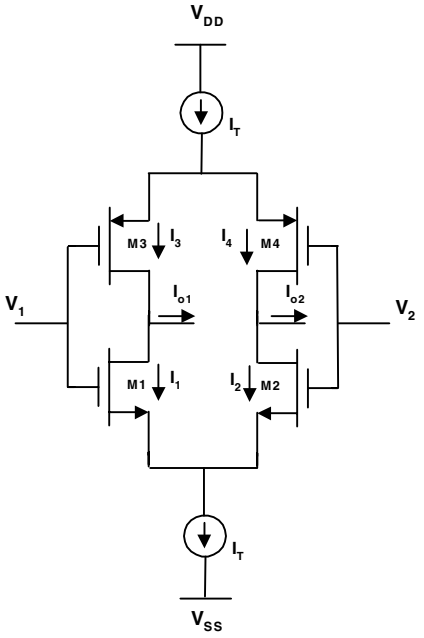

Fig. 1. Floating current source [8].

where I_T is the tail current, v_d is the differential input voltage, and K_n is the NMOS transconductance parameter given by:

$$v_d = V_1 - V_2 \tag{3}$$

$$K_n = \mu_n C_{\mathrm{OX}} \frac{W_1}{L_1} \tag{4}$$

Similarly for the PMOS pair, assuming that M_3 and M_4 are matched and operating in the saturation then:

$$I_3 - I_4 = -v_d \sqrt{K_p} \sqrt{I_T - \frac{K_p v_d^2}{4}} \tag{5}$$

where K_p is the PMOS transconductance parameter given by:

$$K_p = \mu_p C_{\mathrm{OX}} \frac{W_3}{L_3} \tag{6}$$

From Fig. 1, the two output currents can be expressed as:

$$\begin{aligned} I_{o1} &= I_3 - I_1 \\ I_{o2} &= I_4 - I_2 \end{aligned} \tag{7}$$

Using Eqs. (2), (5), and the fact that the two output currents are balanced:

$$\therefore \quad 2I_{o1} = I_3 - I_4 - (I_1 - I_2) \tag{8}$$

$$I_{o1} = -I_{o2} = -\frac{1}{2} v_d \left(\sqrt{K_n} \sqrt{I_T - \frac{K_n v_d^2}{4}} + \sqrt{K_p} \sqrt{I_T - \frac{K_p v_d^2}{4}} \right) \tag{9}$$

The output currents are affected by two nonlinear terms, which limits the linear range of the transconductor. This will be demonstrated in Section 4.

3. Circuit Topology for the Extended Linearity Transconductor

As previously noted, the FCS non-linearity is a result of the constant current drive. Instead of biasing the FCS with constant currents, a negative feedback stabilization action on the source nodes of the FCS is required by means of an amplifier stage, this feedback action forces the common node to track the input common mode voltage as shown in Fig. 2. Assuming all transistors operating in the saturation region, M_1 and M_2 are matched, M_3 and M_4 are matched, then the drain

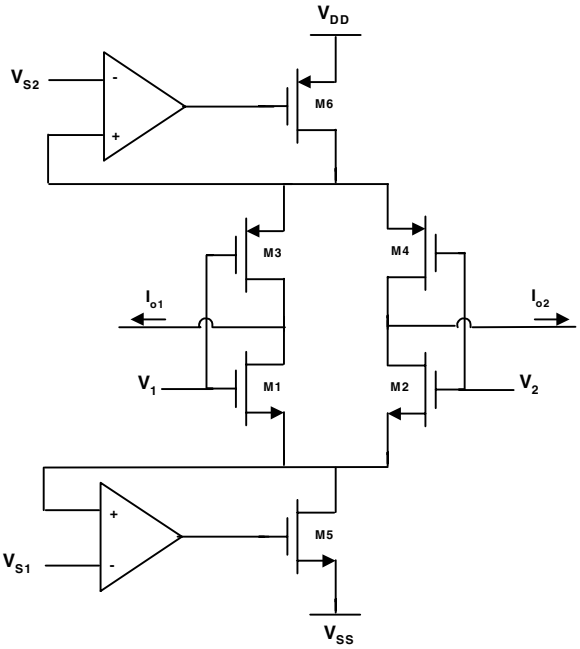

Fig. 2. The proposed transconductor circuit with feedback amplifiers.

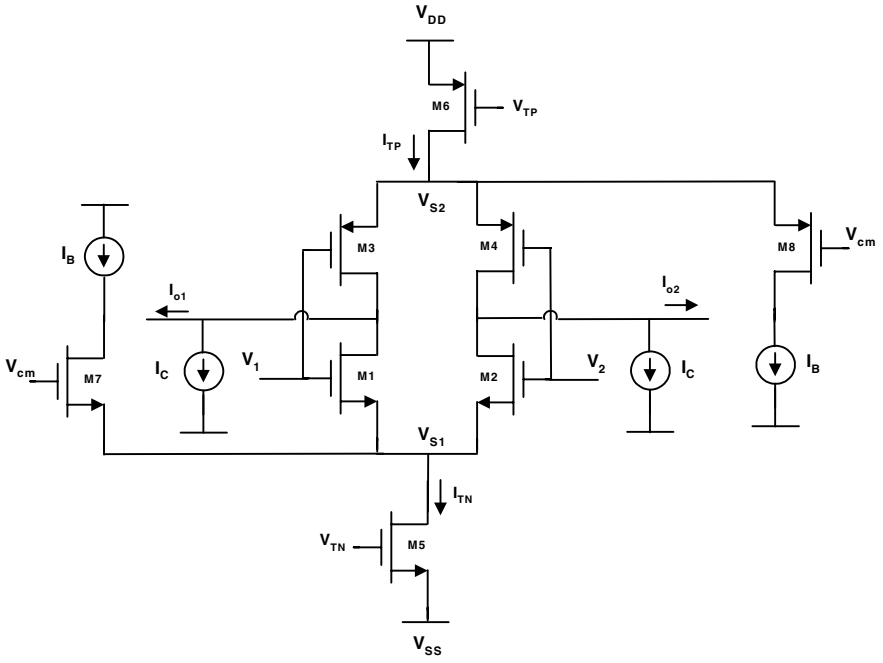

Fig. 3. The proposed transconductor circuit with the current feedback action.

currents are given by:

$$\begin{aligned} I_1 &= \frac{K_n}{2}(V_1 - V_{S1} - V_{\mathrm{TN}})^2 \\ I_2 &= \frac{K_n}{2}(V_2 - V_{S1} - V_{\mathrm{TN}})^2 \\ I_3 &= \frac{K_p}{2}(V_{S2} - V_1 - |V_{\mathrm{TP}}|)^2 \\ I_4 &= \frac{K_p}{2}(V_{S2} - V_2 - |V_{\mathrm{TP}}|)^2 \end{aligned} \tag{10}$$

where K_n is the transconductance parameter of M_1 and M_2, K_p is the transconductance parameter of M_3 and M_4. The differences between the two currents are given by:

$$\begin{aligned} I_1 - I_2 &= \frac{K_n}{2}(V_1 - V_2)(V_1 + V_2 - 2V_{S1} - 2V_{\mathrm{TN}}) \\ I_3 - I_4 &= -\frac{K_p}{2}(V_1 - V_2)(-V_1 - V_2 + 2V_{S2} - 2|V_{\mathrm{TP}}|) \end{aligned} \tag{11}$$

To obtain a linear relation between the currents and the differential input voltage, the two source voltages must be chosen as follows:

$$\begin{aligned} V_{S1} &= V_{\mathrm{CM}} - V_{B1} \\ V_{S2} &= V_{\mathrm{CM}} + V_{B2} \end{aligned} \tag{12}$$

where V_{CM} is the common mode of the input voltages given by:

$$V_{\mathrm{CM}} = \frac{(V_1 + V_2)}{2} \tag{13}$$

Then Eq. (11) becomes,

$$\begin{aligned} I_1 - I_2 &= K_n(V_1 - V_2)(V_{B1} - V_{\mathrm{TN}}) \\ I_3 - I_4 &= -K_p(V_1 - V_2)(V_{B2} - |V_{\mathrm{TP}}|) \end{aligned} \tag{14}$$

From Fig. 3 the two output currents can be expressed as:

$$\begin{aligned} I_{o1} &= I_3 - I_1 - I_C \\ I_{o2} &= I_4 - I_2 - I_C \end{aligned} \tag{15}$$

where I_C is a current subtracted from both output nodes to balance the output currents. The differential output current becomes:

$$\begin{aligned} I_{o1} - I_{o2} &= (I_3 - I_4) - (I_1 - I_2) \\ I_{o1} - I_{o2} &= -v_d[K_n(V_{B1} - V_{\mathrm{TN}}) + K_p(V_{B2} - |V_{\mathrm{TP}}|)] \end{aligned} \tag{16}$$

It is evident from Eq. (16) that the difference between the two output currents is a linear function of the differential input voltage. In this work, opamps are

not used to force the two common source nodes to follow the input common mode voltage. Instead a current feedback action is used to control the voltage of the common source nodes [6, 7]. This is shown in Fig. 3 where transistors M_7 and M_8 act as level shifters and force the common source nodes to track the input common mode voltage. To restore the balanced currents at the output nodes, a current I_C should be subtracted from both output nodes. To obtain an expression for this current it is noted from applying Kirchoff's current law to the modified FCS that:

$$\begin{aligned} I_{\mathrm{TN}} + I_{o1} + I_{o2} + 2I_C &= I_{\mathrm{TP}} \\ \therefore \quad I_C &= \frac{(I_{\mathrm{TP}} - I_{\mathrm{TN}})}{2} \end{aligned} \tag{17}$$

The two voltages V_{B1} and V_{B2} are related to the bias current I_B with the following equations:

$$\begin{aligned} V_{B1} &= \sqrt{\frac{2I_B}{K_{n1}}} + V_{\mathrm{TN}} \\ V_{B2} &= \sqrt{\frac{2I_B}{K_{p1}}} + |V_{\mathrm{TP}}| \end{aligned} \tag{18}$$

where K_{n1} and K_{p1} are the transconductance parameters of transistors M_7 and M_8, respectively. Using Eqs. (16), (18), and the fact that the output currents are balanced then the output currents can be expressed as:

$$I_{o1} = -I_{o2} = -\frac{v_d}{2}\sqrt{2I_B}\left(\frac{K_n}{\sqrt{K_{n1}}} + \frac{K_p}{\sqrt{K_{p1}}}\right) \tag{19}$$

The two voltages V_{TN} and V_{TP} in Fig. 3 are obtained through two feedback loops, which are responsible for deriving the necessary current in transistors M_5 and M_6. The aspect ratios of transistors M_7 and M_8 can be considered as design parameters to achieve the desired transconductance, but their choice affects the DC voltage at nodes V_{S1} and V_{S2}. It is desirable to choose them as small as possible since this will provide a higher transconductance, at the same time decrease the voltage at node V_{S1} and increase the voltage at node V_{S2}. This will give a bigger range for the input variations without turning off transistors M_1 to M_4. On the other hand, this will force a maximum value for the current source I_B.

To obtain the common mode voltage of the two inputs a common mode estimator circuit is used [6, 7]. The circuit diagram of the common mode estimator is shown in Fig. 4. It consists of two differential pairs (M_1, M_2) and (M_3, M_4). If both differential pairs are biased

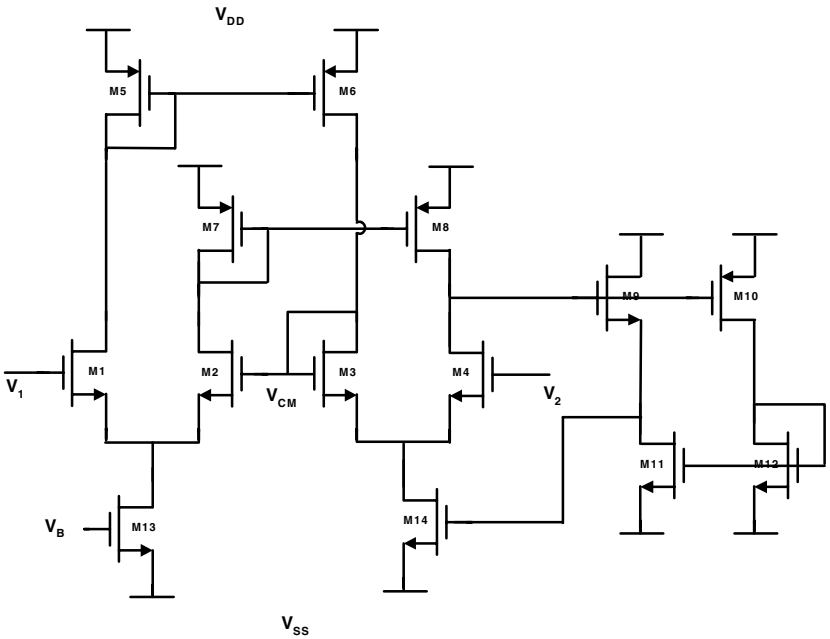

Fig. 4. Common mode estimator circuit [7].

using the same tail current and each branch current is equated to the corresponding branch current through the current mirrors (M_5–M_6) and (M_7–M_8), then the feedback applied will force the common input to the two differential pairs to a value satisfying the equality of the currents.

$$V_1 - V_{CM} = V_{CM} - V_2$$
$$\therefore \quad V_{CM} = \frac{V_1 + V_2}{2} \tag{20}$$

Instead of using a constant current source to bias the second differential pair its tail current is set through a negative feedback loop connected in such a way to equate the two tail currents. For example, if the current in M_{14} is higher than that of M_{13} then the current in M_8 will increase. This will reduce the gate voltage of M_9, the level-shifting transistor M_9 will cause a corresponding drop in the gate voltage of M_{14}. A similar action takes place if the current in M_{14} increases. So the negative feedback loop will force the current of M_{14} to track that of M_{13}. Even if M_{14} slightly enters the linear region both currents will still remain equal as long as the gate voltage of M_{14} can drive the necessary current. If the two inputs are fully differential then V_{CM} is simply a DC value applied to the gates of M_7 and M_8.

Figure 5 shows the transconductor circuit without the common mode estimator circuit. Transistors M_1, M_2, M_3, and M_4 form the main FCS. The currents flowing in the two biasing transistors M_5 and M_6 are obtained through a feedback action in order to stabilize the two node voltages V_{S1} and V_{S2}. M_5 is responsible for controlling V_{S1}, and M_6 is responsible for controlling V_{S2}. The transistors (M_9–M_{12}) and (M_{13}–M_{16}) perform the feedback action in order to bias the two transistors M_5 and M_6, respectively. Both V_{S1} and V_{S2} will still track the common mode input voltage even if the two transistors M_5 and M_6 slightly enter the linear region as long as these two transistors can drain the necessary currents for proper operation of M_1, M_2, M_3, and M_4. To obtain the current I_C both the currents of transistors M_5 and M_6 are subtracted and divided by two. The two transistor pairs (M_{17}, M_{18}) and (M_{19}, M_{20}) are added to ensure that transistors M_{21} and M_{22} replicate the exact currents of M_5 and M_6. This circuit will not be affected by the channel length modulation effect resulting from the two biasing transistors M_5 and M_6. This is due to the fact that the FCS is biased in this case by two voltages at the common source nodes and not by current sources.

4. Simulation Results

In order to compare the performance of both the FCS and the extended linearity transconductor, numerous computer simulations have been carried out using level 8 Spice parameters for a 0.5 μm process, with the supply voltages $\pm$1.5 V. To obtain a fair and accurate

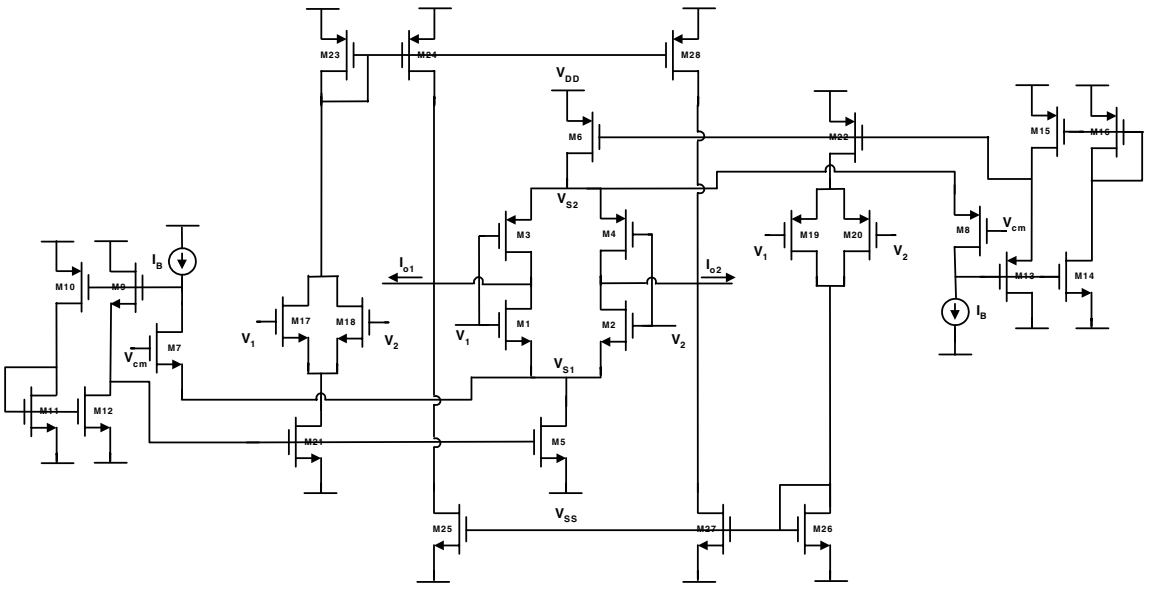

Fig. 5. Overall circuit diagram of the proposed low distortion transconductor.

Table 1. Aspect ratios of the transistors in Fig. 5.

Transistor	Aspect ratio μm/μm	Transistor	Aspect ratio μm/μm
M_1, M_2, M_{17}, M_{18}	5/3.5	M_{12}	1.5/0.5
M_3, M_4, M_{19}, M_{20}	15/3.5	M_{13}	4.5/0.5
M_5, M_{21}	150/3	M_{14}	2.5/0.5
M_6, M_{22}, M_{23}	150/3	M_{15}	4.5/0.5
M_7	0.5/3.5	M_{16}	3/5
M_8	1.5/3.5	M_{24}, M_{28}	75/3
M_9	1.5/0.5	M_{25}, M_{27}	25/3
M_{10}	7/0.5	M_{26}	50/3
M_{11}	1/5		

comparison the circuits presented in Sections 2 and 3 were designed to achieve the best linearity possible for a given transconductance value. The aspect ratios of the transistors in Fig. 5 are given in Table 1.

The following results were obtained while one of the inputs was grounded and the other was varied across the supply range. All substrate terminals were connected to the appropriate supply voltage, thus the body effect is taken into account. The two balanced output currents for the FCS are shown in Fig. 6, while those of the new extended linearity transconductor are shown in Fig. 7. It is evident that the range of operation of the proposed circuit extends from rail-to-rail, while that of the FCS is limited to ±0.5 V. This can also be demonstrated if the value of the transconductance is plotted as shown in Figs. 8 and 9. This range of operation exceeds the range achieved in [12], where the adaptive

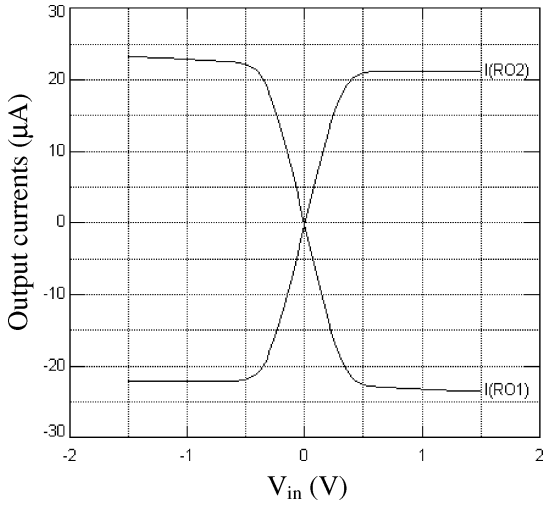

Fig. 6. Output currents of the FCS.

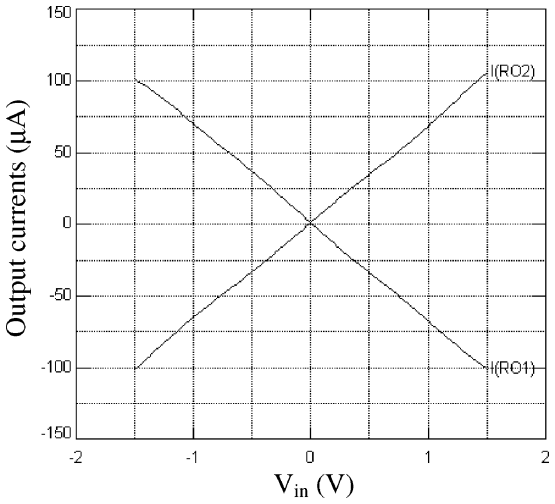

Fig. 7. Output currents of the extended linearity floating transconductor stage.

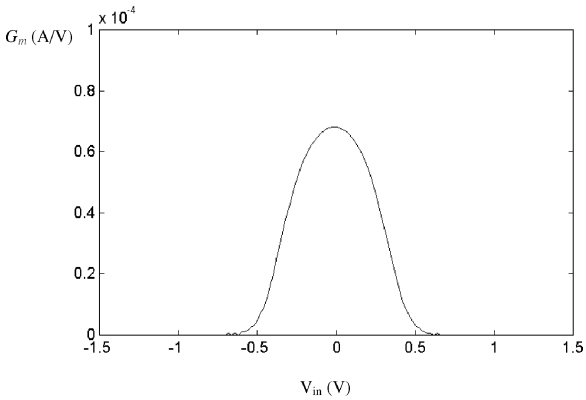

Fig. 8. Transconductance of the FCS.

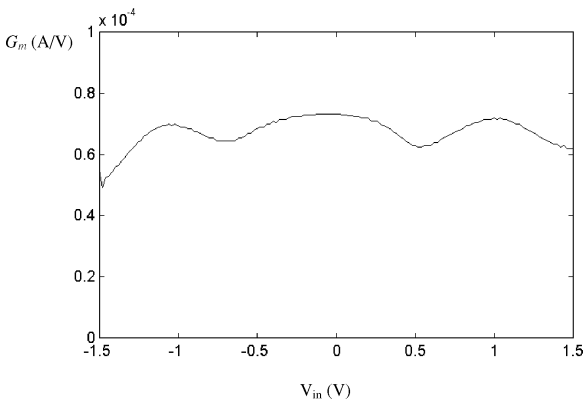

Fig. 9. Transconductance of the extended linearity transconductor.

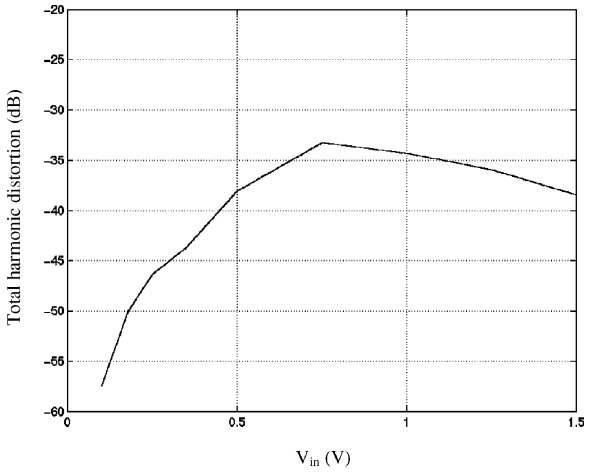

Fig. 10. THD plot versus the input amplitude.

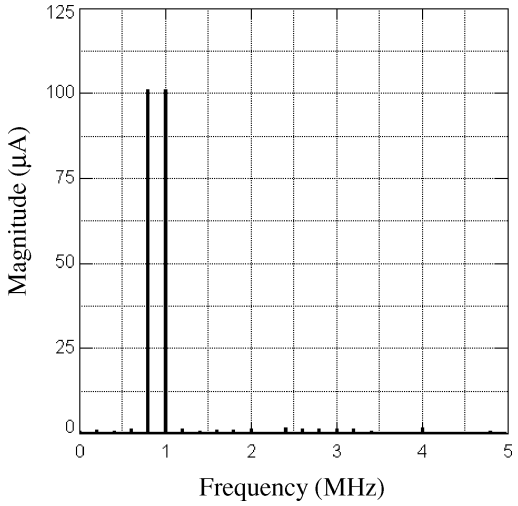

Fig. 11. The spectrum of the output currents when two tones are applied.

biasing and the source degeneration techniques were combined together to linearize a differential pair, in [12] the THD achieved was −37 dB for a 1 V input sinusoid while using a 3.3 V supply. In this work, the achieved THD of the output currents is less than −37 dB for a 1.5 V input sinusoid with 1 MHz frequency, which is a rail-to-rail input signal. The THD plot versus the input amplitude is shown in Fig. 10. Increasing the input amplitude increases the THD, but at higher values for the input signal the THD begins to fall until the input signal reaches the supply rail. This is due to the variations in the transconductance of the circuit. Furthermore, the linearity of the circuit was

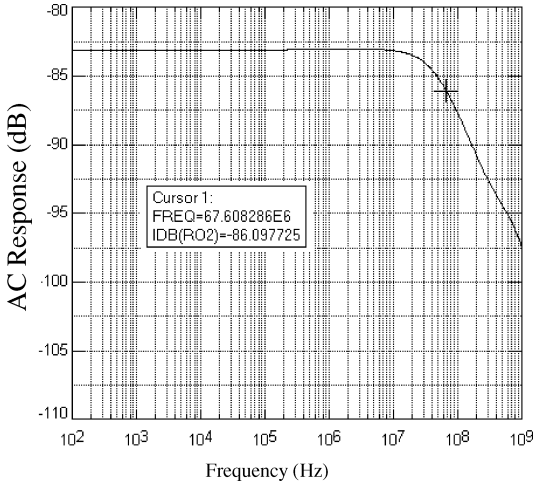

Fig. 12. Frequency response of the proposed transconductor.

tested by applying two tones with different frequencies at the inputs of the transconductor. The tones were chosen at 0.8 and 1 MHz both with 1.5 V amplitude. The spectrum of the output currents shows very small amplitudes at the inter-modulation frequencies and at the harmonics of the two input tones, this is shown in Fig. 11. The largest inter-modulation component was at 0.6 MHz and its amplitude was −39.57 dB relative to the fundamental components. The bandwidth achieved is 67.5 MHz and this is shown in Fig. 12.

5. Conclusion

A new CMOS transconductor with extended linearity range and low distortion was presented in this work. It is suitable for applications requiring wide dynamic range. The idea was based on forcing the common source nodes of the floating current source to track the common mode input voltage. The results achieved show rail-to-rail operation with a small variation in the value of the transconductance, The transconductance of the proposed circuit was plotted with that of the FCS and the performance of both were compared, showing an improved linearity range. The proposed circuit offers −37 dB THD for rail-to-rail input signals and operates under a ±1.5 V supply.

References

1. K. Kimura, "An MOS four-quadrant analog multiplier based on the multitail technique using a quadritail cell as a multiplier core." *IEEE Tans. Circuits Syst. I*, vol. 42, pp. 448–454, 1995.

2. J.A. De Lima and C. Dualibe, "A linearly tunable low-voltage CMOS transconductor with improved common-mode stability and its applications to G_m-C filters." *IEEE Trans. Circuits Syst.-II*, vol. 48, no. 7, pp. 649–660, 2001.
3. E. Seevinck and R.F. Wassenaar, "A versatile CMOS linear transconductor/squaring-law function circuit." *IEEE J. Solid-State Circuits*, vol. 22, pp. 360–377, 1987.
4. A. Nedungadi and T.R. Viswanathan, "Design of linear CMOS transconductance elements." *IEEE Trans. Circuits Syst.*, vol. 31, pp. 891–894, 1984.
5. H. Khorramabadi, "High frequency CMOS continuous time filter." Ph.D. dissertation, Univ. California, Berkeley, 1985.
6. A. Ismail, "Novel low power analog CMOS circuits suitable for baseband section of direct conversion receivers." Master Thesis, Cairo Univ., 2000.
7. A.M. Ismail and A.M. Soliman, "Novel CMOS linearized balanced output transconductor amplifier based on differential pairs." *Frequenz*, vol. 53, pp. 170–174, 1999.
8. A.F. Arbel and L. Goldminz, "Output stage for current-mode feedback amplifiers, theory and applications." *Analog Integrated Circuits and Signal Processing*, vol. 2, pp. 243–255, 1992.
9. M.A. Youssef, "Novel analog CMOS current-mode building blocks for filtering and VGA applications." Master Thesis, Cairo Univ., 2002.
10. M.A. Youssef and A.M. Soliman, "A modified CMOS balanced output transconductor with extended linearity." *Analog Integrated Circuits and Signal Processing*, vol. 36, pp. 239–244, 2003.
11. G. Wilson and P.K. Chan, "Comparison of four CMOS transconductors for fully integrated analogue filter applications." *IEE Proc. G*, vol. 138, no. 6, pp. 683–688, 1991.
12. K. Kuo and A. Leuciuc, "A linear MOS transconductor using source degeneration and adaptive biasing." *IEEE Trans. Circuits Syst. II*, vol. 48, no. 10, pp. 937–943, 2001.