Novel MOS-C Quadrature Oscillator using the Differential Current Voltage Conveyor

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***Abstract*—A new CMOS realization of the Differential Current Voltage Conveyor (DCVC) is introduced. The properties of the DCVC are shown to be suitable for VLSI applications employing MOS transistors operating in ohmic region. A novel electrically tuned MOS-C quadrature oscillator with orthogonal control over the frequency and condition of oscillation is introduced. Additional precise digital trimming can be achieved using the Current Division Network. Compensation techniques for the finite frequency response are presented. Both the experimental results and HSpice simulations are in good agreement with the theoretical analysis.**

I. Introduction

A variety of sinusoidal oscillators using the operational amplifier as the active element are available in the literature. It is well known that the finite gain bandwidth product of the op-amp affects both the condition and the frequency of oscillation [1], [2].

Recently, current-mode analog integrated circuits in CMOS technology have received considerable interest. Current-mode techniques can achieve considerable improvement in amplifier speed, accuracy and bandwidth, overcoming the finite gain-bandwidth product associated with op-amps. Several oscillators have been introduced in the literature using either the Current Conveyor [3]–[5] or the Current Feedback Operational Amplifier(CFOA) [6]–[8] as the active element.

In this paper, the application of the Differential Current Voltage Conveyor (DCVC) in realizing a fully integrated MOS-C quadrature oscillator is introduced. The oscillator circuit presented is fully programmable thus its output can be stabilized against fabrication tolerances and temperature variations. The DCVC is a recently introduced active block [9], [10]. Since the DCVC is not slew limited in the same fashion as op amps, it can provide amplification of high frequency signals with the ease of using standard op amps in addition to a constant bandwidth virtually independent of the gain [10]. The effect of the parasitic capacitances in the proposed circuits is investigated. It is also shown that most of the parasitic capacitances disappear and the remainder can be compensated for, without adding any extra elements.

II. Proposed DCVC CMOS realization

The DCVC is a four terminal analog building block described by the following set of equations:

$$V_{X1} = 0 \quad (1a)$$
$$V_{X2} = 0 \quad (1b)$$
$$I_Z = I_{X1} - I_{X2} \quad (1c)$$
$$V_O = V_Z \quad (1d)$$

The proposed DCVC realization is shown in Fig. 1. The DCVC has similar transmission characteristics to the CFOA, but with two low impedance input terminals, $X1$ and $X2$, a high impedance output terminal, Z, and a low impedance output terminal, O.

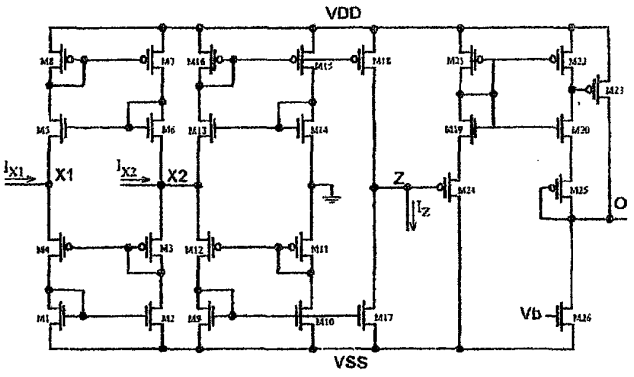

Fig. 1. Proposed CMOS realization of the DCVC.

The DCVC is suitable for non-linearity cancellation since the two input terminals are virtually grounded. A novel voltage mode integrator circuit with all the parasitic capacitances is shown in Fig. 2. Assume the two NMOS transistors M1 and M2 are matched and operating in the ohmic region.

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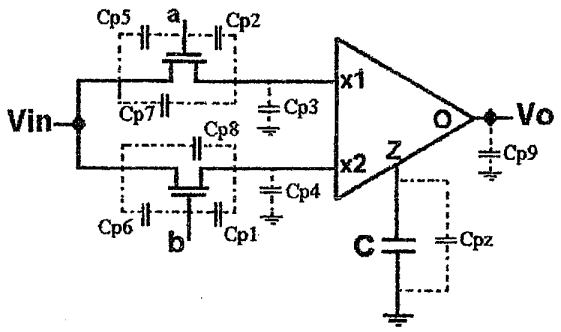

Fig. 2. MOS-C integrator with parasitic capacitances.

The current in the triode region is given by:

$$I = K_n(V_{gs} - V_T)(V_d - V_s) + a_1(V_d^2 - V_s^2) + .. \quad (2)$$

Since the transistors M1 and M2 have equal drain and source voltages, both the even and odd non-linearities are cancelled by subtracting both currents [11], [12] . Neglecting the parasitic capacitances the output voltage, V_o, is given by

$$V_o = V_z = \frac{I_z}{sC} = \frac{I_1 - I_2}{sC} = \frac{GV_{in}}{sC} \quad (3)$$

where $G = \mu_n C_{ox}\frac{W}{L}(V_a - V_b)$.

Positive and negative values of the conductance, G, can be achieved through appropriate choice of the gate control voltages V_a and V_b. Thus both positive and negative integration can be implemented with the same circuit configuration. The input terminals of the DCVC can be used to perform the current differencing operation. The matched transistor pair exhibits self compensation to MOS intrinsic distributed parasitics by the action of the virtual grounded input terminals of the DCVC [12], [13].

Due to the virtual grounded inputs, $X1$ and $X2$, and low impedance output, O, of the DCVC, capacitances C_{p3}, C_{p4} and C_{p9} have little effect. Also, since the voltage sources V_a and V_b are DC sources the effect of the capacitances C_{p1}, C_{p2}, C_{p5} and C_{p6} will be negligible. The capacitances C_{p7} and C_{p8} are drain to source capacitances of two matched NMOS transistors and are connected between equal potential nodes, thus cancel out. Thus response limitations incurred by capacitive time constants are eliminated,due to the low input impedance leading to circuits that are insensitive to stray capacitances [14]. However the DCVC suffers from a parasitic capacitance, C_{pz}, at the Z terminal in a fashion similar to the CFOA.

III. MOS-C QUADRATURE OSCILLATOR

A novel quadrature oscillator is presented in Fig. 3. The quadrature oscillator is based on the cascaded connection of a lossy positive integrator followed by a negative integrator. For ideal operation the characteristic equation is given by:

$$s^2 + \frac{G_3}{C_1}s + \frac{G_1G_2}{C_1C_2} = 0 \quad (4)$$

Thus the circuit represents a minimal component grounded capacitor oscillator with independent control on the condition of oscillation as described by:

$$G_3 = \mu_n C_{ox}\frac{W}{L}(V_{a3} - V_{b3}) = 0 \quad (5)$$

It is seen that the conductance, G_3, controls the condition of oscillation without affecting the radian frequency of oscillation, w_o, which is given by:

$$w_o = \sqrt{\frac{G_1G_2}{C_1C_2}} \quad (6)$$

The passive sensitivities of the proposed oscillator are all low and are given by:

$$S_{G_1}^{w_o} = S_{G_2}^{w_o} = -S_{C_1}^{w_o} = -S_{C_1}^{w_o} = \frac{1}{2} \quad (7)$$

Thus the radian frequency, w_o, can be controlled through adjusting G_1 or G_2 by appropriately choosing the gate voltages V_{a1}, V_{b1}, V_{a2} and V_{b2} without affecting the condition of oscillation which is controlled by V_{a3} and V_{b3}. To ensure the operation of the MOSFETs in the triode region the following conditions apply,

$$V_1 < min[V_{a2} - V_{TB}, V_{b2} - V_{TB}] \quad (8a)$$
$$V_1 < min[V_{a3} - V_{TB}, V_{b3} - V_{TB}] \quad (8b)$$
$$V_2 < min[V_{a1} - V_{TB}, V_{b1} - V_{TB}] \quad (8c)$$

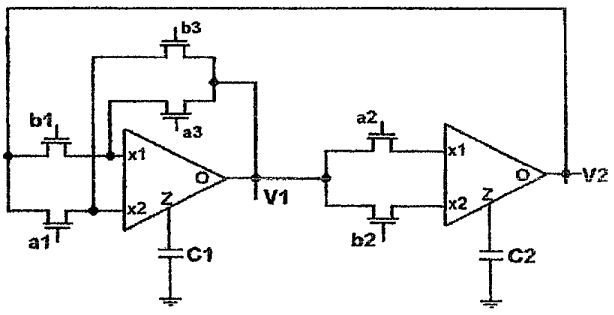

Fig. 3. Novel programmable quadrature oscillator.

For high frequency applications the parasitic capacitance C_{pz} at the , Z, terminal should be considered. Equation (4) reduces to:

$$s^2 + \frac{G_3}{(C_1 + C_{pz})}s + \frac{G_1 G_2}{(C_1 + C_{pz})(C_2 + C_{pz})} = 0 \quad (9)$$

It is clear that the frequency limitations imposed by the parasitic capacitance, C_{pz}, do not increase the system order. Moreover its effect can be reduced if the integrating capacitors, C_1 and C_2, are chosen much larger than C_{pz}. It is also possible to compensate the effect of, C_{pz}, by taking the design value of C_1 and C_2 equal to its theoretical value minus, C_{pz}, achieving self-compensation without using additional elements.

IV. Digitally Controlled MOS-C oscillator

Low supply voltage environments limit the allowable range for analogue tuning voltage, and can result in strong limitations on the maximum achievable signal swing. Thus for low voltage applications digital trimming is preferred. This can be usually achieved by using a weighted capacitor bank or transistor arrays with weighted aspect ratios. However, to provide precise tuning a large number of bits are required and this results in a wide spread in the component values used and an incresed die area.

A digitally controlled version of this oscillator circuit is shown in Fig. 4. This is done by replacing the MOS transistors operating in the triode region with the digitally controlled Current Division Network (CDN) shown in Fig. 5. The CDN provides precise digital trimming without any spread in the transistor aspect ratios, which is important for both area and yield [15], [13].

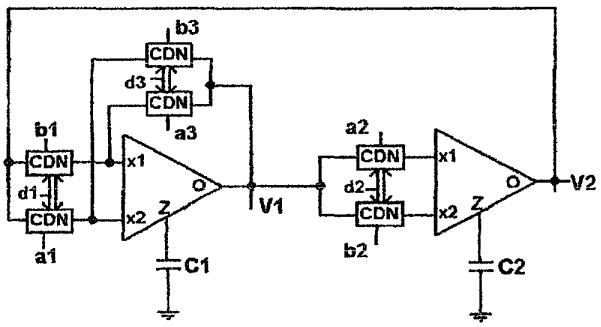

Fig. 4. Digitally Controlled Oscillator.

The condition of oscillation and characteristic equation for this oscillator circuit are given by 5 and 6 where

$$G = \mu_n C_{ox} \frac{W}{2L}(V_a - V_b)\Sigma_{i=1}^{n} 2^{-i} d_i \quad (10)$$

It is clear that in addition to having digital control on the output frequency whose accuracy depends on the number

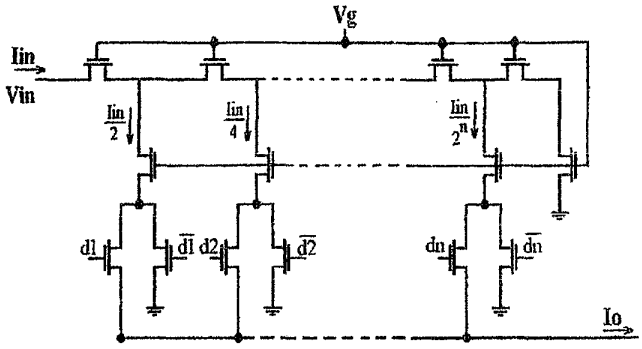

Fig. 5. Current Division Network.

of bits used, we can also achieve very low frequencies of oscillation depending on the digital word applied without using big capacitors which are hard to match and consume a large area.

V. HSpice simulations and experimental results

Fig. 6 shows the HSpice output waveforms of the oscillator circuit in Fig. 3, where $C_1 = C_2 = 100$pF and $G_1 = G_2 = 142.2\mu$A/V. From simulations $f_o = 222.6$ kHz and THD=1.6%.

To verify the proposed circuits, the DCVC was built using the transistor array IC CD4700. Fig. 7 shows the oscilloscope output waveforms of the oscillator circuit shown in Fig. 3, where $C_1 = C_2 = 100$pF and $G_1 = G_2 = 1$mA/V. Fig. 8 illustrates V_{C_1} versus V_{C_2} showing a simple limit cycle of period one, indicating a single harmonic frequency.

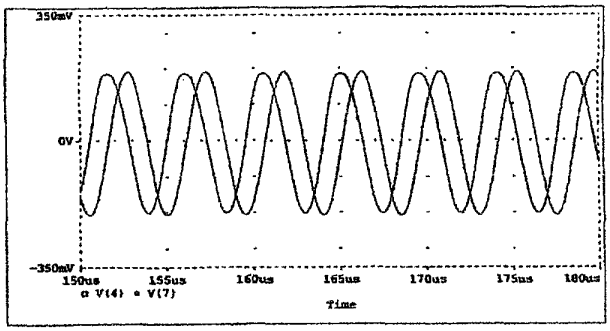

Fig. 6. HSpice output waveforms of the quadrature oscillator.

VI. Conclusions

New parasitic-capacitance-insensitive quadrature oscillator using the differential current voltage conveyor have been presented. Since the DCVC has virtually grounded

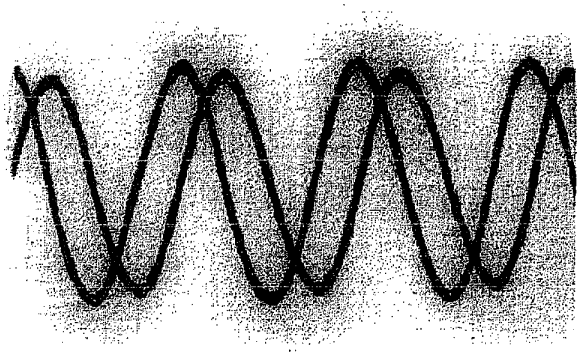

Fig. 7. Oscilloscope Quadrature Outputs for $C_1 = C_2 = 100\text{pF}$ and $G_1 = G_2 = 1\text{mA/V}$

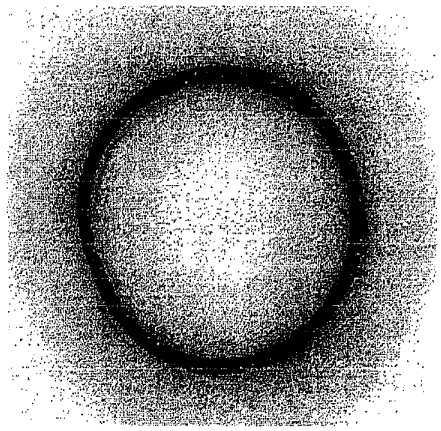

Fig. 8. V_{C_1} versus V_{C_2}.

inputs and low impedance output, most effects of the parasitic capacitances disappear and the remainder can be easily compensated without adding any extra elements. The DCVC's main advantage is the ability to implement different analog circuits without the need of resistors as it can be used to cancel both the odd and even non-linearity terms associated with MOS transistors operating in the triode region. The proposed oscillator has the advantage of programmability that is essential for process and temperature variations. Unlike other oscillator circuits [1-8], it does not use passive resistors that consume large area. More programmability is achieved through digital control using CDN.

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