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A Modified CMOS Balanced Output Transconductor with Extended Linearity

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Abstract. A new CMOS balanced output transconductor is presented. The circuit is based on applying the dynamic biasing technique on the floating current source to extend its linearity range. The difference in the biasing currents is compensated to maintain the two output currents balanced by subtracting it at the output nodes. The proposed transconductor is suitable for high frequency applications requiring a wide dynamic range. Rail-to-rail operation is achieved with THD of −33.64 dB. The bandwidth achieved by the transconductor is 240 MHz, and the supply voltage used is ±1.5 V.

Key Words: transconductor, voltage-to-current transformation, linearization, floating current source, rail-to-rail, dynamic biasing technique

1. Introduction

Linear transconductors or voltage-to-current converter circuits are useful building blocks in analog signal processing systems. They are used in continuous time filters, data converters, variable gain amplifiers, multipliers, and interface circuits [1].

G_m-C filters recently received great interest since they are suitable for integration and can operate at high frequencies [2]. Although on-chip active filters consume power, chip area, and limit the overall dynamic range, they enable high integration and bandwidth tuning [1]. Therefore the design of highly linear and tunable transconductors becomes mandatory. As device sizes and supply voltages are scaled down to achieve higher operating frequencies, obtaining high linearity with reasonable signal levels becomes more challenging.

Several circuit techniques have been proposed in the literature to improve the linearity of MOS transistors. The linearization methods include: cross coupling of multiple differential pairs [1, 3, 4], adaptive biasing [3, 5], source degeneration (using resistors or MOS transistors) [6], and shift level biasing [7].

The realizations based on the long tail differential pair (LTP) have received a great interest [8] since they offer a relatively low level of distortion due to the second order effects such as the body-effect and mobility degradation, however the tunablity is limited.

2. Circuit Topology for the Extended Linearity Transconductor

The floating current source (FCS) shown in Fig. 1 [9] provides two balanced output currents, this is always valid to satisfy Kirchoff's current law.

$$\begin{aligned} I_T &= I_T + I_{o1} + I_{o2} \\ \therefore \quad I_{o1} &= -I_{o2} \end{aligned} \tag{1}$$

This circuit can be viewed as two long tail differential pairs connected in parallel, an NMOS pair and a PMOS pair. For the NMOS differential pair assuming that M_1 and M_2 are matched and operate in the saturation region, it can be shown that:

$$I_1 - I_2 = v_d\sqrt{K_n}\sqrt{I_T - \frac{K_n v_d^2}{4}} \tag{2}$$

where I_T is the tail current of the differential pair, and

$$v_d = V_1 - V_2 \tag{3}$$

$$K_n = \mu_n C_{OX}\frac{W_1}{L_1} \tag{4}$$

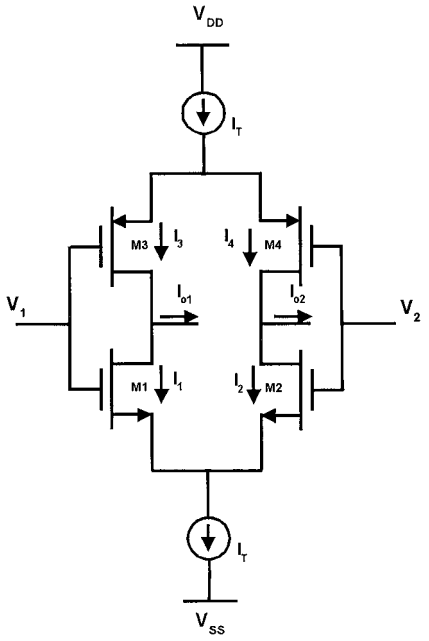

Fig. 1. Floating current source [9].

Similarly for the PMOS differential pair, assuming that M_3 and M_4 are matched and operate in the saturation region then:

$$I_3 - I_4 = -v_d\sqrt{K_p}\sqrt{I_T - \frac{K_p v_d^2}{4}} \tag{5}$$

where,

$$K_p = \mu_p C_{OX}\frac{W_3}{L_3} \tag{6}$$

The two output currents can be obtained as:

$$\begin{aligned} I_{o1} &= I_3 - I_1 \\ I_{o2} &= I_4 - I_2 \end{aligned} \tag{7}$$

$$\therefore \quad 2I_{o1} = (I_3 - I_4) - (I_1 - I_2) \tag{8}$$

$$I_{o1} = -I_{o2} = -\frac{1}{2}v_d\left(\sqrt{K_n}\sqrt{I_T - \frac{K_n v_d^2}{4}} + \sqrt{K_p}\sqrt{I_T - \frac{K_p v_d^2}{4}}\right) \tag{9}$$

Equation (9) reveals the presence of two nonlinear terms, this limits the linear range of operation of the FCS. The effect of the nonlinear terms is demonstrated by the simulation results shown in Fig. 5. In this work, it is required to cancel both nonlinear terms to extend the linear range of operation of the transconductor.

The adaptive biasing technique, which was first proposed in [10], was used in [3] to cancel the nonlinear term and extend the operating region of the LTP transconductor, by choosing the tail current according to the following equation:

$$I_T = I_B + \frac{K v_d^2}{4} \tag{10}$$

It is evident from Eq. (9) that both transconductors of the FCS can't be linearized using the same tail current. To linearize the NMOS differential pair the NMOS tail current I_{TN} should be:

$$I_{TN} = I_B + \frac{K_n v_d^2}{4} \tag{11}$$

While to linearize the PMOS differential pair the PMOS tail current I_{TP} should be:

$$I_{TP} = I_B + \frac{K_p v_d^2}{4} \tag{12}$$

Since the two biasing current sources are unequal then the output currents of the transconductor will not be balanced. A current I_c should be subtracted from the output nodes to balance the output currents again, as shown in Fig. 2, thus compensating the effect of unequal tail

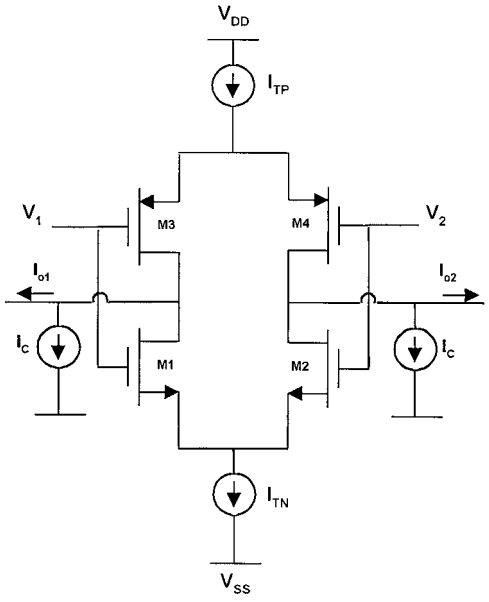

Fig. 2. The proposed extended linearity balanced output transconductor.

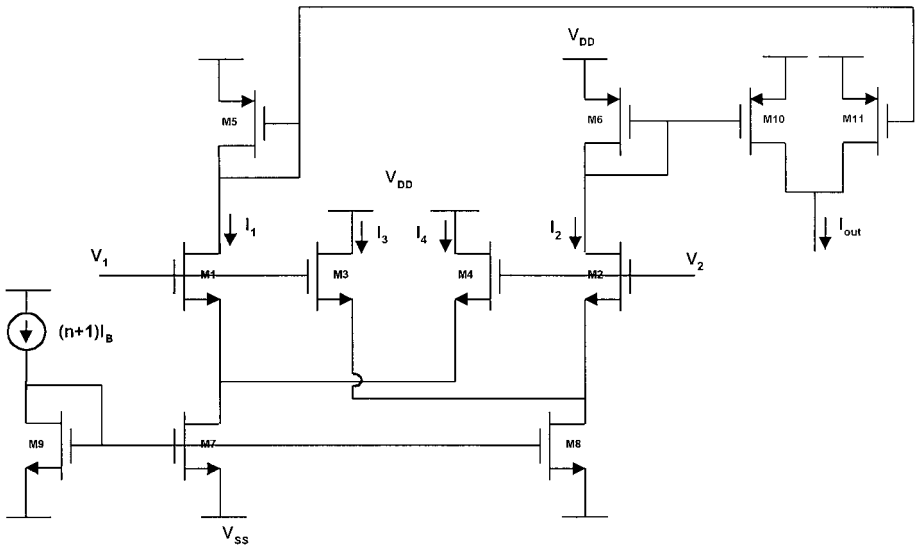

Fig. 3. Squaring circuit used to generate the biasing current I_{TN} for the NMOS differential pair.

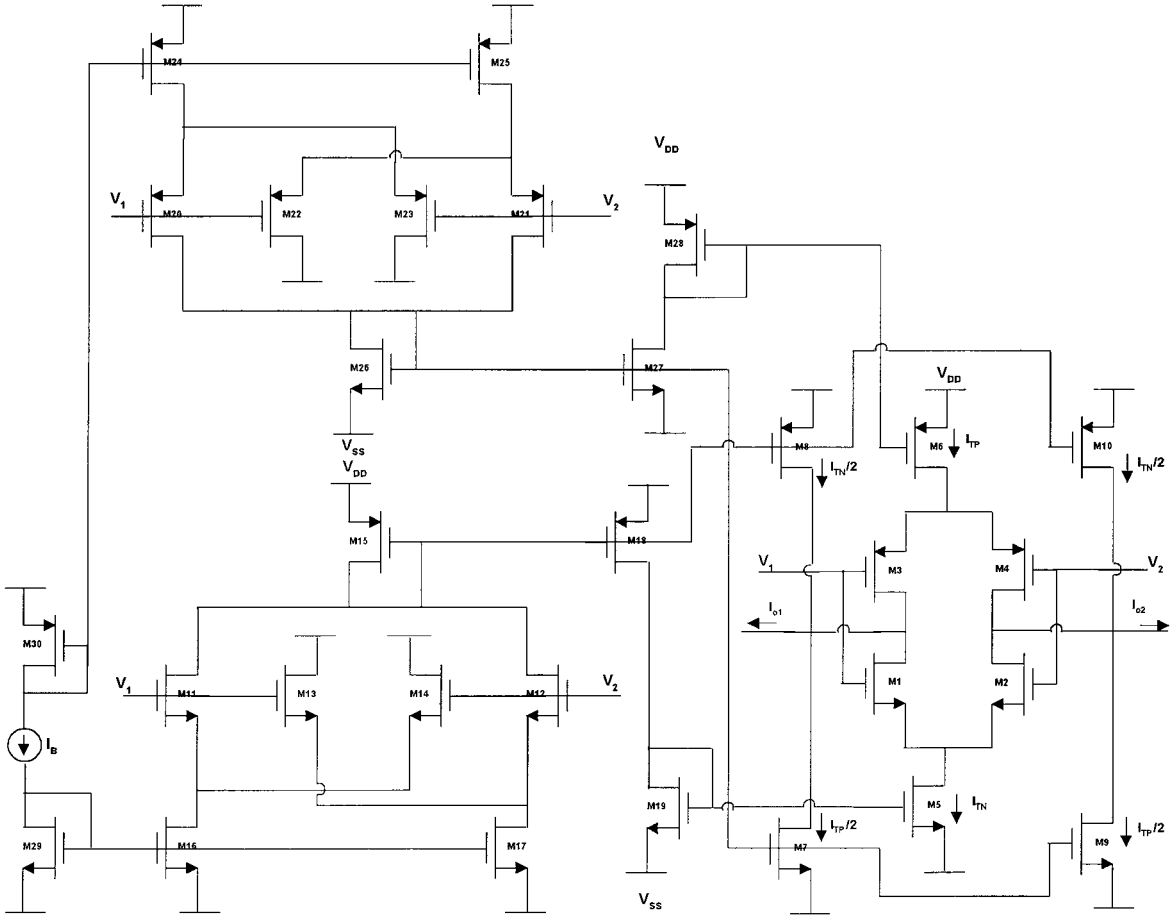

Fig. 4. Circuit diagram of the extended linearity transconductor based on the dynamic biasing technique.

currents. In this case the output currents can be expressed as:

$$I_{o1} = I_3 - I_1 - I_c$$
$$I_{o2} = I_4 - I_2 - I_c \quad (13)$$

$$\therefore \quad I_{o1} - I_{o2} = (I_3 - I_4) - (I_1 - I_2) \quad (14)$$

It can be proved that the output differential current is given by:

$$I_{o1} - I_{o2} = -v_d(\sqrt{K_n} + \sqrt{K_p})\sqrt{I_B} \quad (15)$$

Equation (15) shows that the proposed linearized transconductor has a very wide range of operation. There should be no common mode output current for balanced operation, therefore:

$$I_{o1} + I_{o2} = I_{TP} - I_{TN} - 2I_c = 0 \quad (16)$$

The value of the current source I_c should be chosen as:

$$I_c = \frac{I_{TP} - I_{TN}}{2} \quad (17)$$

The value of the transconductance G_m is:

$$G_m = 2(\sqrt{K_n} + \sqrt{K_p})\sqrt{I_B} \quad (18)$$

The two tail currents I_{TN} and I_{TP} given by Eqs. (11) and (12) can be obtained using any squaring circuit. In this work the squaring circuits used are based on cross coupling differential pairs [3]. Although using squaring circuits based on cross-coupling differential pairs doesn't provide a low power solution, but it is intended to demonstrate the applicability of the linearization technique on the FCS. They can then be replaced by any other low power squaring circuits [5]. Figure 3 shows the squaring circuit used to obtain the NMOS differential pair tail current, I_{TN}. The circuit used to obtain the PMOS differential pair tail current, I_{TP}, can be similarly obtained. The overall circuit diagram of the extended linearity CMOS balanced output transconductor is shown in Fig. 4. Transistors M_1–M_6 are the main FCS, M_7–M_{10} are the current mirrors generating the compensation current I_c, M_{11}–M_{17} perform the squaring function to obtain I_{TN}, and M_{20}–M_{26} perform the squaring function to obtain I_{TP}.

3. Simulation Results

To compare the performance of both the FCS and the proposed extended linearity balanced output transconductor, numerous computer simulations have been carried out using level 8 Spice parameters for a 0.5 μm CMOS process, with the supply voltages ± 1.5 V. To obtain a fair and accurate comparison, the circuits presented in Section 2 have been optimized to achieve the best linearity possible for a given transconductance value. The following results were obtained while one

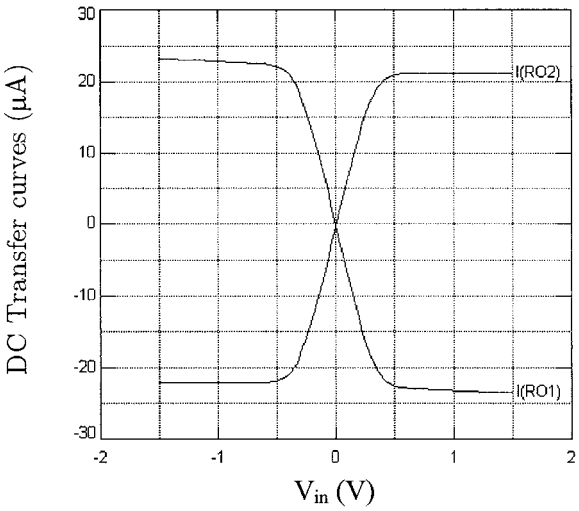

Fig. 5. Output currents of the FCS.

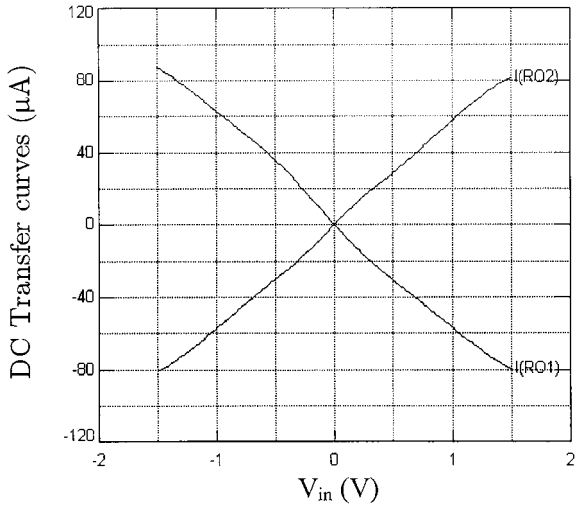

Fig. 6. Output currents of the proposed extended linearity transconductor.

of the inputs was grounded and the other was varied across the supply range. The two balanced output currents of the FCS are shown in Fig. 5, while those of the new extended linearity balanced output transconductor

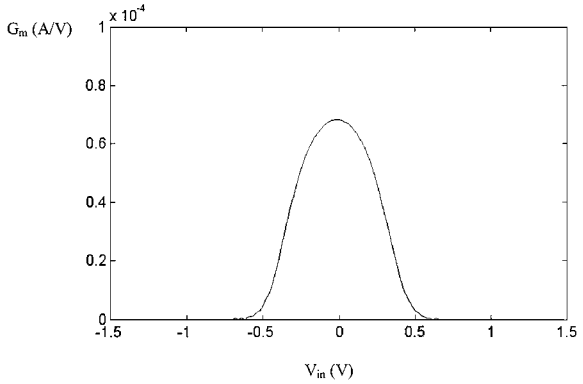

Fig. 7. Transconductance of the FCS.

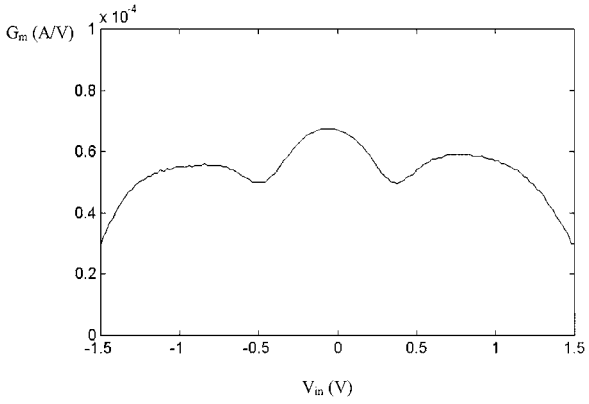

Fig. 8. Transconductance of the proposed extended linearity transconductor.

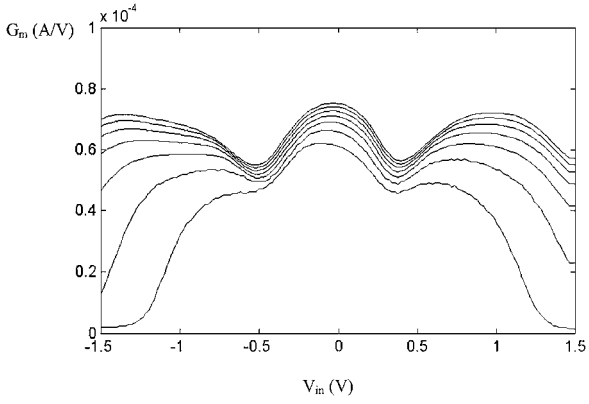

Fig. 9. Effect of varying the bias current I_B on the value of the transconductance.

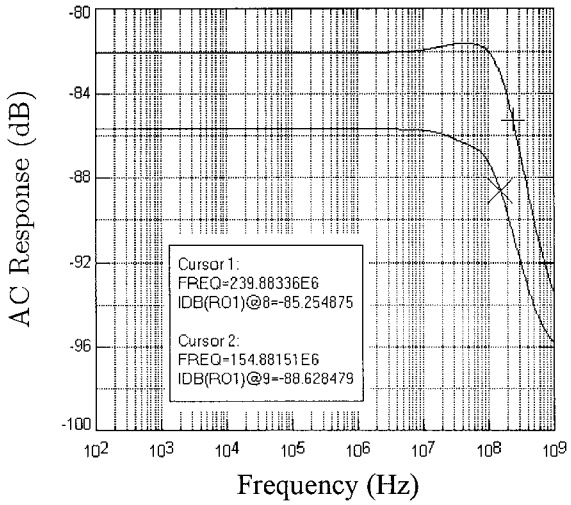

Fig. 10. Frequency response of the transconductor for different values of I_B.

are shown in Fig. 6. It is evident that the range of operation of the proposed circuit extends from rail-to-rail, while that of the FCS is limited to ± 0.5 V. This can be clearly demonstrated if the value of the transconductance is plotted as shown in Figs. 7 and 8. The range of operation obtained in this work exceeds the range achieved by combining two different linearization techniques in [11]. Varying the value of the biasing current I_B affects the value of the transconductance, and also the variations in the transconductance [12], this is shown in Fig. 9 where I_B was changed from 50 μA to 400 μA. As the value of I_B increases the variations decrease, on the other hand the power consumption increases. The achieved THD of the output currents was -33.64 dB for an input sinusoid with

Table 1. Aspect ratios of the transistors in Fig. 4.

Transistor	Aspect ratio μm/μm	Transistor	Aspect ratio μm/μm
M_1, M_2	5/2	M_{13}, M_{14}	40/4.5
M_3, M_4	15/2	M_{15}, M_{18}	120/3
M_5, M_{19}	10/2	M_{16}, M_{17}, M_{29}	20/2
M_6, M_{28}	30/2	M_{20}, M_{21}	24/4.5
M_7, M_9	20/3	M_{22}, M_{23}	120/3
M_8, M_{10}	60/3	M_{24}, M_{25}, M_{30}	60/2
M_{11}, M_{12}	8/4.5	M_{26}, M_{27}	40/3
M_7, M_9	20/3		

1.5 V peak value and 1 MHz frequency. The bandwidth of the transconductor varies between 155 and 240 MHz according to the value of I_B, this is shown in Fig. 10. The aspect ratios of the transistors used to design the extended linearity transconductor, Fig. 4, are given in Table 1.

4. Conclusion

This paper presented a new CMOS rail-to-rail balanced output transconductor, based on the dynamic biasing of the FCS to cancel the nonlinear terms and extend the dynamic range. The proposed transconductor is suitable for high frequency applications requiring a wide dynamic range. The results achieved show rail-to-rail operation with small variations in the value of the transconductance. The THD achieved was −33.64 dB for rail-to-rail input signals.

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