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MOS-C TOW-THOMAS FILTER USING VOLTAGE OP AMP, CURRENT FEEDBACK OP AMP AND OPERATIONAL TRANSRESISTANCE AMPLIFIER

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Several MOS-C realizations of the Tow-Thomas circuit using the commercially available voltage operational amplifier and the current feedback operational amplifier are reviewed in this paper. Additional MOS-C Tow-Thomas realizations using the operational transresistance amplifier and the differential current voltage conveyor are also included. MOS-C realizations of the Tow-Thomas circuit using CMOS operational amplifier, CMOS current feedback operational amplifier and CMOS operational transresistance amplifier are also given. Spice simulation results using 0.18 CMOS technology model from MOSIS are included together with detailed comparison tables to demonstrate the differences between MOS-C Tow-Thomas circuits using both of the commercially available active building blocks and CMOS integrated building blocks.

Keywords: Tow-Thomas Filter; CFOA; OTRA; DCVC.

1. Introduction

The history of Tow-Thomas (TT)[1,2] second order filter using operational amplifiers (op-amps) has been reviewed in Ref. 3. Passive and active compensation methods to improve the circuit performance for high Q designs were also reviewed. It is well known that the classical TT circuit using op-amps has frequency limitations due to the finite gain-bandwidth of the op-amps.

In this paper, the progress in the realization of the MOS-C TT circuit using the commercially available voltage operational amplifier (VOA),[4–7] the current feedback operational amplifier (CFOA),[8–11] operational transresistance amplifiers (OTRA),[12–17] the differential current voltage conveyor (DCVC)[18,19] is reviewed. The OTRA and the DCVC are realized using two CFOA. MOS-C realizations of the

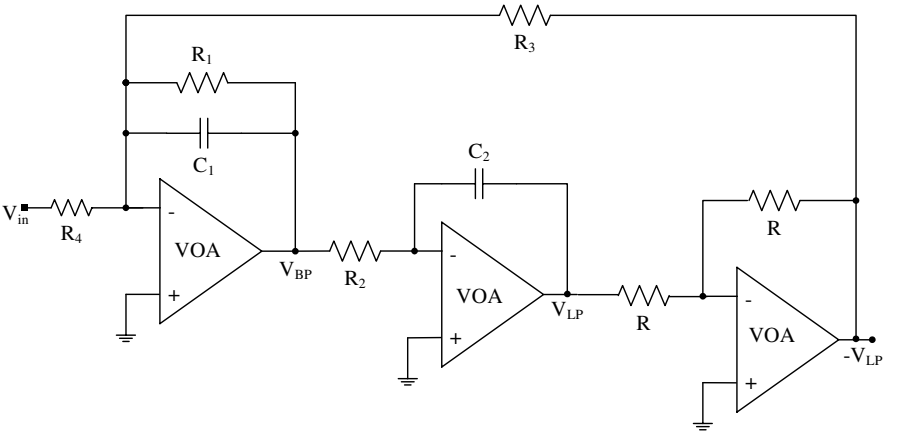

Fig. 1. Tow-Thomas filter using VOA and RC.[1,2]

TT circuit using CMOS operational amplifier, CMOS current feedback operational amplifier and CMOS operational transresistance amplifier are also given. Spice simulation results using 0.18 CMOS technology model from MOSIS are included and detailed comparison tables summarizing the differences between MOS-C TT circuits are included.

2. The Tow-Thomas Circuit Using Op-Amps

The Tow-Thomas (TT) active RC circuit using three op-amps is shown in Fig. 1.[1–3] The transfer functions are given by:

$$\frac{V_{BP}}{V_{in}} = \frac{-\dfrac{s}{C_1 R_4}}{s^2 + \dfrac{s}{C_1 R_1} + \dfrac{1}{C_1 C_2 R_2 R_3}}, \tag{1}$$

$$\frac{V_{LP}}{V_{in}} = \frac{\dfrac{1}{C_1 C_2 R_2 R_4}}{s^2 + \dfrac{s}{C_1 R_1} + \dfrac{1}{C_1 C_2 R_2 R_3}}. \tag{2}$$

Although the TT circuit has very low passive sensitivities to all passive circuit components, it suffers from a rather drastic Q-factor enhancement effect due to the op-amp finite gain bandwidth.

Recently the non-idealities of the classical TT active RC circuit using VOA and CFOA-based Miller integrator has been reported in Ref. 20.

3. The MOS Transistor Nonlinearities and Cancellation Methods

An NMOS transistor is shown in Fig. 2(a), with its gate connected to a control voltage V_G. The terminal voltages V_1 and V_2 are assumed to remain below V_G by

at least the threshold voltage of the transistor V_T to allow operation in the non-saturation region. The current in the non-saturation region is given by Refs. 4–6.

$$I = K(V_G - V_T)(V_1 - V_2) + a_1(V_1^2 - V_2^2) + a_2(V_1^3 - V_2^3) + \cdots . \tag{3}$$

K is the transconductance parameter of the NMOS transistor and is given by:

$$K = \mu_n C_{OX} \left(\frac{W}{L}\right) , \tag{4}$$

where (W/L) is the transistor aspect ratio, C_{OX} is the gate oxide capacitance per unit area and μ_n is the electron mobility.

Many different techniques have been proposed for eliminating the effect of the nonlinearities.[4–6] Some cancel the even nonlinearities in the current of one MOS transistor; others cancel the nonlinearities in the difference of the currents in two or four MOS transistors. The various technique used in this paper to realize MOS-C TT filters are summarized in Figs. 2(b)–2(d).

It is easily verified from the drain current of the MOS transistor in the non-saturation region given above, that the even nonlinearities are eliminated for the MOS transistor with its drain and source voltages out of phase[6] as shown in Fig. 2(b), and the current in this case is approximately given by:

$$I = 2K(V_G - V_T)V_1 \quad \text{for } V_G - V_T \geq |V_1| . \tag{5}$$

The circuit shown in Fig. 2(c) accomplishes in principle complete cancellation of both the even and odd nonlinearities in the difference between the currents of M_1 and M_2. Since the transistors M_1 and M_2 have equal drain and source voltages, therefore the difference between two currents is given by:

$$I = I_1 - I_2 = KV_G(V_1 - V_2) \quad \text{for } V_G - V_T \geq \max(V_1, V_2) . \tag{6}$$

The circuit shown in Fig. 2(d)[4,5] also performs a complete cancellation of the nonlinearities and the linearized current is given by:

$$I = (I_1 + I_3) - (I_2 + I_4) = KV_G\,(V_1 - V_2) \quad \text{for } V_G - V_T \geq \max(V, V_1, V_2) . \tag{7}$$

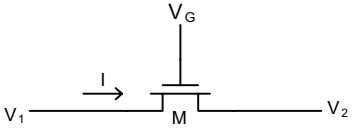

Fig. 2(a). Symbol of NMOS transistor.

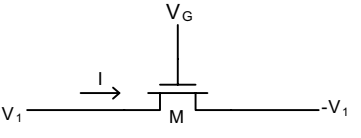

Fig. 2(b). NMOS transistor with even nonlinearity cancellation.

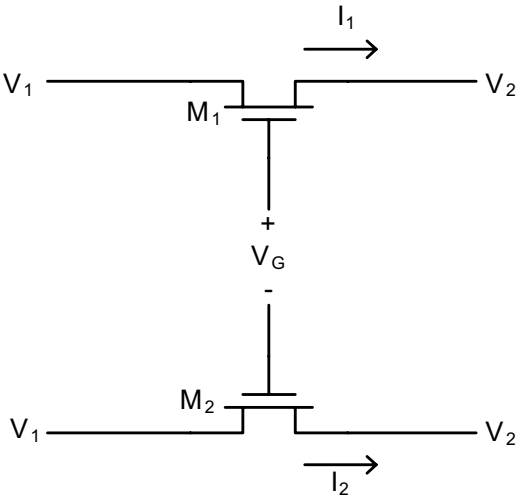

Fig. 2(c). Two MOS transistors circuit with full nonlinearities' cancellation.

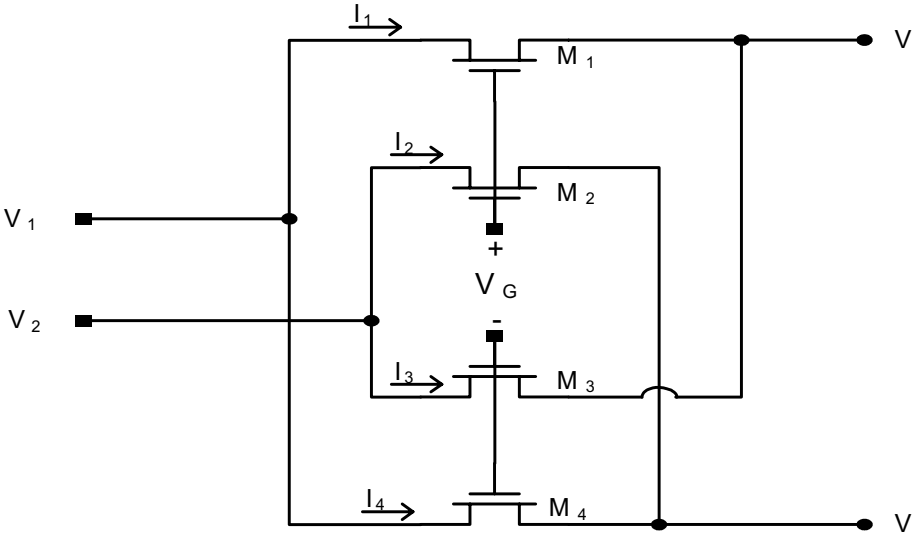

Fig. 2(d). Four MOS transistors circuit with full nonlinearities' cancellation.[4–6]

In the following sections the MOS-C TT circuits using the VOA, CFOA, OTRA and DCVC are considered together with detailed simulation and comparison tables. The OTRA and the DCVC are realized using the commercially available CFOA AD844-available from Analog Devices.[21]

4. MOS-C TT Circuit Using VOA

The first MOS-C TT circuit using VOA was introduced in Ref. 5 and is shown in Fig. 3(a). The circuit equations are given by:

$$\frac{V_{BP}}{V_{in}} = \frac{-\dfrac{KV_{G4}}{C_1}s}{s^2 + \left(\dfrac{KV_{G1}}{C_1}\right)s + \left(\dfrac{K^2V_{G2}V_{G3}}{C_1C_2}\right)}, \tag{8}$$

$$\frac{V_{LP}}{V_{in}} = \frac{-\dfrac{K^2V_{G2}V_{G4}}{C_1C_2}}{s^2 + \left(\dfrac{KV_{G1}}{C_1}\right)s + \left(\dfrac{K^2V_{G2}V_{G3}}{C_1C_2}\right)}, \tag{9}$$

$$\omega_0 = K\sqrt{\frac{V_{G2}.V_{G3}}{C_1C_2}}, \quad Q = \frac{1}{V_{G1}}\sqrt{\frac{C_1}{C_2}V_{G2}V_{G3}}\,. \tag{10}$$

It is seen that the filter Q can be independently controlled by V_{G1}.

The same circuit with programmable ω_0 and Q was studied in Ref. 7.

The PSpice simulations have been carried out using 0.18 CMOS technology model from MOSIS to realize a bandpass response with $f_0 = 1\,\text{MHz}$ and $Q = 10$.

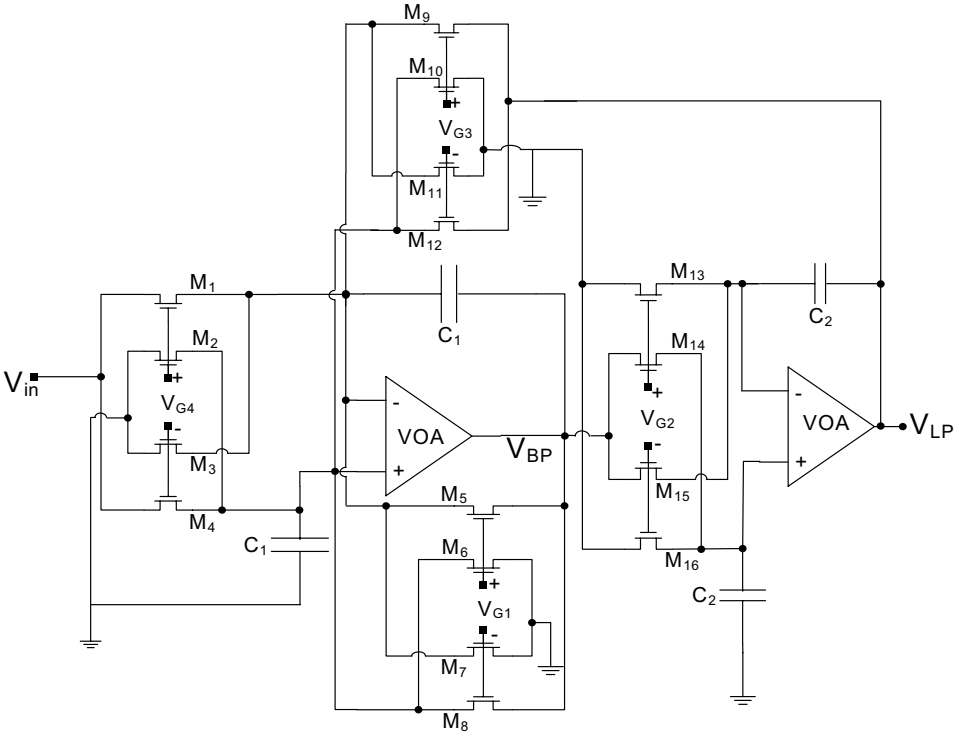

Fig. 3(a). TT filter using VOA MOS-C.[5]

The design values of the circuit parameters are $C_1 = C_2 = 55\,\text{pF}$. The transistor aspect ratios $(W/L) = (2\,\mu\text{m}/4\,\mu\text{m})$, $K' = 251.497\,\mu\text{A/V}^2$, and the gate voltages have been taken as $V_{G2} = V_{G3} = V_{G4} = 2.748\,\text{V}$ and $V_{G1} = 0.2748\,\text{V}$. For the VOA the exact model of LM 741 is used with supply voltages of $\pm 12\,\text{V}$.

Figures 3(b) and 3(c) show the magnitude and phase responses of the simulated and the ideal responses respectively from simulation; the TT using op-amp does not satisfy the requirements of the required filter.

Figure 3(d) shows the input/output referred noise.

5. MOS-C TT Circuit Using CFOA

Recently, great interest has been devoted to the analysis and design of current-feedback operational amplifier circuits,[21–25] mainly because these circuits exhibit performance, particularly higher speed and better bandwidth, than classic voltage-mode operational amplifiers, which are limited by a constant gain-bandwidth product.

The current-feedback operational amplifier (CFOA) is a four-port network with a describing matrix of the form:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_O \end{bmatrix}. \tag{11}$$

Several CMOS realizations for the CFOA have been reported in the literature.[26–31]

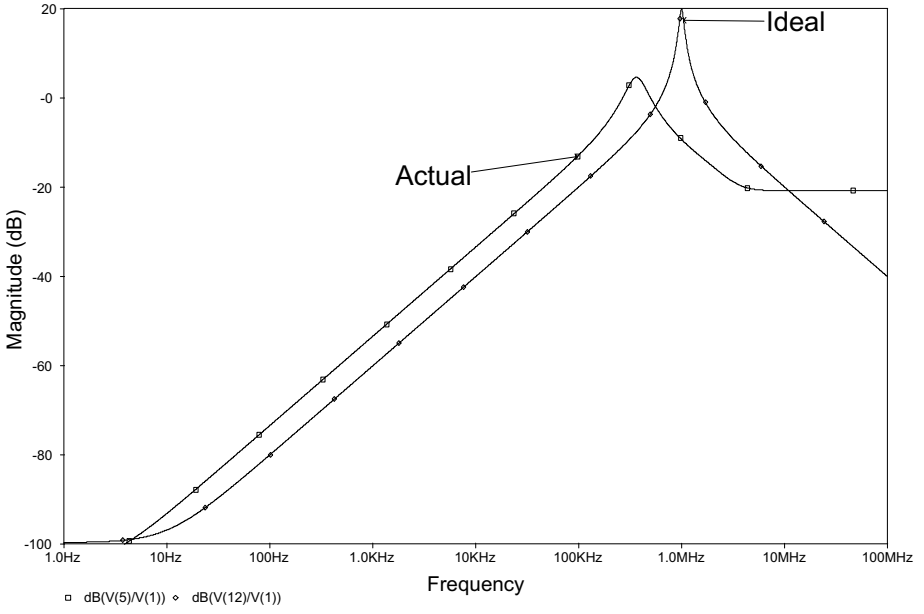

Fig. 3(b). Magnitude responses of TT using LM741 as VOA and MOS-C.

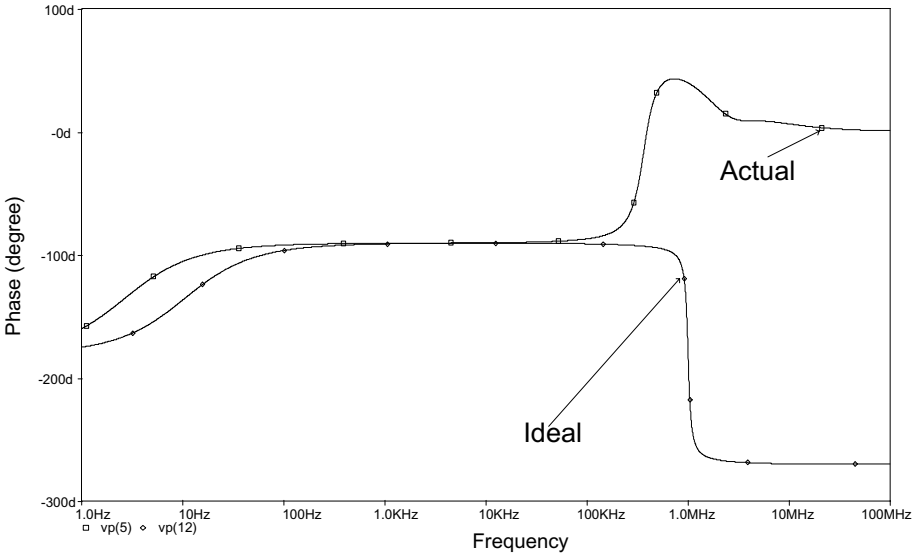

Fig. 3(c). Phase responses of TT using LM741 as VOA and MOS-C.

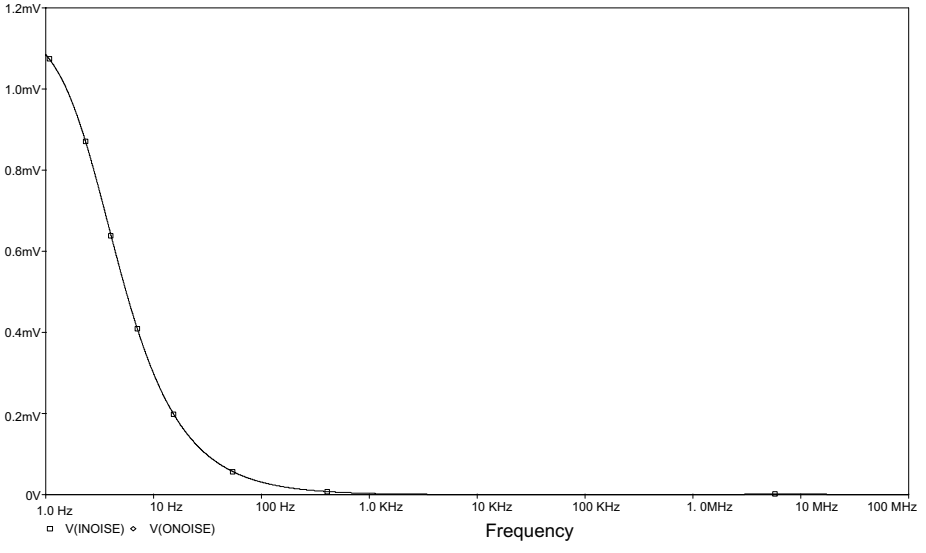

Fig. 3(d). Input/output referred noise of the TT using LM741 and MOS-C.

5.1. *MOS-C TT circuit using CFOA as a three-terminal device*

In this section the CFOA is used as a three-port network leaving the Z port open circuit.

In this case the MOS-C TT circuit shown in Fig. 4(a) is similar to the VOA circuit and the circuit equations are the same as given by Eqs. (8)–(10).

The PSpice simulations have been carried out for the circuit of Fig. 4(a) using the same design values as in the previous section. For the CFOA, the exact model of AD-844 is used with supply voltages of ±5 V.

Figures 4(b) and 4(c) show the magnitude and phase responses of the simulated and the ideal responses respectively. From the simulations of the TT using the

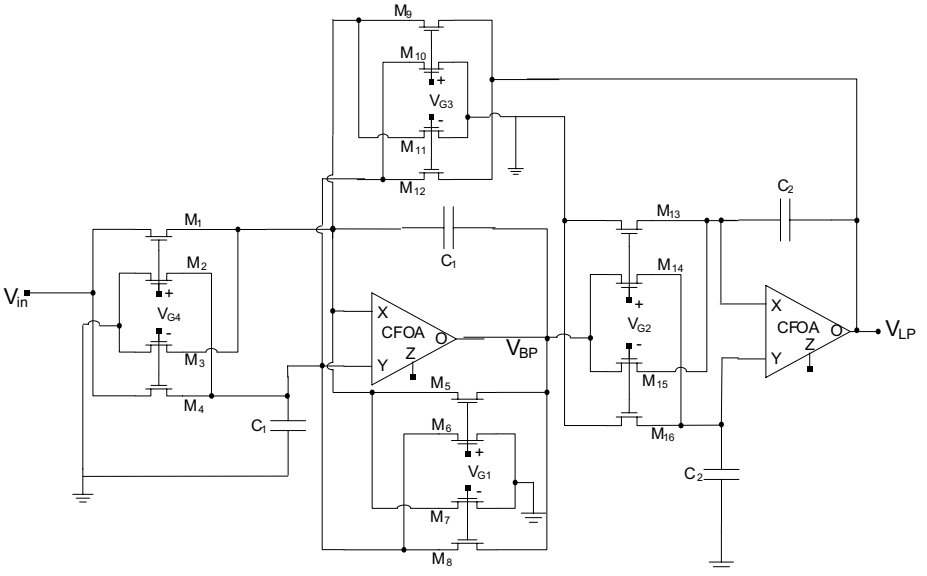

Fig. 4(a). TT filter using CFOA (AD844) as a three-terminal, and MOS-C.

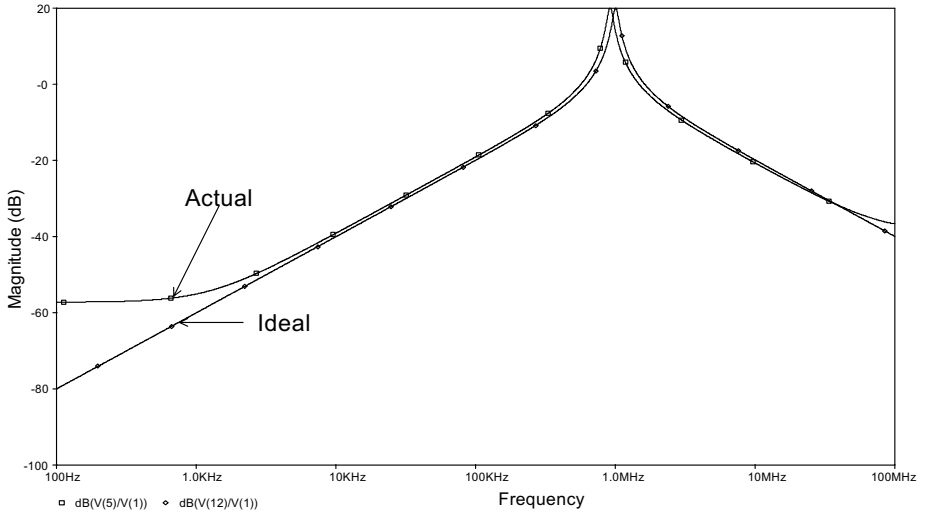

Fig. 4(b). Magnitude responses of TT using AD844 as a VOA and MOS-C.

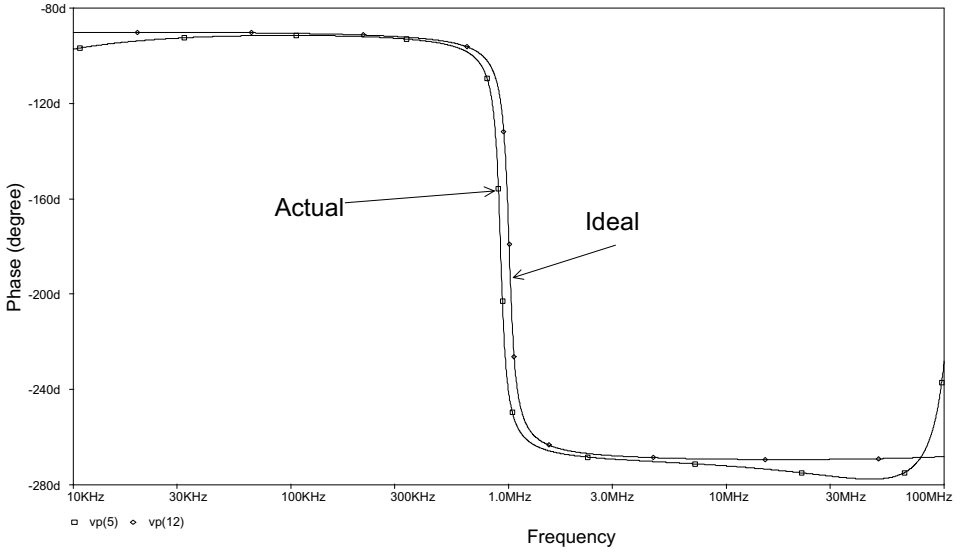

Fig. 4(c). Phase response of the band-pass TT using AD844 as a VOA and MOS-C.

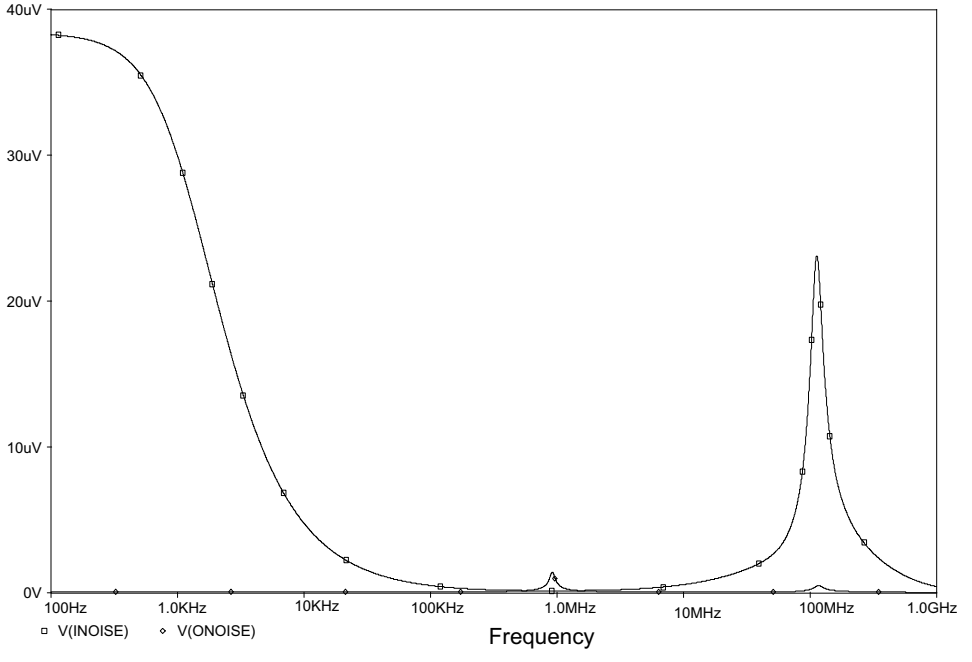

Fig. 4(d). Input/output referred noise of the TT using AD844 and MOS-C.

CFOA as a three-terminal device, it is seen that the requirements of the required filter are nearly satisfied.

Figure 4(d) shows the input/output referred noise.

5.2. *MOS-C TT circuit using CFOA as four-terminal device*

In this section the CFOA is used as a four-port network utilizing the Z port.

In this case the MOS-C TT circuit shown in Fig. 5(a) and it uses six grounded capacitors and four MOS resistor circuits.[9] The circuit equations are given by:

$$\frac{V_{BP}}{V_{\text{in}}} = \frac{-\dfrac{KV_{G4}}{C_1}s}{s^2 + \left(\dfrac{KV_{G1}}{C_1}\right)s + \left(\dfrac{K^2V_{G2}V_{G3}}{C_1C_2}\right)}, \tag{12}$$

$$\frac{V_{LP}}{V_{\text{in}}} = \frac{\dfrac{K^2V_{G2}V_{G4}}{C_1C_2}}{s^2 + \left(\dfrac{KV_{G1}}{C_1}\right)s + \left(\dfrac{K^2V_{G2}V_{G3}}{C_1C_2}\right)}, \tag{13}$$

$$\omega_0 = K\sqrt{\frac{V_{G2}.V_{G3}}{C_1C_2}}, \quad Q = \frac{1}{V_{G1}}\sqrt{\frac{C_1}{C_2}V_{G2}V_{G3}}\,. \tag{14}$$

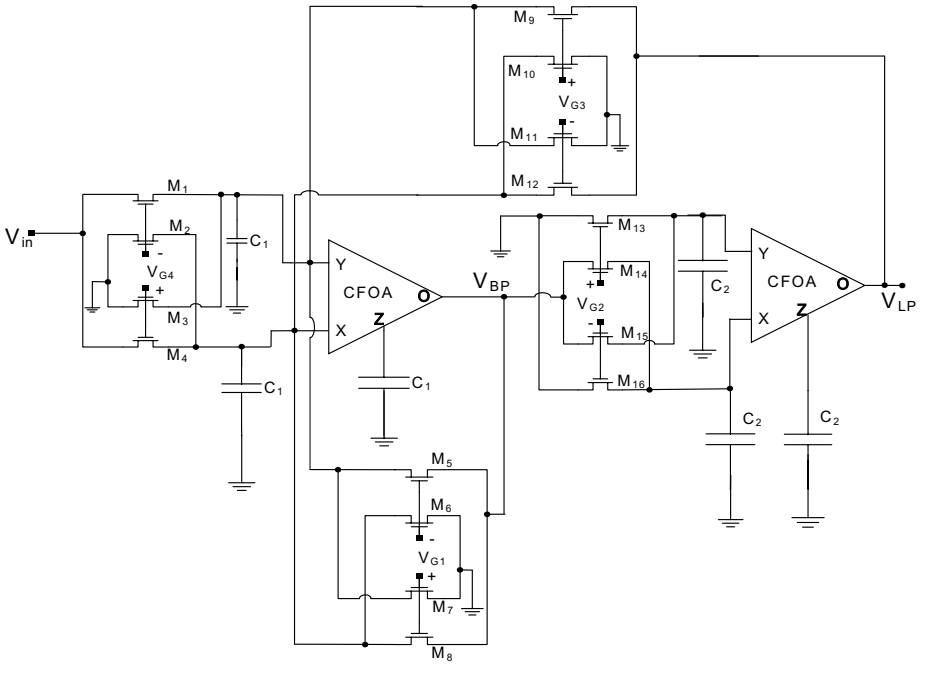

Fig. 5(a). TT filter using CFOA and MOS-C.[9]

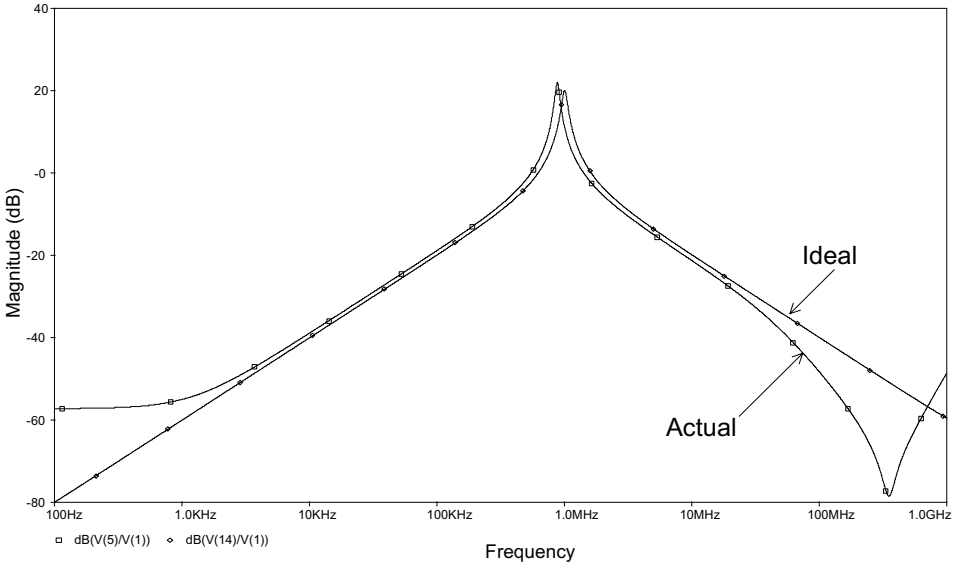

Fig. 5(b). Magnitude responses of TT using AD844 and MOS-C.

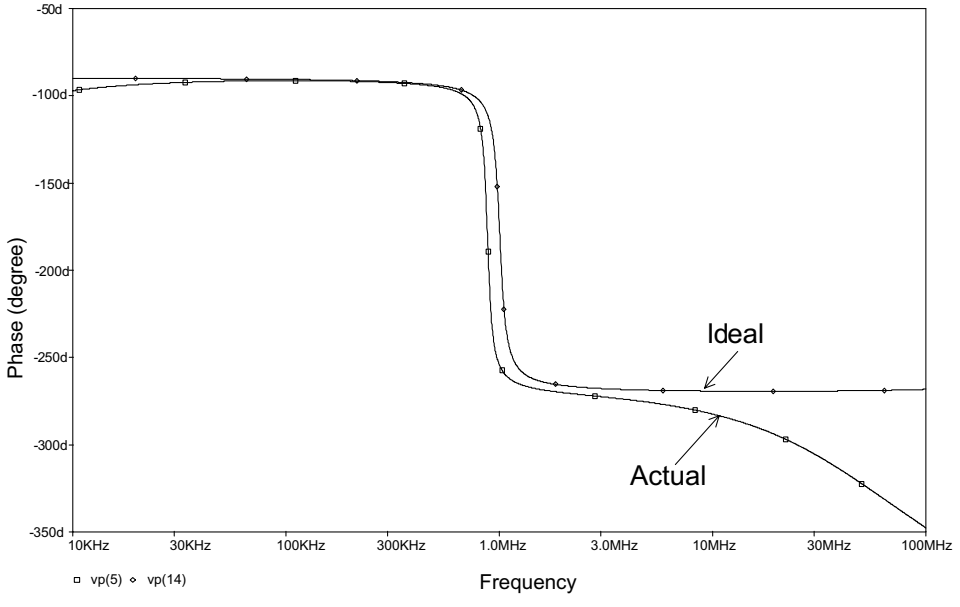

Fig. 5(c). Phase responses of TT using AD844 and MOS-C.

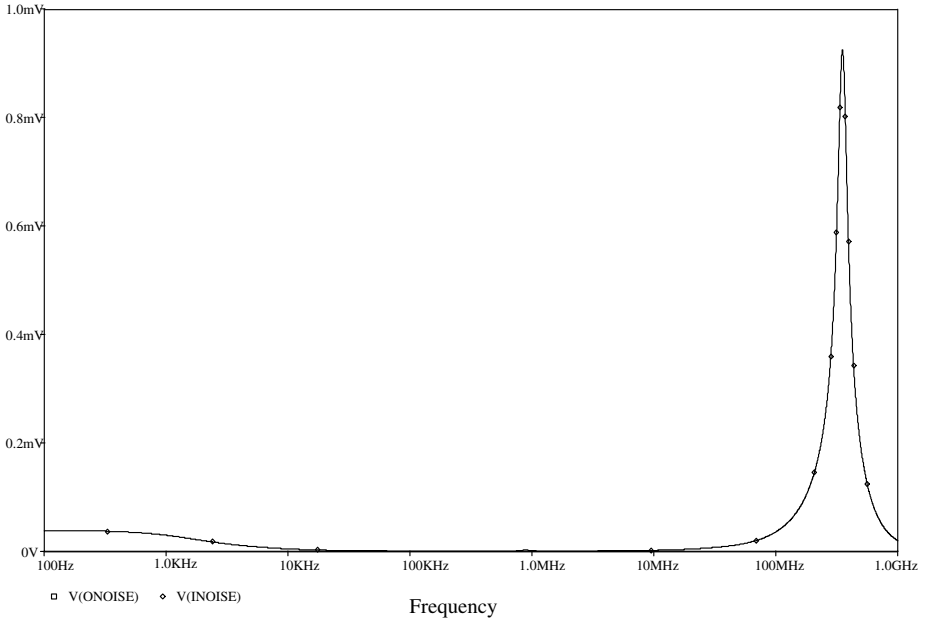

Fig. 5(d). Input/output referred noise of the TT using AD844 and MOS-C.

Figures 5(b) and 5(c) show the magnitude and phase responses of the simulated and the ideal responses respectively. From the simulation results of the TT using CFOA as a four-terminal device, it is seen that the actual response is very close to the ideal response.

Figure 5(d) shows the input/output referred noise.

5.3. *MOS-C pseudo TT circuit using CFOA as four-terminal device*

In this section the CFOA is used as a four-port network utilizing the Z port.

In this case the MOS-C Pseudo TT circuit shown in Fig. 6 and it is canonic as it uses only two grounded capacitors[10] and the circuit equations are given by:

$$\frac{V_{BP}}{V_{\text{in}}} = \frac{-\dfrac{KV_{G1}}{C_1}s}{s^2 + s\dfrac{K(V_{G3} - V_{G1})}{C_1} + \dfrac{K^2 V_{G2} V_{G3}}{C_1 C_2}}, \tag{15}$$

$$\frac{V_{LP}}{V_{\text{in}}} = \frac{\dfrac{K^2 V_{G1} V_{G2}}{C_1 C_2}}{s^2 + s\dfrac{K(V_{G3} - V_{G1})}{C_1} + \dfrac{K^2 V_{G2} V_{G3}}{C_1 C_2}}, \tag{16}$$

$$\omega_0 = K\sqrt{\frac{V_{G2} \cdot V_{G3}}{C_1 C_2}}, \quad Q = \frac{1}{(V_{G3} - V_{G1})}\sqrt{\frac{C_1}{C_2} V_{G2} V_{G3}}\,. \tag{17}$$

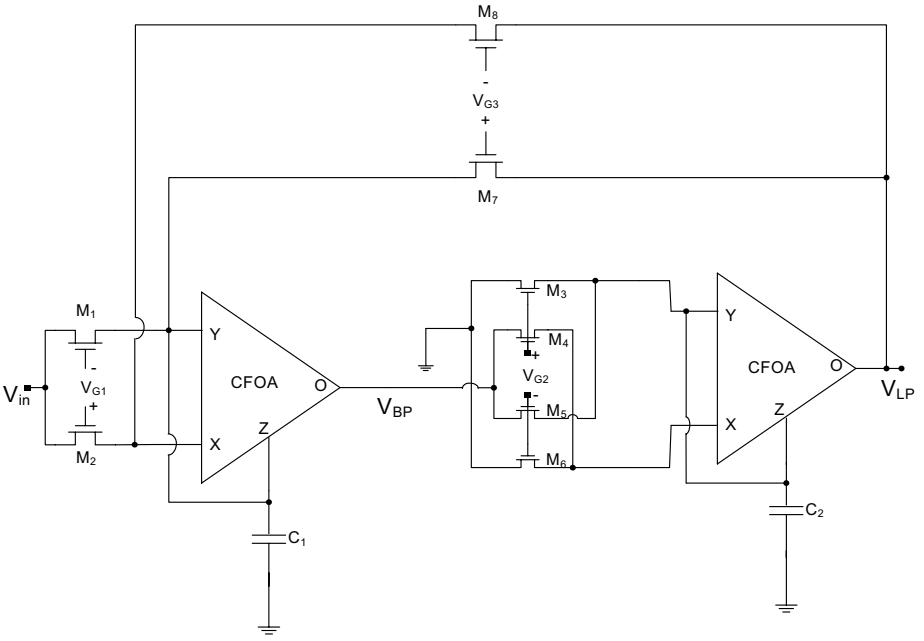

Fig. 6. TT filter using CFOA and MOS-C.[10]

From the above equations it is seen that there is a subtraction in the s term of the denominator, which makes the circuit sensitive and different from the TT circuit and that is why it is called Pseudo TT circuit. Another difference from the original TT circuit is that there is no independent control on the gain. This circuit is included only for completeness and will not be considered in the comparison of the MOS-C TT circuit family.

6. MOS-C TT Circuit Using OTRA

The operational transresistance amplifier (OTRA) is a three-terminal analog building block shown symbolically in Fig. 7(a) and is defined by the following matrix equation:

$$\begin{bmatrix} V_+ \\ V_- \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \cdot \begin{bmatrix} I_+ \\ I_- \\ I_o \end{bmatrix} \tag{18}$$

R_m is the transresistance gain.

Both the input and output terminals are characterized by low impedance. The input terminals are virtually grounded leading to circuits that are insensitive to stray capacitances.[13,15] Ideally the transresistance gain, R_m, approaches infinity, and applying external negative feedback will force the two input currents, I_+ and I_-, to be equal.

The circuit equations are the same as given by Refs. 12–14.

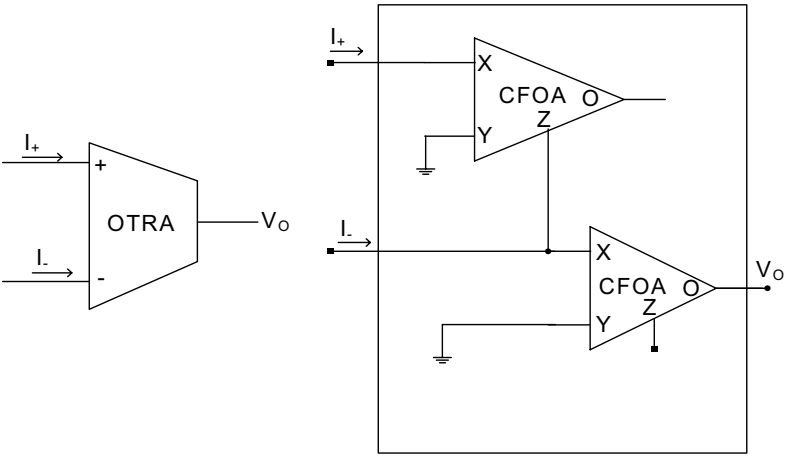

Fig. 7(a). OTRA symbol, (b) OTRA implementation using CFOAs.[12]

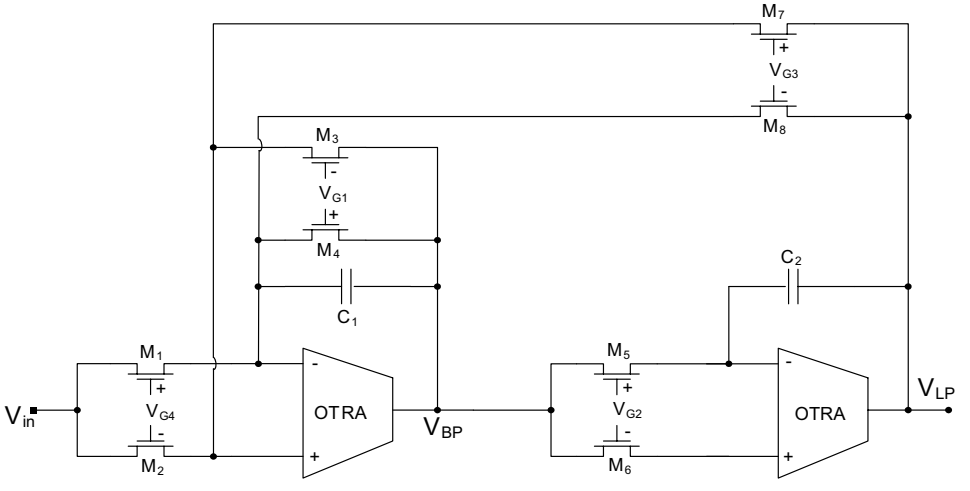

Fig. 7(c). TT filter using OTRA and MOS-C.[13]

The OTRA could be realized using two CFOAs as shown in Fig. 7(b). The PSpice simulations have been carried out for the circuit of Fig. 7(c) using the same design values as in the previous sections.

Figures 7(d) and 7(e) show the magnitude and phase responses of the simulated and the ideal responses respectively from simulating the TT using OTRA satisfying the requirements of the required filter.

Figure 7(f) shows the input/output referred noise.

It is worth noting that four alternative sign combinations of the bandpass and low-pass polarities by proper choice of the signs of V_{Gi} ($i = 1$ to 4) as explained in Ref. 13.

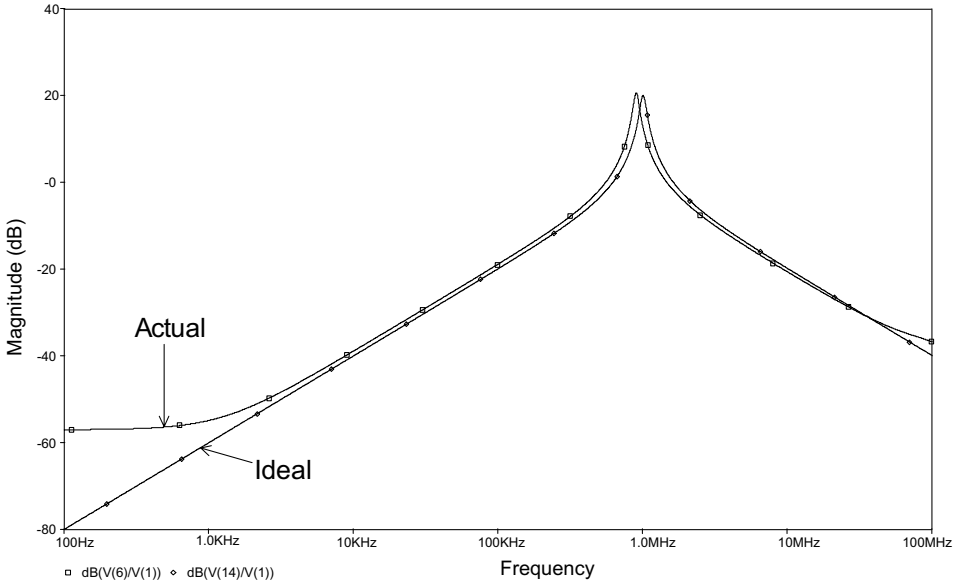

Fig. 7(d). Magnitude responses of TT using OTRA and MOS-C.

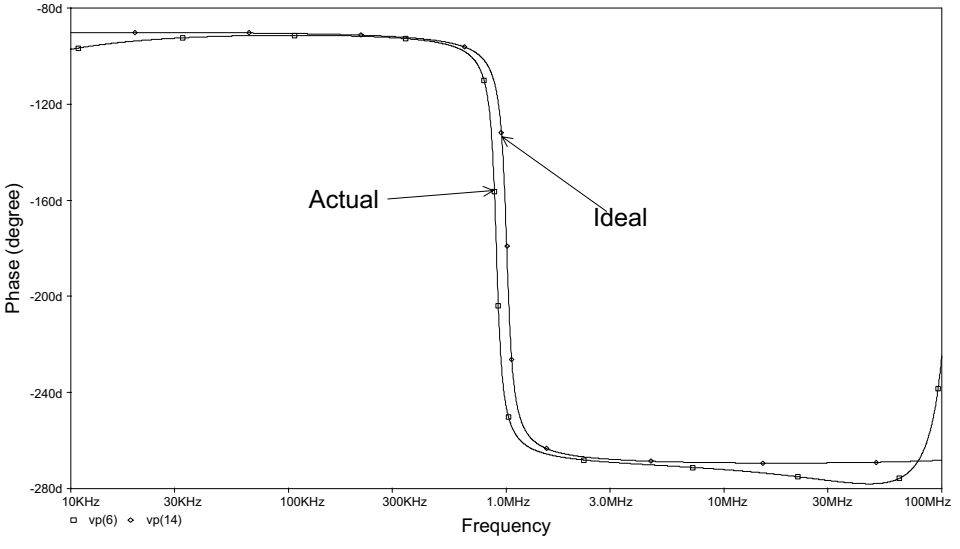

Fig. 7(e). Phase responses of TT using OTRA and MOS-C.

7. MOS-C TT Circuit Using DCVC

The DCVC is a versatile four-terminal analog building block based on cascaded connection of Modified Differential Current Conveyor MDCC[19] and a voltage follower.

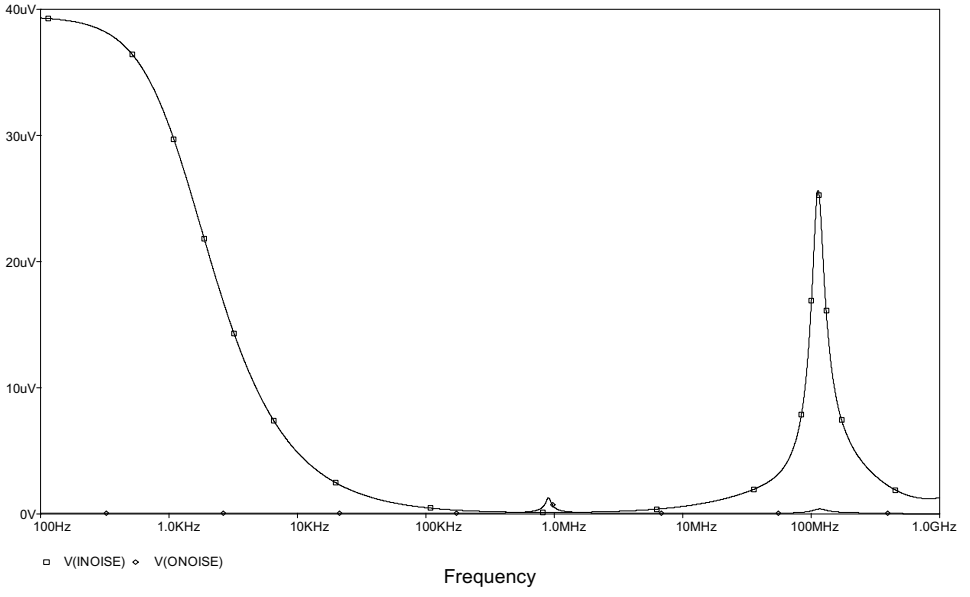

Fig. 7(f). Input/output referred noise of the TT using OTRA and MOS-C.

The DCVC is represented symbolically as shown in Fig. 8(a). It is characterized by the following matrix equation:

$$\begin{bmatrix} V_{X1} \\ V_{X2} \\ I_Z \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_{X1} \\ I_{X2} \\ V_Z \\ I_O \end{bmatrix}. \tag{19}$$

The circuit equations are the same as given by Eqs. (12) to (14).

The DCVC could be realized using two CFOAs as shown in Fig. 8(b).

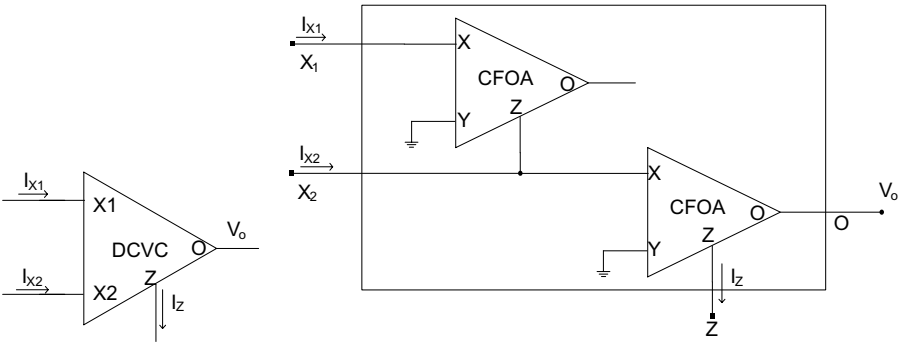

Fig. 8(a). DCVC symbol, (b) DCVC implementation using CFOAs.

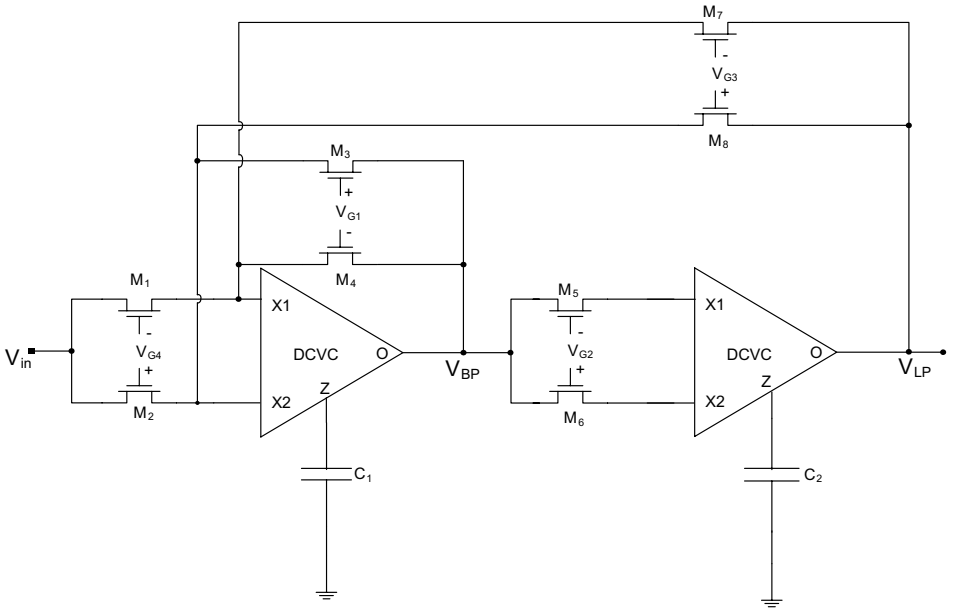

Fig. 8(c). TT filter using DCVC and MOS-C.[18]

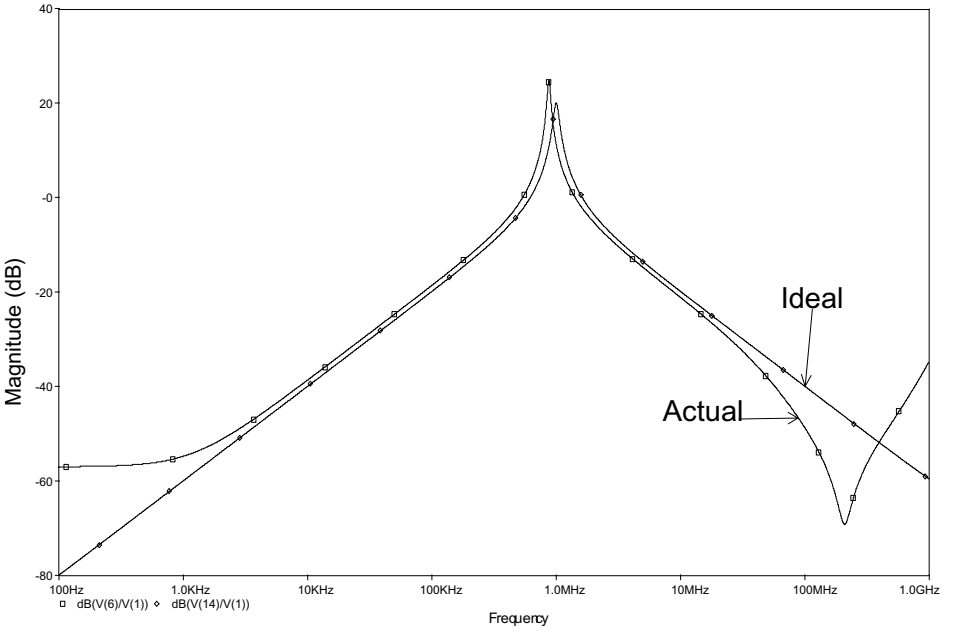

Fig. 8(d). Magnitude responses of TT using DCVC and MOS-C.

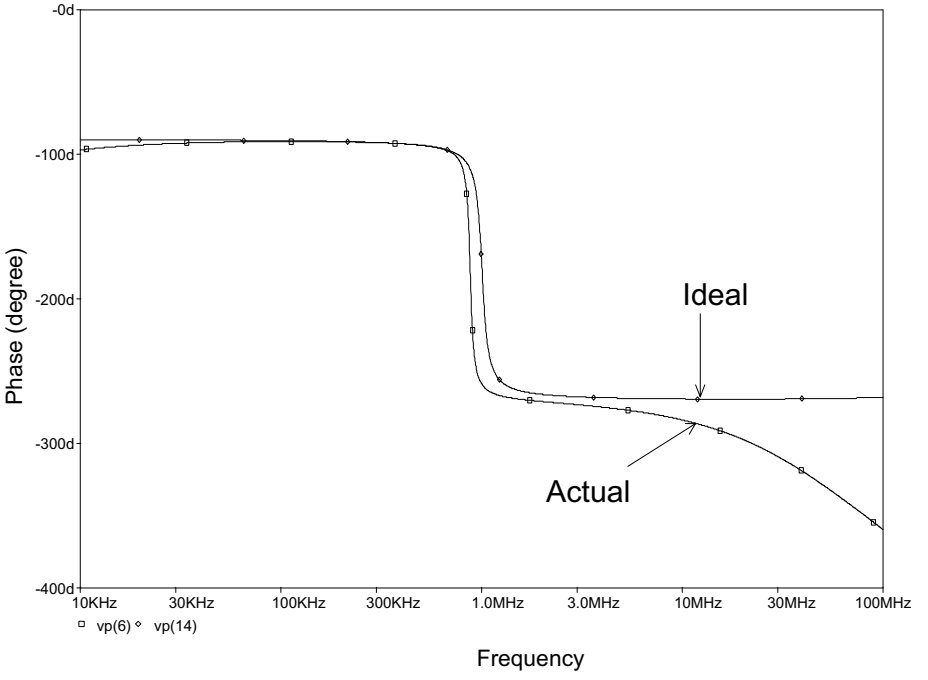

Fig. 8(e). Phase responses of TT using DCVC and MOS-C.

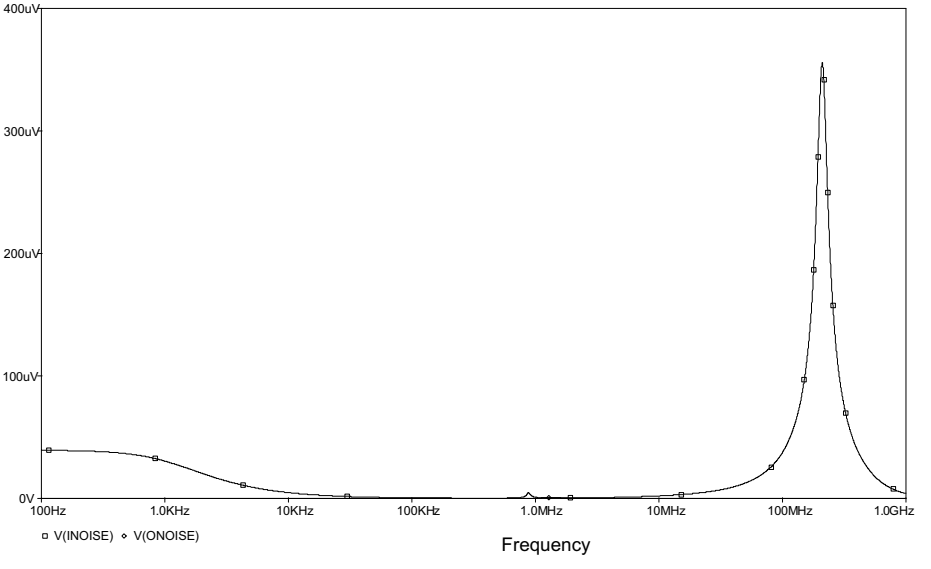

Fig. 8(f). Input/output referred noise of the TT using DCVC and MOS-C.

The PSpice simulations have been carried out for the circuit of Fig. 8(c) using the same design values as in the previous sections.

Figures 8(d) and 8(e) show the magnitude and phase responses of the simulated and the ideal responses respectively from simulating the TT using DCVC satisfying the requirements of the required filter. Figure 8(f) shows the input/output referred noise.

It is worth noting that four alternative sign combinations of the bandpass and low-pass polarities by proper choice of the signs of V_{Gi} ($i = 1$ to 4) as explained in Ref. 18.

8. MOS-C TT Circuit Using CMOS–VOA

In this section the CMOS–VOA given in Ref. 32 and shown here in Fig. 9(a) is used as the active building block in the TT circuit. The compensating capacitor C_c is taken 2.5 pF and the compensating resistor R_c is taken 10 kΩ. Table 3 includes the transistor aspect ratios of the CMOS circuit of Fig. 9(a). This CMOS VOA circuit is used in the TT circuit shown in Fig. 3(a).

The PSpice simulations have been carried out using 0.18 CMOS technology model from MOSIS to realize a bandpass response with $f_0 = 1$ MHz and $Q = 10$. The design values of the circuit parameters are $C_1 = C_2 = 55$ pF. The transistor aspect ratios of $(W/L) = (2\,\mu\text{m}/4\,\mu\text{m})$, $K' = 251.497\,\mu\text{A/V}^2$, and the gate voltages have been taken as $V_{G2} = V_{G3} = V_{G4} = 2.748$ V and $V_{G1} = 0.2748$ V. The CMOS–VOA is used with supply voltages of ± 1.5 V and V_{B1} of -1 V.

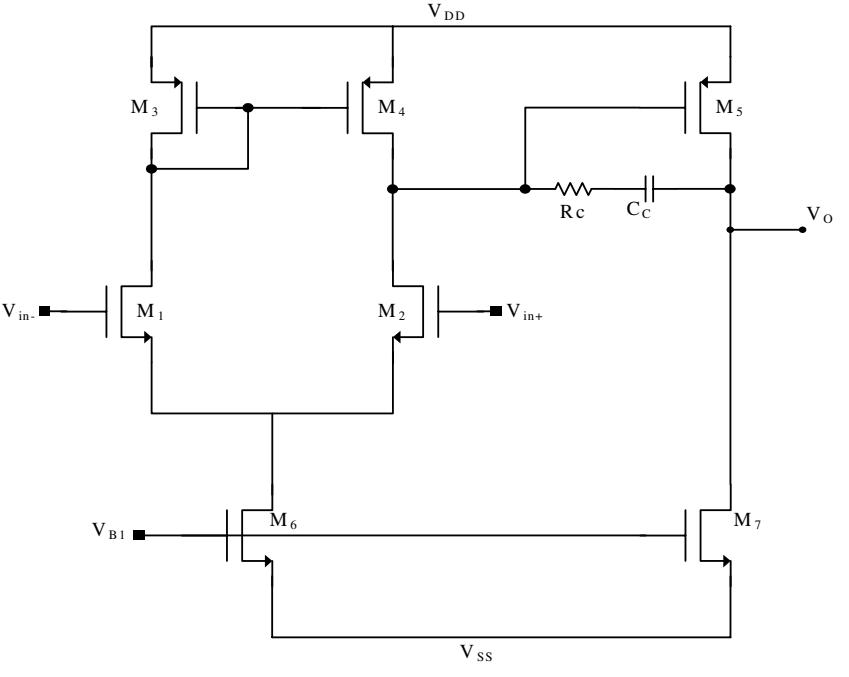

Fig. 9(a). CMOS realization of the op-amp[32] used to realize TT circuit.

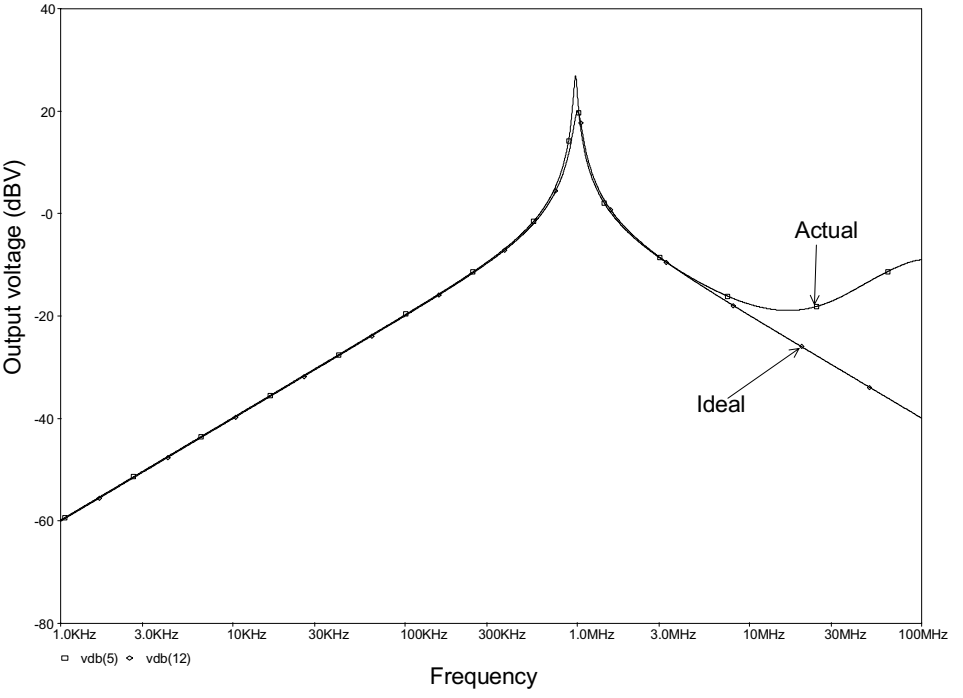

Fig. 9(b). Magnitude responses of TT using CMOS–VOA and MOS-C.

Figures 9(b) and 9(c) show the magnitude and phase responses of the simulated and the ideal responses respectively. It is seen that both responses are much better than those shown in Fig. 3 with the commercially available VOA. Figure 9(d) shows the input/output referred noise.

9. MOS-C TT Circuit Using CMOS–CFOA

In this section the CMOS–CFOA given in Ref. 30 and shown here in Fig. 10(a) is used as the active building block in the TT circuit. Table 4 includes the transistor aspect ratios of the CMOS circuit of Fig. 10(a). This CMOS–CFOA circuit is used in the TT circuit shown in Fig. 5(a).

The PSpice simulations have been carried out using 0.18 CMOS technology model from MOSIS to realize a bandpass response with $f_0 = 1\,\text{MHz}$ and $Q = 10$. The design values of the circuit parameters are the same as in the previous circuit. The CMOS–CFOA is used with supply voltages of $\pm 1.5\,\text{V}$, V_c and V_{B1} are taken $1.4\,\text{V}$ and $-0.8\,\text{V}$ respectively.

Figures 10(b) and 10(c) show the magnitude and phase responses of the simulated and the ideal responses respectively. It is seen that both responses are much better than those shown in Fig. 3(a) with the commercially available CFOA. Figure 10(d) shows the input/output referred noise.

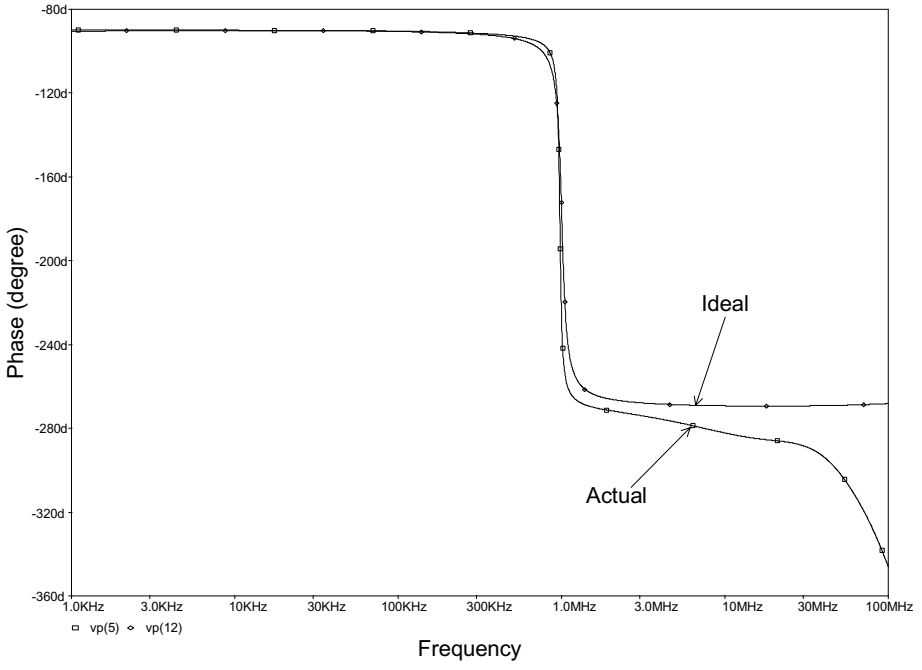

Fig. 9(c). Phase responses of TT using CMOS–VOA and MOS-C.

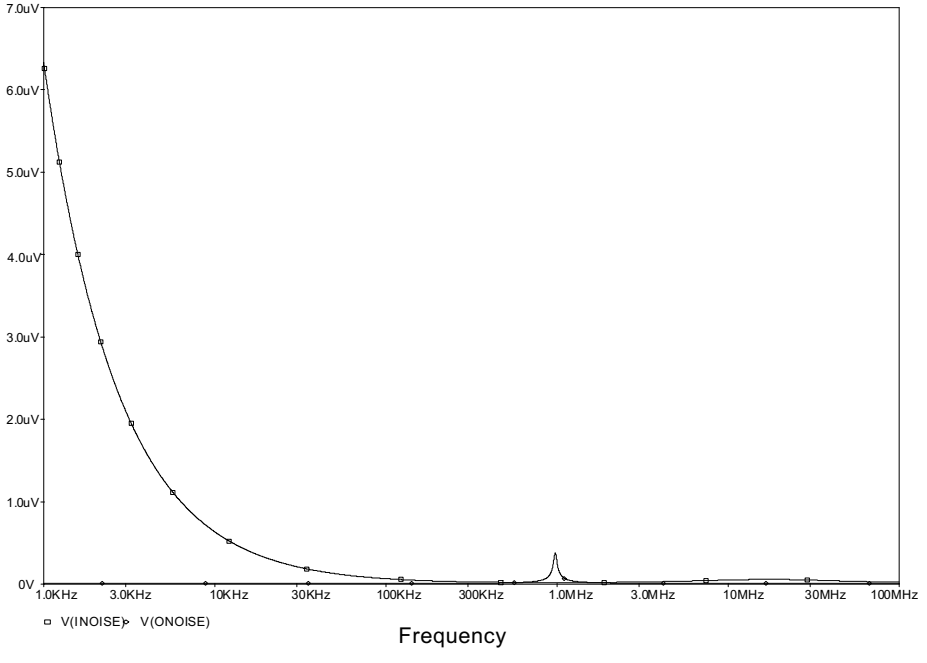

Fig. 9(d). Input/output referred noise of the TT CMOS–VOA and MOS-C.

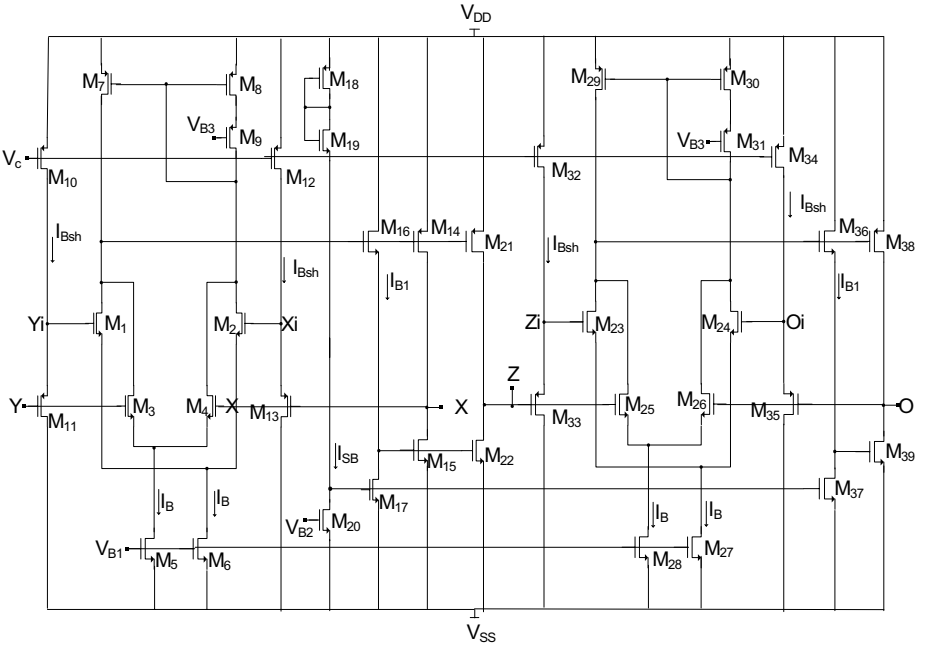

Fig. 10(a). CMOS realization of the CFOA[30] used to realize the TT circuit.

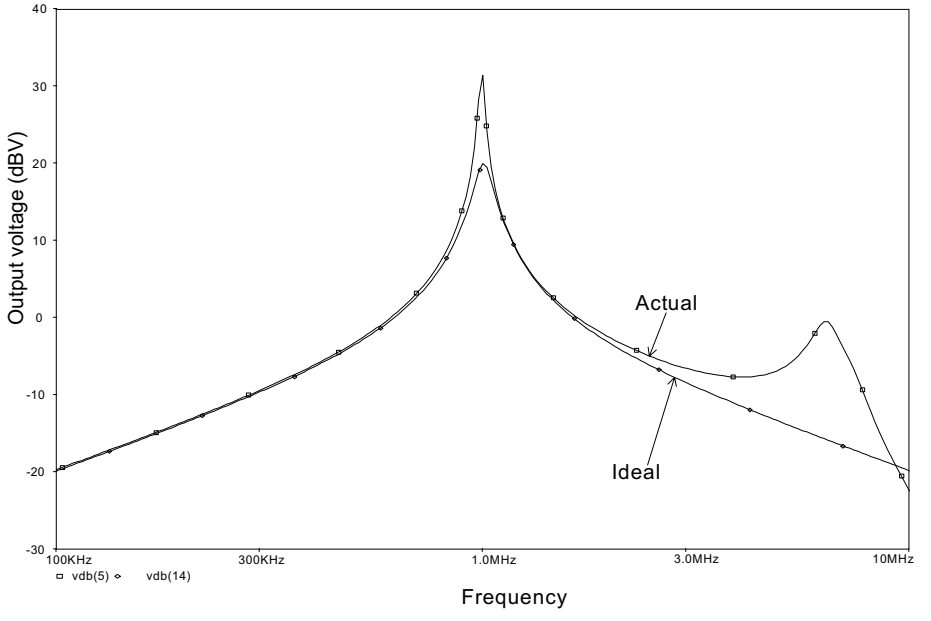

Fig. 10(b). Magnitude responses of TT using CMOS–CFOA and MOS-C.

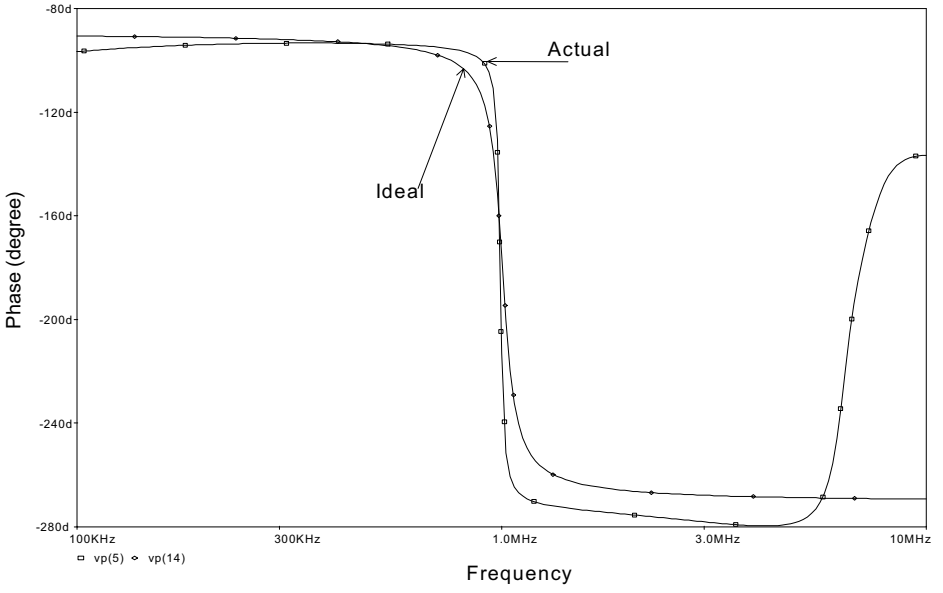

Fig. 10(c). Phase responses of TT using CMOS–CFOA and MOS-C.

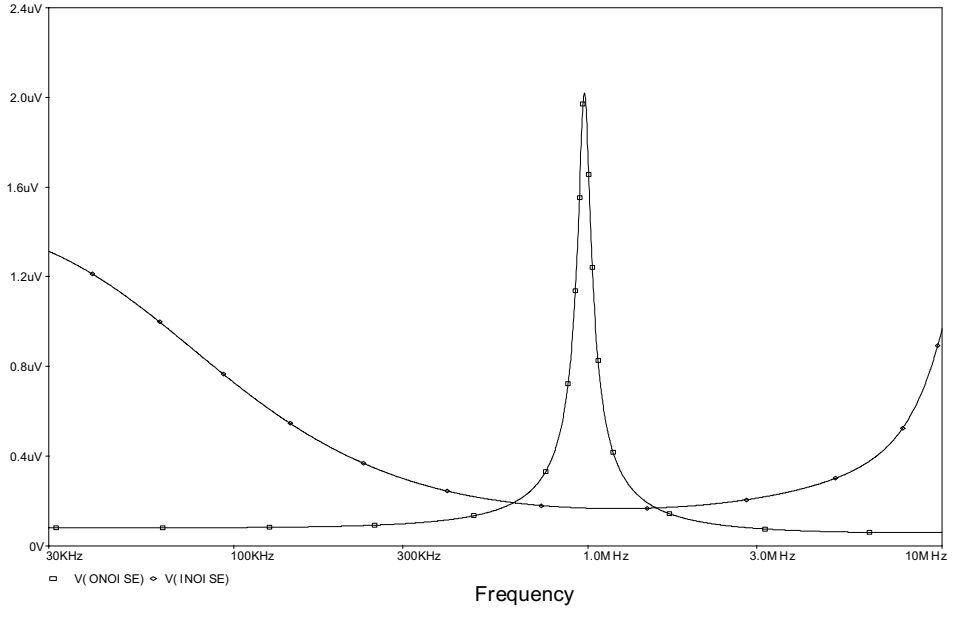

Fig. 10(d). Input/output referred noise of the TT CMOS–CFOA and MOS-C.

Table 1. Summary of Tow-Thomas MOS-C simulation results using VOA and CFOA.

		Fig. 3(a) Ref. 5	Fig. 4(a)	Fig. 5(a) Ref. 9	Fig. 7(c) Ref. 12	Fig. 8(c) Ref. 18
No. of capacitors	Grounded	2	2	6	0	2
	floating	2	2	0	2	0
Number/Type of active elements		2/LM741*	2/AD844**	2/AD844**	4/AD844**	4/AD844**
Number of transistors		16	16	16	8	8
Power Supplies (V_{dd}, V_{ss})		12 V, −12 V		5 V, −5 V		
Power consumption		78 mW	140 mW	140 mW	281 mW	281 mW
Input referred noise		$1.08\,\text{mV}/\sqrt{\text{Hz}}$	$38\,\mu\text{V}/\sqrt{\text{Hz}}$	$0.9\,\text{mV}/\sqrt{\text{Hz}}$	$39\,\mu\text{V}/\sqrt{\text{Hz}}$	$355\,\mu\text{V}/\sqrt{\text{Hz}}$
Output referred noise		$207\,\text{nV}/\sqrt{\text{Hz}}$	$1.4\,\mu\text{V}/\sqrt{\text{Hz}}$	$3.5\,\mu\text{V}/\sqrt{\text{Hz}}$	$1.3\,\mu\text{V}/\sqrt{\text{Hz}}$	$4.6\,\mu\text{V}/\sqrt{\text{Hz}}$
THD@ 1 MHz		76%	1.75%	4.7%	2.03%	2.29%

*LM741 macro model provided by National Semiconductor.
**AD844 macro model provided by Analog Devices.

Table 2. Percentage error from the ideal frequency ($f_{0\text{ideal}} = 1\,\text{MHz}$).

	$f_{0\text{Actual}}$ (KHz)	% error
Fig. 3(a) Ref. 5	366.438	63.56%
Fig. 4(a)	918.333	8.17%
Fig. 5(a) Ref. 9	881.049	11.9%
Fig. 7(c) Ref. 12	899.498	10.05%
Fig. 8(c) Ref. 18	877.001	12.3%

Table 3. Aspect ratio of the transistors of the CMOS–VOA circuit shown in Fig. 9.[32]

Transistors	W (μm)	L (μm)
M_1, M_2	56	3.6
M_3, M_4, M_5	90	4.8
M_7, M_8	0.18	1.8

10. MOS-C TT Circuit Using CMOS–OTRA

In this section the CMOS–OTRA given in Ref. 15 and shown here in Fig. 11(a) is used as the active building block in the TT circuit. Table 5 includes the transistor aspect ratios of the CMOS circuit of Fig. 11(a). This CMOS–OTRA circuit is used in the TT circuit shown in Fig. 7(c).

Figures 11(b) and 11(c) show the magnitude and phase responses of the simulated and the ideal responses respectively. Figure 11(d) shows the input/output referred noise.

Table 4. Aspect ratio of the transistors of the CFOA shown in Fig. 10.[30]

Transistors	W (μm)	L (μm)
$M_1 - M_4$, $M_{23} - M_{26}$	1.8	0.72
M_5, M_6, M_{27}, M_{28}	5.2	0.72
M_7, M_8, M_{29}, M_{30}	110	3.6
$M_{10} - M_{13}$, $M_{32} - M_{35}$	140	3.6
$M_{18} - M_{20}$	3.6	3.6
M_{16}, M_{17}, M_{36}, M_{37}	1	1
M_{14}, M_{21}, M_{38}	37	3.6
M_{15}, M_{22}, M_{39}	30	3.6

Table 5. Aspect ratio of the transistors of the OTRA circuit shown in Fig. 11.[15]

Transistors	W (μm)	L (μm)
$M_1 - M_3$, M_{12}, M_{13}	100	1.8
M_4, M_7	10	1.8
M_5, M_6	30	1.8
$M_8 - M_{11}$	50	1.8
M_{14}	50	3.6

Table 6. Summary of TT MOS-C simulation results using CMOS–VOA, CMOS–CFOA and CMOS–OTRA active blocks.

Active building block	CMOS–VOA Fig. 9 Ref. 32	CMOS–CFOA Fig. 10 Ref. 30	CMOS–OTRA Fig. 11 Ref. 15
Power Supplies (V_{DD}, V_{SS})		1.5 V, −1.5 V	
Power consumption	1.98 mW	4.62 mW	2.58 mW
Input referred noise	$6.33\,\mu V/\sqrt{Hz}$	$39.8\,\mu V/\sqrt{Hz}$	$558.6\,\mu V/\sqrt{Hz}$
Output referred noise	$0.382\,\mu V/\sqrt{Hz}$	$3.4\,\mu V/\sqrt{Hz}$	$0.722\,\mu V/\sqrt{Hz}$
THD@ 1 MHz	14.42%	14.2%	5.7%

The PSpice simulations have been carried out using 0.18 CMOS technology model from MOSIS to realize a bandpass response with $f_0 = 1$ MHz and $Q = 10$. The design values of the circuit parameters are the same as in the previous circuit. The CMOS–OTRA is used with supply voltages of ± 1.5 V and V_{B1} of -0.9 V.

It is seen that this circuit provides the best magnitude and phase responses among all circuits considered in this paper.

11. Conclusions

A detailed study of the MOS-C TT circuits using the VOA, CFOA, OTRA and DCVC has been presented. Both the VOA and the CFOA with the Z terminal open require four capacitors (two of them are floating) and the VOA has the highest frequency and Q deviations due to the finite gain bandwidth. Although the CFOA TT circuit uses grounded capacitors it is seen that the circuit of Fig. 5(a) uses six

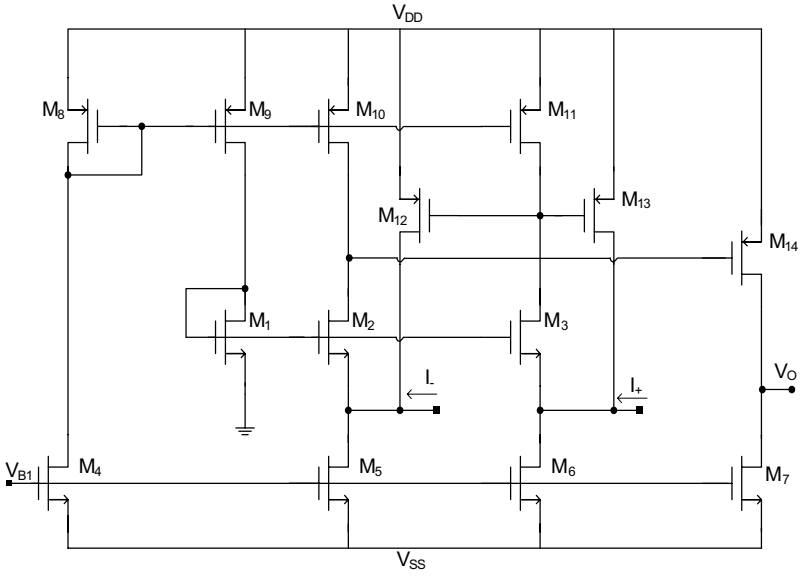

Fig. 11(a). CMOS realization of the OTRA[15] used to realize the TT circuit.

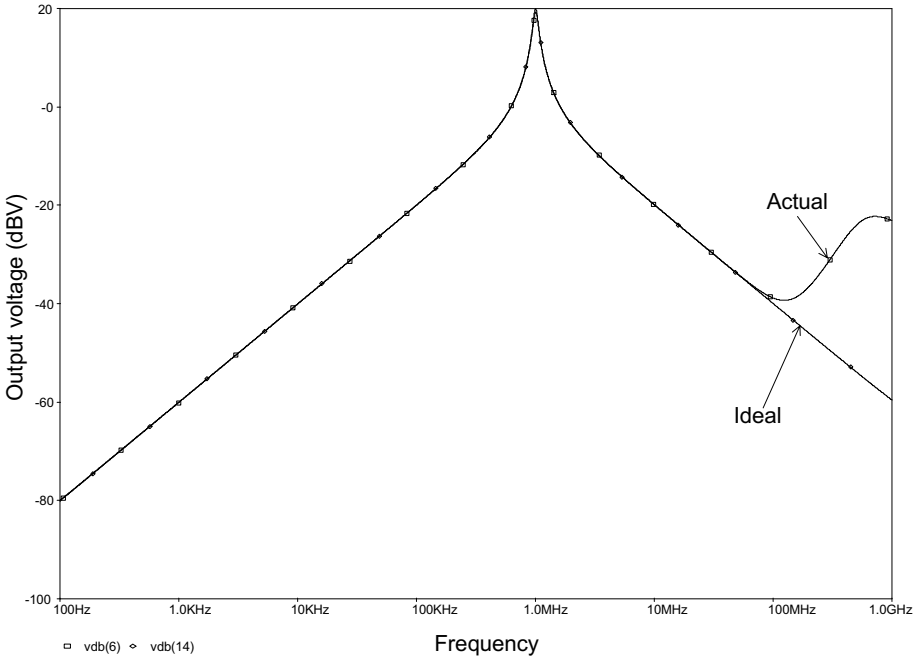

Fig. 11(b). Magnitude responses of TT using CMOS–OTRA and MOS-C.

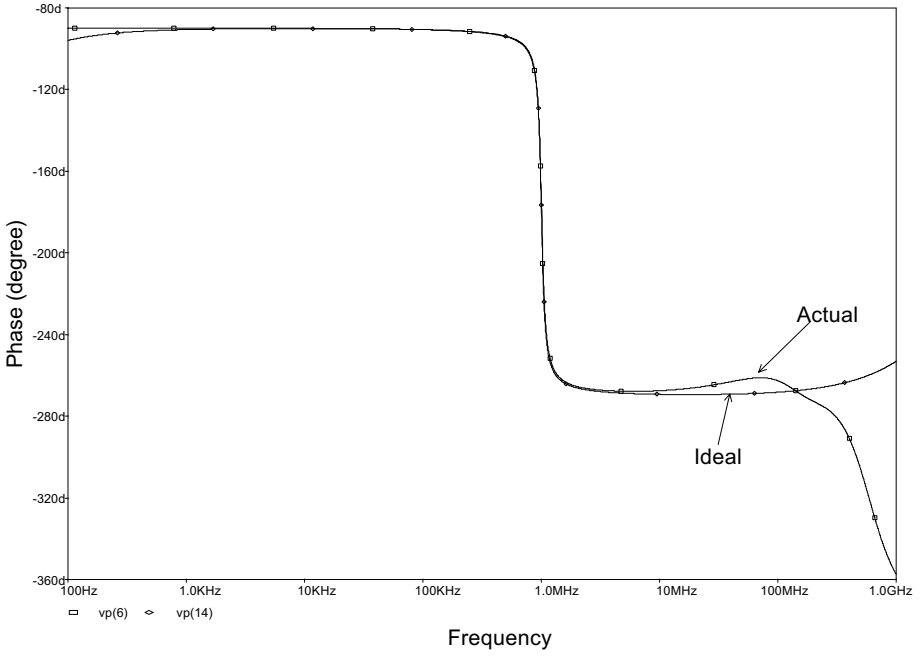

Fig. 11(c). Phase responses of TT using CMOS–OTRA and MOS-C.

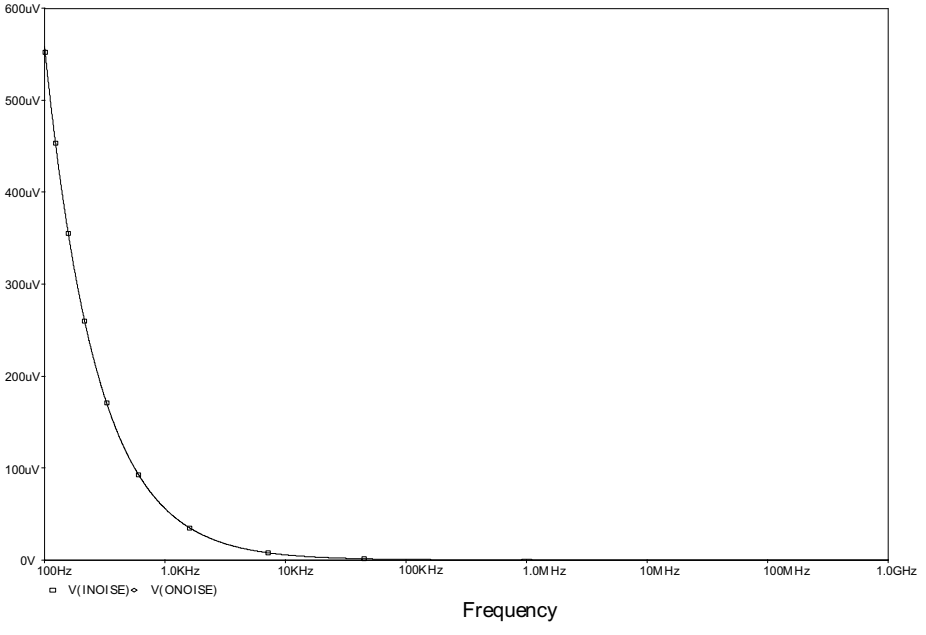

Fig. 11(d). Input/output referred noise of the TT CMOS–OTRA and MOS-C.

capacitors[9] and the canonic circuit of Fig. 6 has no independent control on the gain and is sensitive due to the subtraction in the s term in the denominator transfer function[10] and it is a Pseudo-TT circuit. Although the circuit of Fig. 7(b) uses only two capacitors, both of them are floating.[13] The DCVC MOS-C TT circuit uses two grounded capacitors only and achieves all the properties of the TT circuit. Besides, it can realize the bandpass and lowpass responses with the four sign combinations.[18] Of course this circuit is intended to be used with the CMOS–DCVC as the basic building block.[18]

Simulation results demonstrating the differences between circuits performance have been included. Table 1 includes comparison between different MOS-C TT circuits using the commercially available VOA and CFOA.

Table 6 includes comparison between different MOS-C TT circuits using CMOS–VOA, CMOS–CFOA and CMOS–OTRA.

It is seen the power consumption with CMOS active building blocks is much lower than the power consumption with the commercially available building blocks.

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