Low-Voltage Digitally Controlled Fully Differential Current Conveyor

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***Abstract*—Design and simulation of a digitally controlled CMOS fully differential current conveyor (DCFDCC) is presented. A novel current division network (CDN) is used to provide the digital control of the current gain between terminals X and Z of this DCFDCC. The proposed DCFDCC operates under low supply voltage of ± 1.5 V. The realization of the DCFDCC using the new CDN is presented by two approaches. First approach has linearly proportional current gain with the digitally controlled parameter of the CDN, while the second approach exhibits current gain between terminals X and Z greater than, or equal to, one. Applications of the DCFDCC in realizing second order universal active filter and variable gain amplifier are given. PSPICE simulation confirms the performance of the proposed blocks and its applications.**

***Index Terms*—Current conveyor (CC), current division network (CDN), current gain, fully differential buffer.**

I. Introduction

PROGRAMMABLE characteristic of an analog cell is a key feature that is used in so many useful applications. Analog or digital tuning can be employed to control the parameters of the analog cell. However, in low-voltage applications, there is a limitation on the allowable range of the analog tuning voltage. Hence, in these applications, the digital control is more attractive [1], [2]. Another example utilizing digital control is the interface with the digital signal processing unit (DSP) in the modern digital systems. For example, in modern wireless systems, all of the baseband signal processing is implemented digitally by DSP unit. There are baseband analog blocks required in the integrated wireless receiver such as highly linear filter section for out-of band blockers attenuation, tunable filter section for channel selection, and variable gain amplifier (VGA) for providing programmable gain setting and a primary requirement of those baseband analog blocks are to be digitally controlled [3].

Recently, the analog circuit design using current-mode approach has gained considerable attention. This stems from its inherent advantages of wide bandwidth, high slow rate, low power consumption, and simple circuitry [4], [5]. The second generation current conveyor (CCII) proposed by Sedra and Smith [6] is one of the most versatile current-mode building blocks. Since its introduction, it has been used in wide range of applications and several circuit realizations have been proposed for its implementation (e.g., [7]–[15]). The CCII is a single ended device, however, fully differential circuit configuration recently have been widely used in high frequency analog signal applications [5]. As compared to their single-ended counterparts, they have higher rejection capabilities to clock-feed-through, charge rejection errors and power supply noises, larger output dynamic range, higher design flexibility, and reduced harmonic distortion [16].

In this paper, a digitally controlled fully differential second generation current conveyor (DCFDCC) is presented, the DCFDCC is based on using fully differential buffer [5] with its output current sensed and copied to the current ports with a current gain where this current gain is digitally controlled. Precise gain control is achieved using a novel current division technique as will be discussed on the following section. Realization of the DCFDCC is presented using two approaches. The first approach is the direct realization, which has linearly proportional current gain with the digitally controlled parameter. Application of this approach is realizing digitally tuned universal filter with the advantage of linearly proportional tuned frequency to the digitally controlled parameter. In the second approach, the realization of the DCFDCC has current gain greater than, or equal to, one based on feedback technique. Application of this approach is realizing VGA with only one DCFDCC and the gain-tuning is achieved without any change of the external passive elements. Realization of the DCFDCC will be given in Section III then its applications will be given in Section IV.

II. Proposed Current Division Network

The block diagram of the proposed current division network (CDN) is shown in Fig. 1(a). It consists of n current division cells (CDCs). According to the current division principle, each CDC of this network has three output currents. The output currents of the current division cell number i (CDC_i) are I_{O1i}, I_{O2i}, and I_{O3i} whose relations to the input current of this cell (Ii_i) are expressed as follows:

$$I_{O1i} = a_i \frac{Ii_i}{2} \tag{1}$$

$$I_{O2i} = \bar{a}_i \frac{Ii_i}{2} \tag{2}$$

$$I_{O3i} = \frac{Ii_i}{2} \tag{3}$$

where a_i is the digital control bit of this cell. As shown from Fig. 1(a), I_{O3i} of the CDC_i is used as the input current of the

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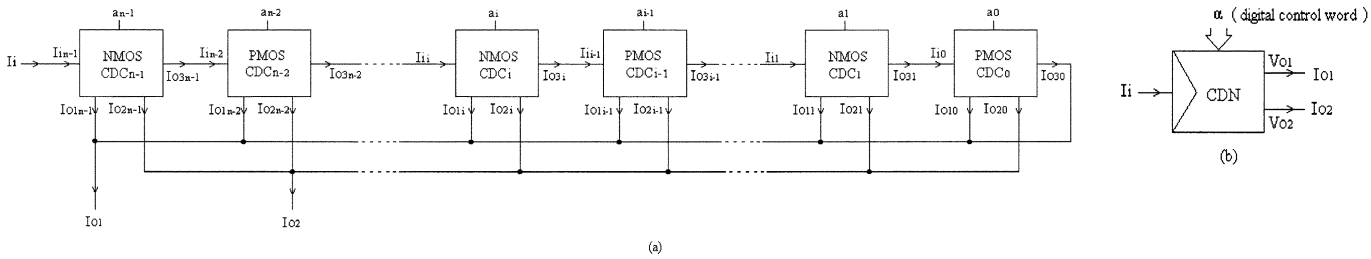

Fig. 1. (a) Block diagram of the proposed CDN. (b) Symbol of the proposed CDN.

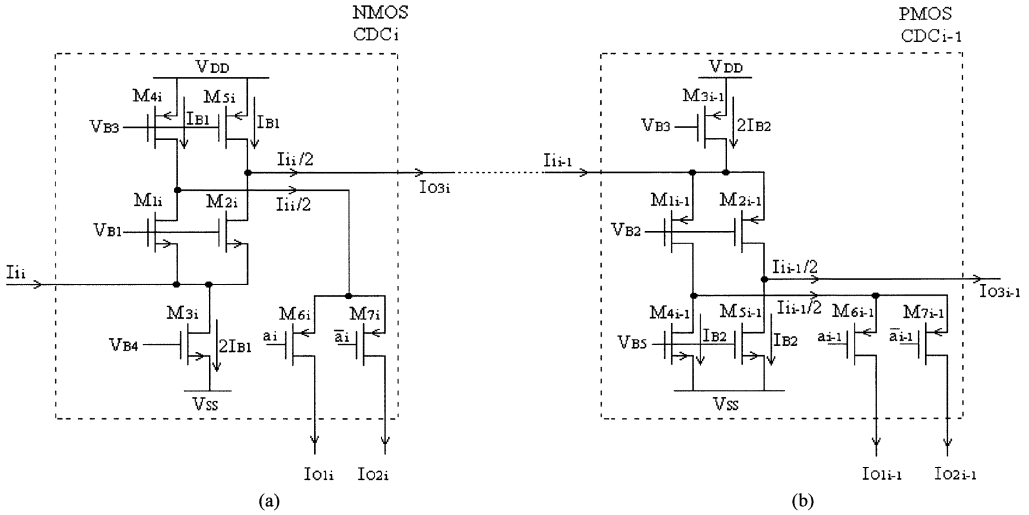

Fig. 2. (a) Circuit realization of the proposed nMOS current division cell. (b) Circuit realization of the proposed pMOS current division cell.

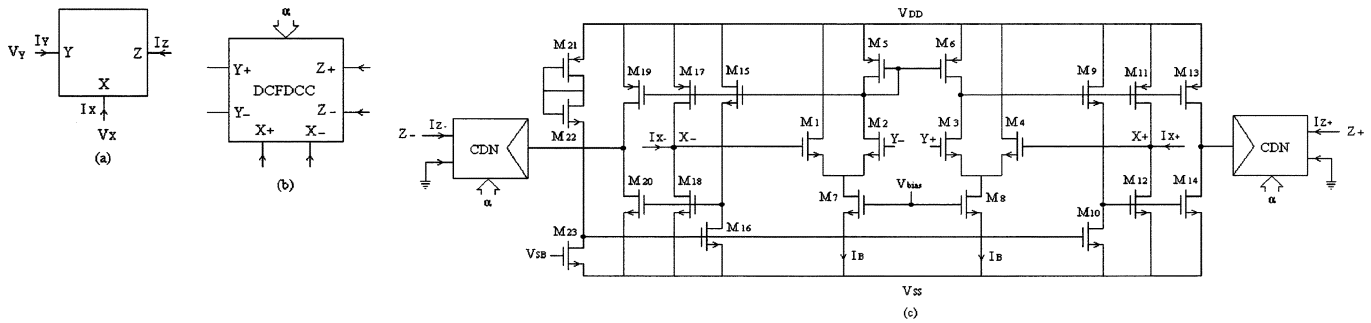

Fig. 3. (a) Symbol of the single-ended CCII. (b) Symbol of the first realization of the DCFDCC. (c) CMOS circuit of the first realization of the DCFDCC.

next stage Ii_{i-1} and I_{O30} is added to I_{O1}. Therefore, the two output currents of the CDN are given by

$$I_{O1} = I_{O30} + \sum_{i=0}^{i=n-1} I_{O1i} = \frac{1}{2^n}\left(1 + \sum_{i=0}^{i=n-1} 2^i a_i\right) Ii \quad (4)$$

$$I_{O2} = \sum_{i=0}^{i=n-1} I_{O2i} = \frac{1}{2^n}\left(\sum_{i=0}^{i=n-1} 2^i \bar{a}_i\right) Ii \quad (5)$$

$$\alpha = \frac{I_{O1}}{Ii} = \frac{1}{2^n}\left(1 + \sum_{i=0}^{i=n-1} 2^i a_i\right). \quad (6)$$

Hence, the current gain (α) of the proposed CDN is digitally controlled where α is less than, or equal to, one. The symbol of the CDN is shown in Fig. 1(b).

The traditional approach to implement the CDN is to use the well-known resistive R-$2R$ ladder circuit. For proper operation, all the resistance in the ladder must be matched. This may be

TABLE I
ASPECT RATIOS OF TRANSISTORS CONSTRUCTING DCFDCC

Circuit	Transistor	Aspect Ratio [μm/μm]
Proposed CDN of Fig. 2	M_{1i}, M_{2i}.	80/1
	M_{3i}.	120/2
	M_{4i}, M_{5i}.	240/2
	M_{1i-1}, M_{2i-1}.	120/1
	M_{3i-1}.	240/2
	M_{4i-1}, M_{5i-1}.	80/2
DCFDCC of Fig. 3(c)	M_1, M_2, M_3, M_4.	80/1
	M_5, M_6.	100/2
	M_7, M_8.	80/2
	M_9, M_{10}, M_{15}, M_{16}.	2/1
	M_{12}, M_{14}, M_{18}, M_{20}, M_{22}.	150/2
	M_{11}, M_{13}, M_{17}, M_{19}, M_{21}.	200/2

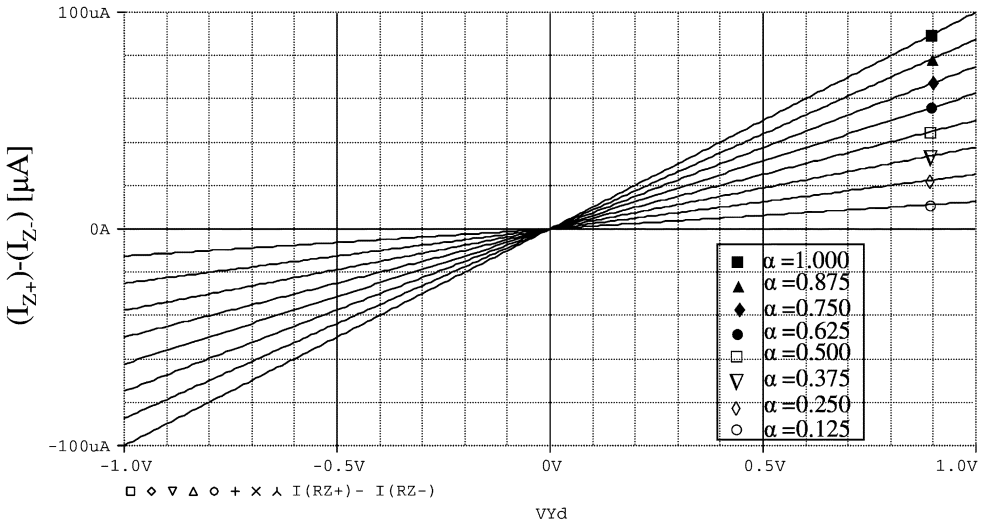

Fig. 4. DC response of the Z-terminals current of the first realization of the DCFDCC. α is scanned from 0.125 to 1 with 0.125 step.

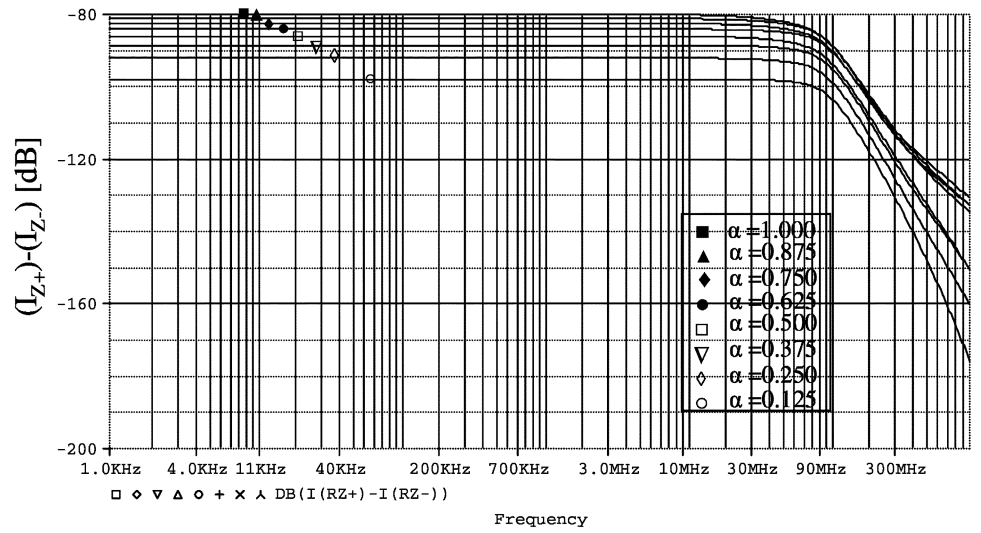

Fig. 5. AC response of the Z-terminals current of the first realization of the DCFDCC. α is scanned from 0.125 to 1 with 0.125 step.

very difficult to achieve in practice especially when number of bits increases. Also, the output nodes (I_{O1} and I_{O2}) of this CDN should be at virtual ground voltages. This prevents the use of this circuit in the applications where the input resistance of the stage next to the CDN is finite. Furthermore, there is trade off between the input and output resistances by choosing the value of R.

A better approach to implement the CDN is to use of MOS ladder circuit [17]. The structure of this circuit is similar to the classical resistor based R-$2R$ ladder. In this approach, the current division function is inherently linear, independent of the input current, and independent of the operation region of the MOS transistors constructing the ladder circuit. However, MOS ladder circuit still suffers from the drawbacks of the resistive ladder stated above such as the need of matching all the transistors in the circuit, and the requirement of virtual ground voltages at the output nodes (I_{O1} and I_{O2}).

Both CDNs given in [1] and [2] have high output resistance since the output currents are drown from the drain of the transistors. Hence, no need for virtual ground nodes. Besides, only the transistors inside each CDC are required to be matched rather than matching all the transistors in the entire CDN. Hence, the matching-requirements are relaxed. Since the transistors are assumed to operate in the saturation region, higher current drive capability is expected than in the case of the MOS ladder for the same aspect ratios of transistors. Moreover, the CDN given in [1] has advantages over its counterpart in [2] where there is no limitation on the number of the control bits due to voltage supply, and no need to external biasing voltages. However, both [1] and [2] circuits suffer from the drawback of operating in only single direction of the input current.

The proposed CDN is based on alternatively using nMOS-CDC followed by pMOS-CDC shown in Fig. 2. This will give the CDN the advantage of unlimited number of bits due to the supply voltage limitation where the voltage levels are regenerated from one cell to another. The proposed CDN also has advantages based on the structure of the CDC itself such as low input impedance, and high output impedance. Hence, no need for virtual ground nodes. Also, the matching-requirements are relaxed since only the transistors inside each CDC are required

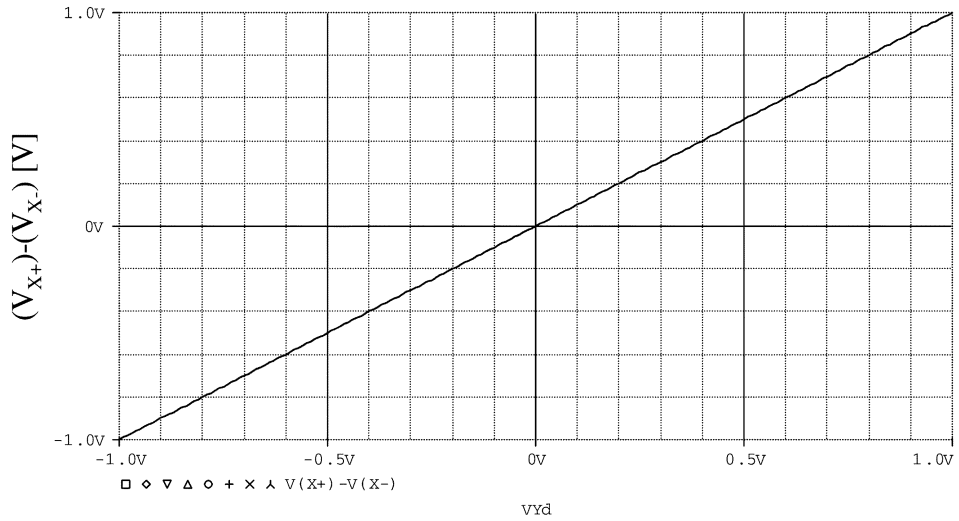

Fig. 6. DC response of the X-terminals voltage of the first realization of the DCFDCC. α is scanned from 0.125 to 1 with 0.125 step.

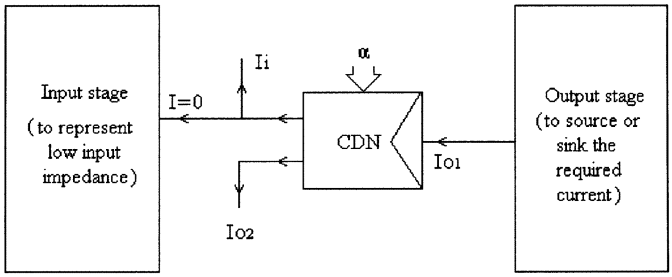

Fig. 7. Basic idea of the current gain approach.

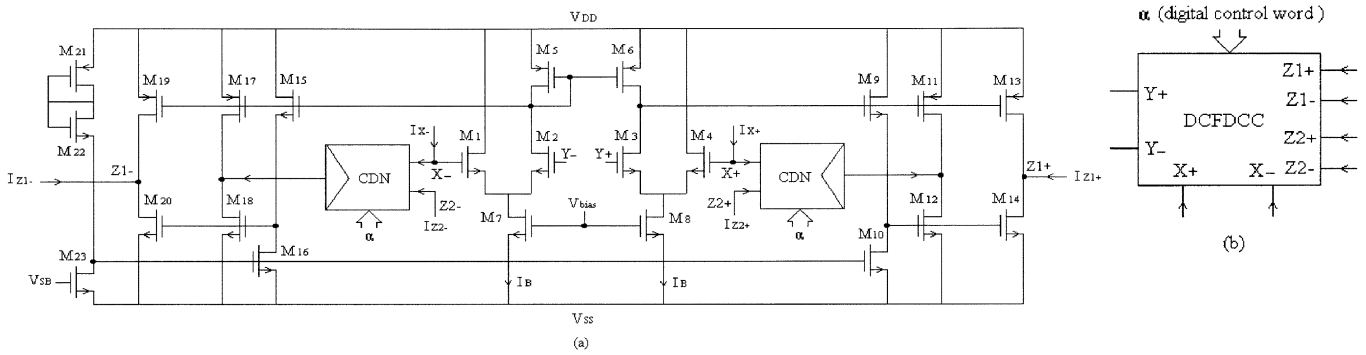

Fig. 8. (a) CMOS realization of the second realization of the DCFDCC. (b) Symbol of the second realization of the DCFDCC.

to be matched rather than matching all the transistors in the entire CDN. Moreover, the proposed CDN has the ability of driven by bidirectional input current.

The proposed nMOS-CDC is shown in Fig. 2(a). M_{1i} and M_{2i} are matched and assumed to be operated in saturation region. M_{4i} and M_{5i} are matched and operate as current sources with drain current equal to I_{B1}. Also, M_{3i} operates as current source with drain current equal to $2I_{B1}$. Using the drain current equation of MOS transistor in saturation region, the input current of the $\mathrm{CDC}_i(Ii_i)$ is divided equally between the matched transistors M_{1i} and M_{2i} as shown in (7)

$$I_{M1i} = I_{M2i} = I_{B1} - \frac{Ii_i}{2}. \tag{7}$$

Hence, a current equals $Ii_i/2$ is transferred to I_{O3i} as stated in (3). Only one transistor of M_{6i} or M_{7i} is on at a time due the value the digital control bit a_i. Hence, the current of $Ii_i/2$ is either switched to I_{O1i} or I_{O2i} as given in (1) and (2). The operation of the pMOS-CDC shown in Fig. 2(b) is typically as its nMOS counterpart.

III. Realizations of DCFDCC

Basically, a CCII is a three-terminal device [as shown in Fig. 3(a)] derived by interconnecting a voltage and current follower. An ideal CCII exhibits infinite resistance at terminals Y and Z, and zero resistance at terminal X. The voltage at terminal X follows that at terminal Y, and the current at terminal Z is a replica of the current at terminal X. Positive and negative CCIIs are defined according to the follow direction of the Z-terminal current. Of course, a CCII− can be derived from

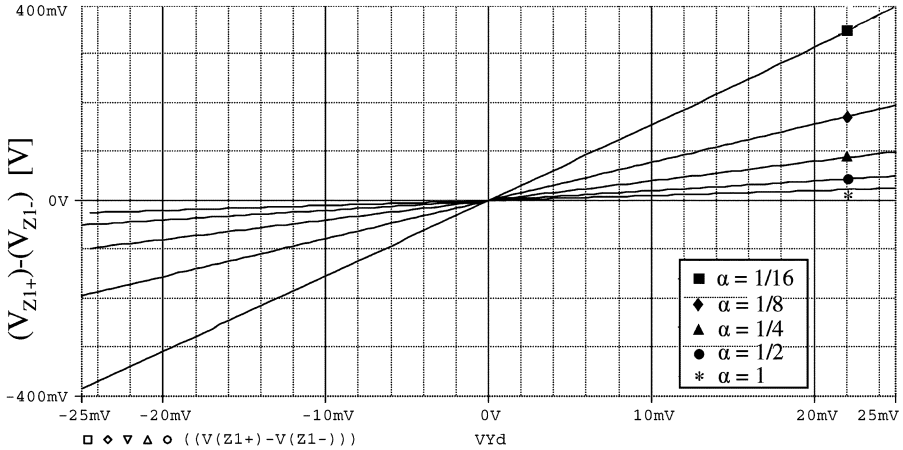

Fig. 9. DC response of the Z1-terminals differential voltage of the second realization of the DCFDCC at gain setting 1, 2, 4, 8, and 16 ($\alpha = 1, 1/2, 1/4, 1/8,$ and $1/16$ respectively).

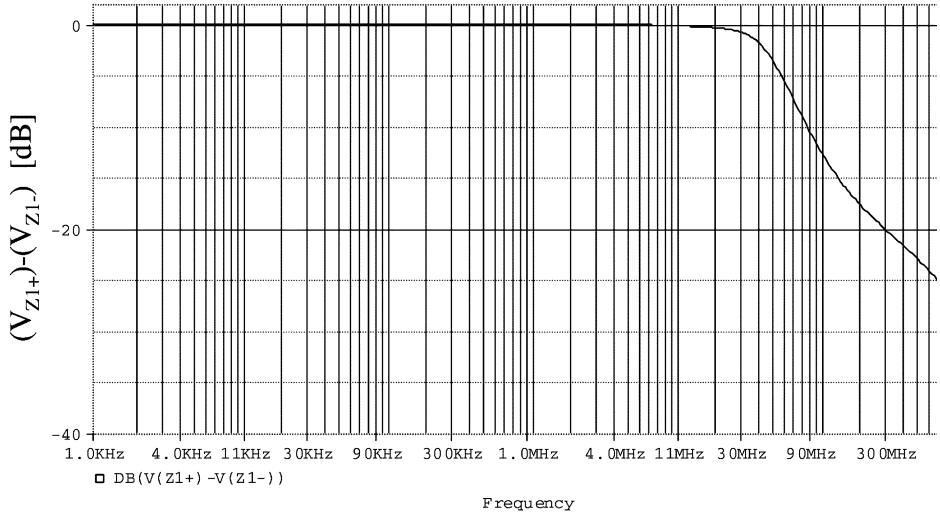

Fig. 10. AC response of the Z1-terminals differential voltage of the second realization of the DCFDCC ($\alpha = 1$).

a CCII+ by simply using current mirrors to invert the output current direction, and vice versa [15]. The fully differential second generation current conveyor is a six-terminal device and had the notation DCFDCC for simplicity. In the following subsections, first approach of the DCFDCC using direct realization will be presented. Then, a current gain approach to operate the CDN with current gain greater than one will be given. Finally, second realization of the DCFDCC using current gain approach will be presented.

A. Direct Realization of the DCFDCC

The DCFDCC, represented symbolically as in Fig. 3(b), can be realized using Class-AB fully differential buffer (FDB) presented in [5] with its output current is sensed and copied to the current port and followed by the proposed bidirectional CDN as shown in Fig. 3(c). The DCFDCC is represented mathematically by the following matrix equation:

$$\begin{pmatrix} V_{Xd} \\ I_{Zd} \\ I_{Yd} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 1 \\ \alpha & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} I_{Xd} \\ V_{Zd} \\ V_{Yd} \end{pmatrix} \tag{8}$$

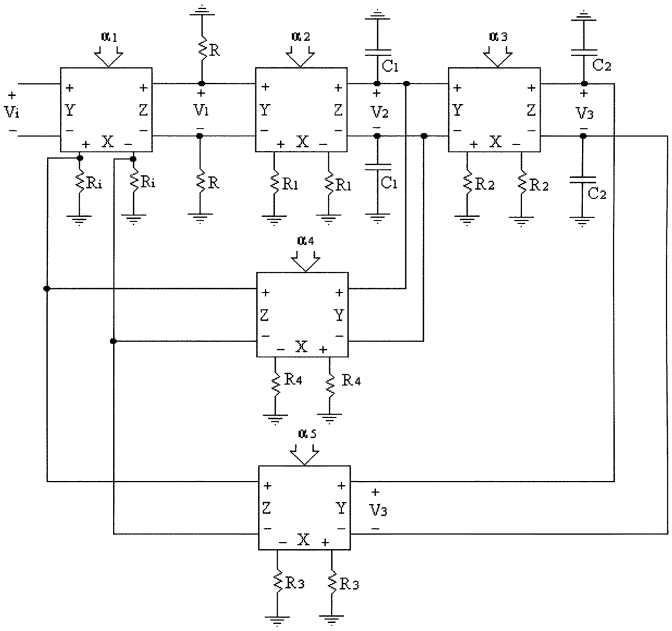

Fig. 11. DCFDCC-based universal active filter.

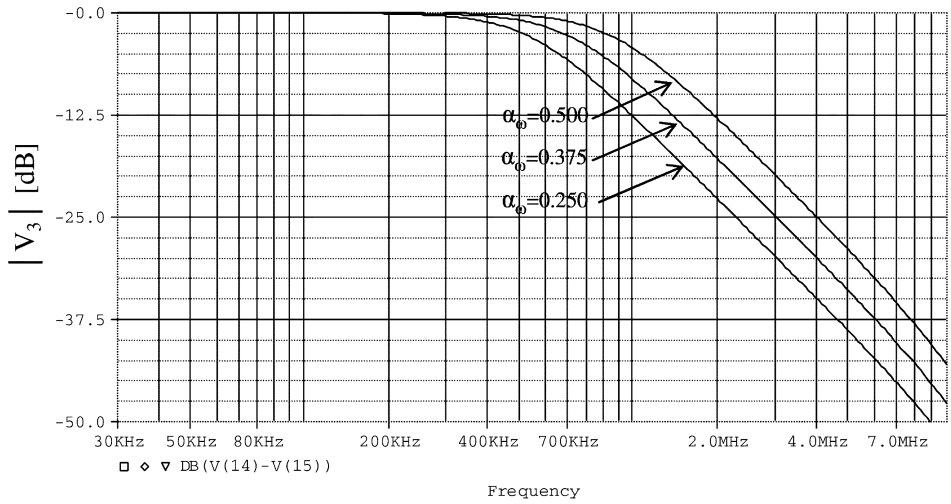

Fig. 12. Magnitude response the differential voltage low-pass output.

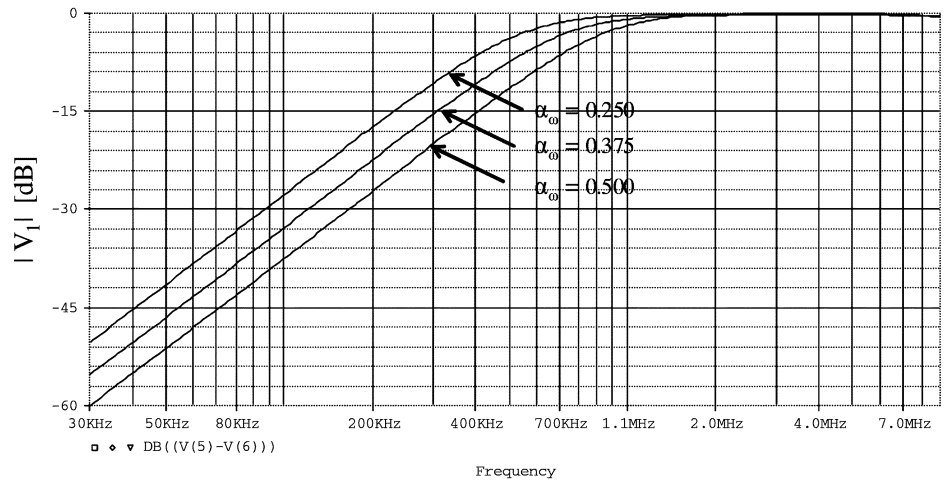

Fig. 13. Magnitude response the differential voltage high-pass output.

where $V_{Xd} = (V_{X+}) - (V_{X-}), V_{Yd} = (V_{Y+}) - (V_{Y-}), I_{Zd} = (I_{Z+}) - (I_{Z-}), I_{Xd} = (I_{X+}) - (I_{X-})$, and $(I_{Y+}) = (I_{Y-}) = 0$. The FDB consists of two matched differential pairs (M_1, M_2) and (M_3, M_4), matched biasing currents sources transistors (M_7, M_8), matched active load transistors (M_5, M_6), and two Class-AB output stages (M_9–M_{12}, and M_{15}–M_{18}, and the biasing of the output stage M_{21}–M_{23}). The differential input is applied to the two high impedance terminals of the nMOS transistors M_2 and M_3. The tail current transistors M_7 and M_8 carry equal bias current I_B, therefore

$$I_{M1} + I_{M2} = I_{M3} + I_{M4}. \tag{9}$$

By the current mirror action of transistors M_5 and M_6

$$I_{M2} = I_{M3}. \tag{10}$$

From the above equations, its follows that $I_{M1} = I_{M4}$. Hence, the two matched differential pairs carry equal differential and common mode current values. Therefore

$$(V_{X+}) - (V_{X-}) = (V_{Y+}) - (V_{Y-}). \tag{11}$$

To maintain a good current drive capability with low output impedance terminals, Class-AB output stages are used. Transistors M_{11}–M_{12} and M_{17}–M_{18} form the push pull output stage transistors. The level shift circuits formed by M_9–M_{10} and M_{15}–M_{16} are used to realize a controlled floating voltage sources that controls the standby current through the output stage transistors. The standby current is adjusted by the biasing circuit formed of M_{21}–M_{23}. Transistors M_{13}–M_{14} and M_{19}–M_{20} are used to copy the current of the Class-AB output stages of the FDB and transfer it to the proposed bidirectional CDNs. Hence, the current gain, between X and Z-terminals, is linearly proportional to the digitally controlled parameter α as given in (8).

The DCFDCC circuit in Fig. 3(c) has been simulated using PSPICE simulation with 0.5-μm CMOS parameters. The power-supply voltages $V_{\rm DD}$ and $V_{\rm SS}$ are balanced (1.5 and -1.5 V, respectively). $n = 6$ bits and the aspect ratios of the transistors are given in Table I. I_{B1} and I_{B2} of the proposed CDN are adjusted to 100 and 50 μA, respectively. Also, I_B of the FDB is set to 100 μA. The Z-terminals characteristics are tested through Figs. 4 and 5. In Fig. 4, the differential Z-terminals current of the DCFDCC is shown when the differential Y-terminals voltage is swept from -1 to 1 V for different values of the digitally controlled parameter α ranging from 0.125 to 1 with step of 0.125. Z-terminals are loaded by $R_{Z+} = R_{Z-} = 1$

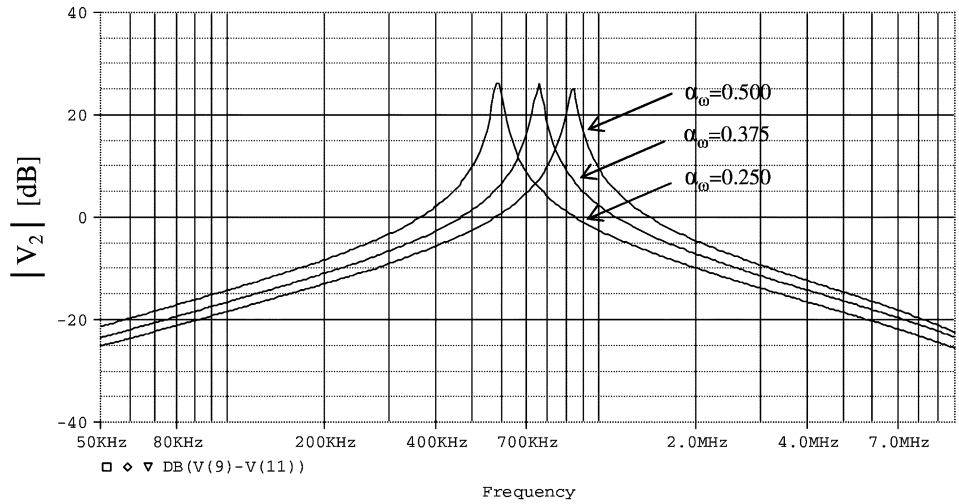

Fig. 14. Magnitude response the differential voltage bandpass output (different f_0 and the same Q: $\mathrm{Q} = 20$).

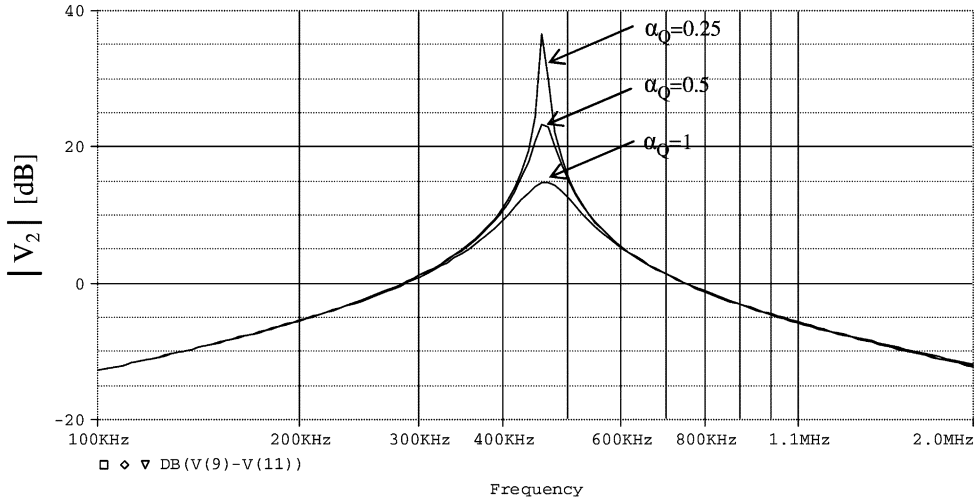

Fig. 15. Magnitude response the differential voltage bandpass output (different Q and the same f_0 : $f_0 = 450$ kHz).

kΩ while X-terminals are loaded by $R_{X+} = R_{X-} = 10$ kΩ. Fig. 5 shows the ac response of the Z-terminals current for the same α setting of Fig. 4 from which it is seen that the bandwidth is approximately constant and equal to 64.6 MHz. The X-terminals dc response is shown in Fig. 6 from which it is clear that the differential X-terminals' voltage follows the differential Y-terminals' voltage for different values of α setting with maximum linearity error less than 0.1%. The time response of the circuit has been simulated by calculating the percentage of the total harmonic distortion (THD) at the Z-terminals of the DCFDCC when the input signal at Y-terminals had 1-MHz frequency and 1-V peak-to-peak amplitude. For $\alpha = 1,\ 0.5$, and 0.25, the percentage of THD was found to be less than 1%.

B. Current Gain Approach to Operate the CDN With Current Gain Greater Than One

The basic idea of using the CDN with current gain greater than, or equal to, one is shown in Fig. 7. It depends on injecting

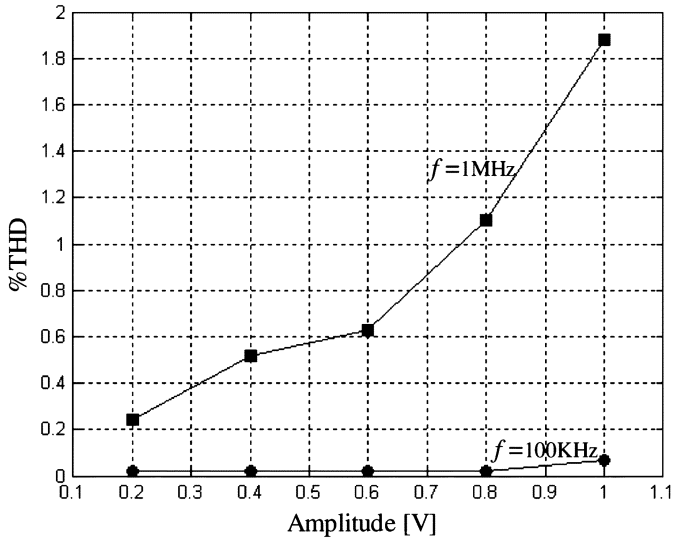

Fig. 16. Total harmonic distortion of the low-pass output (input frequency is 100 kHz and 1 MHz).

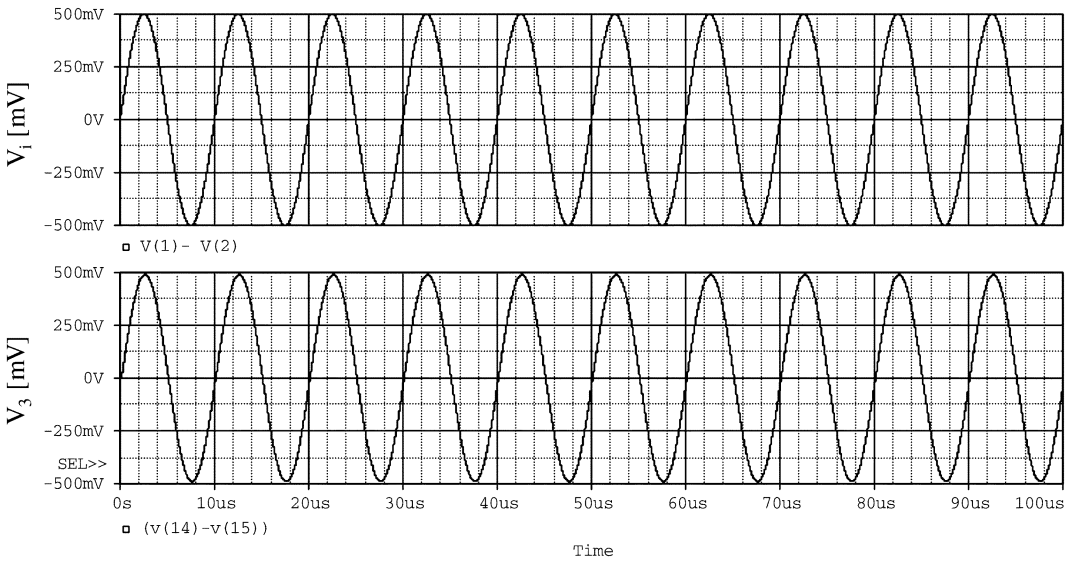

Fig. 17. Time response of the low-pass output when the input signal has 1-V peak-to-peak magnitude and 100-kHz frequency.

the input current in the first output-node of the CDN and receiving it from the input node (i.e., exchanging the input/output nodes). Using (6), the new current equations of the CDN in Fig. 7 will be written as follows:

$$I_{O1} = \frac{Ii}{\alpha} = \frac{2^n Ii}{\left(1 + \sum_{i=0}^{i=n-1} 2^i a_i\right)} \tag{12}$$

$$I_{O2} = \frac{(1-\alpha)}{\alpha} Ii. \tag{13}$$

Hence, the current gain at I_{O1} will be $1/\alpha$ which is greater than, or equal to, one. To realize this idea, an input stage is required to represent low input impedance at the current injection node since the output nodes of the CDN itself are high impedance nodes. Also, an output stage is required to sink (or source) the required current as (12) indicates. Considering Fig. 7, it is worth note that an attractive output current is available at node I_{O2} where the current gain $((1-\alpha)/\alpha)$ can be used for either attenuation (at $\alpha \geq 0.5$) or amplification (at $\alpha \leq 0.5$).

C. Realization of the DCFDCC Using Current Gain Approach

Based on the current gain approach discussed above, DCFDCC of Section III-A can be rearranged as shown in Fig. 8 to exhibit digitally controlled current gain between X- and Z-terminals greater than, or equal to, one. Considering the left half of the circuit of Fig. 8(a), transistors M_1, M_2, M_5, and M_7 represent the input stage of Fig. 7. The required output stage is formed by transistors M_{15}–M_{18} and M_{21}–M_{23} which represent Class-AB push–pull output stage as previously discussed in Section III-A. Transistors M_{19} and M_{20} sense the current of the output stage and transfer it to the output node $Z1-$. Therefore, the complete circuit of the DCFDCC has two fully-differential

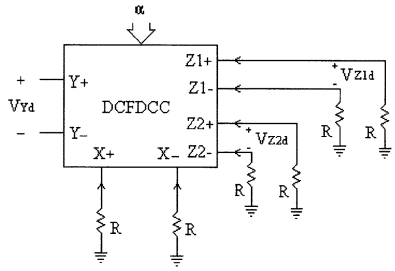

Fig. 18. DCFDCC-based VGA.

Z-terminals and the matrix equation representing its operation is as follows:

$$\begin{pmatrix} V_{Xd} \\ I_{Z1d} \\ I_{Z2d} \\ I_{Yd} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 1 \\ \left(\frac{1}{\alpha}\right) & 0 & 0 & 0 \\ \left(\frac{(1-\alpha)}{\alpha}\right) & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} I_{Xd} \\ V_{Z1d} \\ V_{Z2d} \\ V_{Yd} \end{pmatrix}. \tag{14}$$

The CMOS circuit in Fig. 8(a) has been simulated using PSPICE simulation with the same aspect ratios of the transistors given in Table I. The Y-$Z1$ transfer characteristics are shown in Figs. 9 and 10. In Fig. 9, the differential $Z1$-terminals voltage is shown versus the differential Y input for gain setting of $1, 2, 4, 8$, and $16(\alpha = 1, 1/2, 1/4, 1/8$, and $1/16$, respectively) when all X- and Z-terminals are loaded by equal resistance $R = 10\,\text{k}\Omega$. Fig. 10 shows the ac response of the $Z1$-terminals voltage of the DCFDCC at $\alpha = 1$.

As in the case of the direct realization of the DCFDCC, the time response of the DCFDCC circuit using current gain approach has been simulated by calculating the percentage of the THD at the Z1-terminals when the input signal at Y-terminals had 1-MHz frequency and 1-V peak-to-peak amplitude. For $\alpha = 1$, the percentage of THD was found to be less than 0.5%. Because the output voltage of $Z1$-terminals is inversely proportional to α, $Z1$ voltage level may be distorted when α is decreased (maintaining the same input voltage amplitude). Therefore, the %THD is increased as α decreased for the same input voltage amplitude.

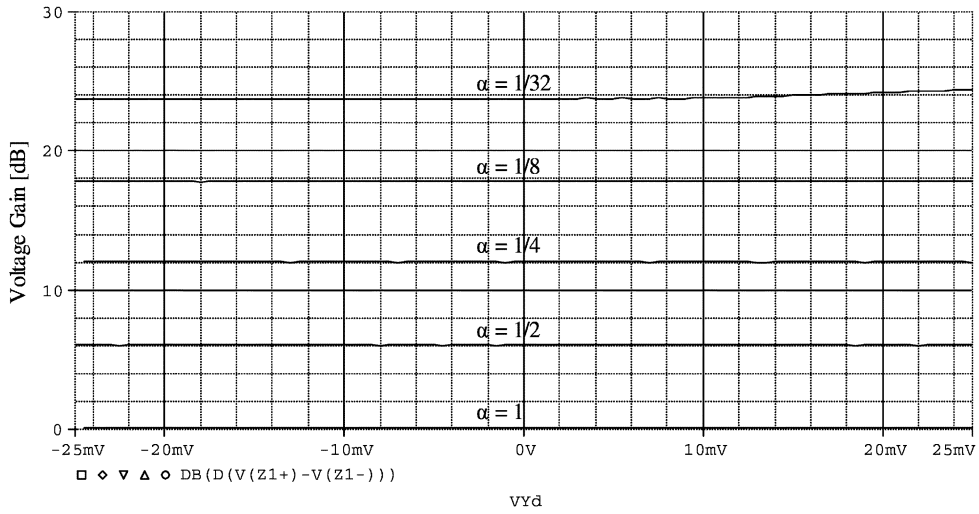

Fig. 19. Simulation of the DCFDCC-based VGA at decibel-linear gain setting of $Z1$-terminals.

IV. Applications

Application of the first approach of the DCFDCC, given in Section III-A, is realizing digitally tuned universal filter. This filter has the advantage of linearly proportional tuned frequency to the digitally controlled parameter α. The filter circuit, analysis, and simulation are presented in the following subsection.

Then, application of the second approach of the DCDCC, given in Section III-C, to realize VGA is presented.

A. Digitally Programmable Universal Active Filter

The single-ended universal-filter presented in [18] can be implemented using DCFDCC in fully differential configuration as shown in Fig. 11. This filter employs five DCFDCC and all-grounded passive elements. This configuration provides several advantages. It has infinite input impedance. All elements are grounded. It realizes high-pass, bandpass, and low-pass differential voltage responses. Also, ω_0 and Q of the filter can be adjusted independently. By direct analysis, the following transfer functions are obtained:

$$\begin{aligned}\frac{V_1}{V_i} &= \frac{\left(\frac{\alpha_1 R}{R_i}\right)s^2}{D(s)}\\ \frac{V_2}{V_i} &= \frac{\left(\frac{\alpha_1\alpha_2 R}{C_1 R_1 R_i}\right)s}{D(s)}\\ \frac{V_3}{V_i} &= \frac{\left(\frac{\alpha_1\alpha_2\alpha_3 R}{C_1 C_2 R_1 R_2 R_i}\right)}{D(s)}\end{aligned} \tag{15}$$

$$D(s) = s^2 + \frac{\alpha_1\alpha_2\alpha_4 R}{C_1 R_1 R_4}s + \frac{\alpha_1\alpha_2\alpha_3\alpha_5 R}{C_1 C_2 R_1 R_2 R_3}. \tag{16}$$

Hence, the ω_0 and Q of the filter are given by

$$\begin{aligned}\omega_0 &= \sqrt{\frac{\alpha_1\alpha_2\alpha_3\alpha_5 R}{C_1 C_2 R_1 R_2 R_3}}\\ Q &= \frac{R_4}{\alpha_4}\sqrt{\frac{\alpha_3\alpha_5 C_1 R_1}{\alpha_1\alpha_2 C_2 R R_2 R_3}}.\end{aligned} \tag{17}$$

Using the following set of design equations:

$$\begin{aligned}&R_i = R_1 = R_2 = R_3 = R\\ &C_1 = C_2 = C\\ &\alpha_1 = \alpha_5 = 1\\ &\alpha_2 = \alpha_3 = \alpha_\omega\\ &\alpha_4 = \alpha_Q.\end{aligned} \tag{18}$$

The ω_0 and $Q$of the filter will be given by

$$\omega_0 = \frac{\alpha_\omega}{CR} \quad Q = \frac{1}{\alpha_Q}\frac{R_4}{R}. \tag{19}$$

As seen from (19), the ω_0 and Q of the filter can be independently programmed digitally using α_ω and α_Q, respectively without distorting each others.

The circuit of Fig. 11 has been simulated using PSPICE simulation with $C = 16$ pF, and $R4 = 0.707R = 5$ kΩ to obtain a maximally flat low-pass (high-pass) response for a dc gain of 1 and with digitally tunable f_o. The frequency response of the low-pass and the high-pass outputs are shown in Figs. 12 and 13, respectively, for different values of the digitally controlled parameter α_ω. Fig. 14 shows the simulated bandpass response of the same circuit for different values of the digitally controlled parameter α_ω while Q is constant at approximately 20. Fig. 15 shows simulation of varying Q using different values of $\alpha_{\rm Q}$ while f_o is constant at 450 kHz. Finally, the time response of the low-pass output of the filter is simulated through Figs. 16 and 17 when $\alpha_\omega = 1$. In Fig. 16, the total harmonic distortion is plotted versus the input signal amplitude (the input frequency is equal to 100 kHz and 1 MHz). It is clear that the filter can handle magnitude of the input signal up to 1-V peak-to-peak with percentage of THD less than 2%. The time response of the low-pass output is shown in Fig. 17 when the input signal has 1-V peak-to-peak amplitude and 100-kHz frequency.

B. Digitally Programmable VGA

The circuit of the VGA is shown in Fig. 18. The VGA employs only one DCFDCC and all-equal resistors. Using direct

analysis and (14), the two output voltages of the VGA, V_{Z1d}, and V_{Z2d}, are given by the following equation:

$$V_{Z1d} = \frac{1}{\alpha} V_{Yd} \tag{20}$$

$$V_{Z2d} = \frac{1-\alpha}{\alpha} V_{Yd}. \tag{21}$$

Therefore, the gain at terminals $Z1$ is greater than, or equal to, one while the gain at terminals $Z2$ may be greater than one $(\alpha \leq 0.5)$ or less than one $(\alpha \geq 0.5)$. The gain-tuning is achieved without any change of the external passive elements.

Fig. 19 shows the simulation of the VGA with decibel-linear gain setting from 0 to 24 dB in 6-dB steps.

V. Conclusion

In this paper, a DCFDCC has been presented. A novel CDN has been proposed to provide a current gain between terminals X and Z of the DCFDCC. The proposed CDN has been used with a fully differential buffer in two configurations. First configuration provides linearly proportional current gain with the digitally controlled parameter of the CDN. The second configuration provides a digitally controlled current gain between terminals X and Z greater than, or equal to, one. Applications of the DCFDCC in realizing second order universal active filter and variable gain amplifier VGA have been given. The proposed blocks and its applications have been confirmed using PSPICE simulation.

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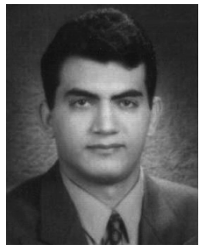

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