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Novel CMOS current conveyor realizations suitable for high-frequency applications

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Abstract

Novel CMOS realizations of the second and the third generation current conveyors based on the use of the current conveyor of the first generation are given. The simulations show that these circuits have an excellent performance and an exceptional bandwidth.

Keywords: Current conveyors; CMOS realizations

1. Introduction

Since its conception, the current conveyor has proven to be an exceptionally versatile current mode building block that can be implemented as several functional circuits, a current amplifier, current integrator and current summer [1–14]. The current conveyor is a three-port network with a describing matrix of the form

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ m & 0 & 0 \\ K & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix} \quad (1)$$

where m determines the nature of the conveyor. If $m = 1$, the conveyor is a first generation current conveyor (CCI), if $m = 0$, the conveyor is a second generation current conveyor (CCII) and if $m = -1$, the conveyor is a third generation current conveyor (CCIII). K determines the polarity of the conveyor. If $K = 1$, the conveyor is a CC+ and if $K = -1$, the conveyor is a CC−.

The purpose of this article is to give new CMOS realizations for the CCII and the CCIII with a wide operating range and excellent frequency response.

The CCI, introduced by Smith and Sedra [1], is shown in Fig. 1. In the circuit shown, a perfect matching between the transistors M1–M2 and M3–M4 is necessary for the proper operation of the circuit [2]. Two local feedback actions across the drains of transistors were responsible for the remarkable performance of this circuit despite its simplicity. The circuit conveys the voltage from Y to X, and the current from X to Y and Z, which offers a simplicity in use and a considerable frequency response giving birth to the current mode approach in the analog circuit design. Several applications were then introduced in the literature [2–9].

The key performance features of current-mode signal processing are wideband capability and a wide dynamic range under low-power operation. To exploit such potentials of current-mode signal processing, the CCII derived from the CCI reported in Ref. [2] (see Fig. 2) is based on the translinear loop and has prototyped many innovative designs that are simple and offer an excellent current following action over a wide bandwidth. However, it suffers from gain inaccuracy due to area mismatch between the input and the output transistors of the current and from the relatively low output resistance at the node Z. Brunn [10] employs a Floating Current Source (FCS) configured as CCII− in order to obtain an accurate current following action which is unaffected by area mismatch. However, this requires matched PMOS and NMOS pairs in the voltage-follower section. Therefore, the voltage following action is inaccurate and there is a DC offset. A very promising technique to implement CCII consists of a feedback-stabilized voltage. This technique employs a high open-loop amplification in order to reduce the DC offset and to reduce the input resistance of the CCII. Several accurate implementations in the literature have followed this op-amp-based architecture [15]. However, these circuits have always suffered from an inaccurate current following action especially at high

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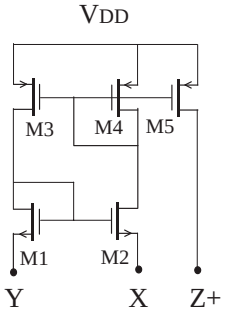


Fig. 1. The circuit configuration of the CCI+.

frequency. The frequency response of these circuits is affected by PMOS current mirrors.

In this article, novel realizations of the current conveyor that has both accurate voltage and current following actions is proposed. The CCI circuit will be used to implement the CCII+ and the CCII−. Then using the same technique, novel realizations for the CCIII+ and the CCIII− will be presented. It will be proved that such an approach gives excellent performance.

2. The new CCII+ circuit realization

The CCII is a versatile analog device which is used to implement many analog signal processing functions [9–14]. Several CMOS realizations of the CCII have been reported in the literature [2–8] Recently, current-mode circuits have received a great interest since they are suitable to operate under low voltage supplies since the current mode substitutes current swings for voltage swings in signal propagation.

The circuit configuration of the proposed CCII+ is shown in Fig. 3(a). It consists mainly of two differential pairs (M1–M3 and M2–M4). It can be easily noted that the transistors (M3–M6) form the CCI introduced in Ref. [2]. All

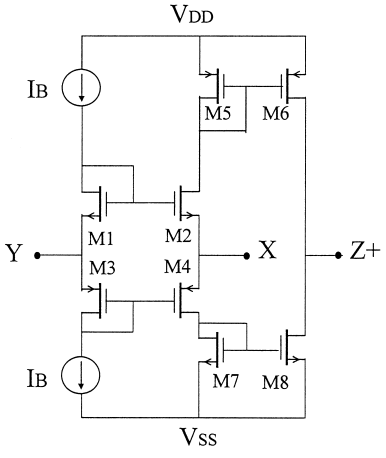


Fig. 2. The basic CCII based on the use of two complementary CCI circuits [2].

transistors are assumed to be operating in the saturation region with their body terminals connected to the proper supply voltage. The action of the proposed CCII is described next. Assuming that the differential pairs (M1, M3 and M2, M4) are perfectly matched, the CCI formed by M3–M6 conveys the voltage from the source of the transistor M4 to the source of the transistor M3 and the current from the transistor M5 to the transistor M6, thus the voltage V_Y applied to the gate of M2 does not effect the current flowing in M4 since the latter follows the current flowing in M3 and since the sources of transistors M1 and M2 have the same voltage (due to the action of the CCI) and carry the same current (since the currents in M3 and M4 are equal), the voltage V_Y is conveyed to the node X successfully. The current coming from X can be reproduced at Z by the action of the current mirror (M7–M8) as shown in Fig. 3(a). It is noted that the arrangement of the circuit can also be seen as two LTPs that are forced to match each other by two local feedback actions across the drains of the transistors M2 and M3. Note that the output current of the Long Tail differential Pair (LTP) transconductor is given by:

$$I_O = \sqrt{K_n I_B}(V_1 - V_2)\sqrt{1 - \frac{K_n(V_1 - V_2)^2}{4I_B}} \tag{2}$$

$$K_n = (\mu_n C_{ox})\left(\frac{W}{L}\right) \tag{3}$$

where $V_2 = V_Y$ (or V_X), K_n is the transconductance parameter, μ_n is the effective carrier mobility, C_{OX} is the gate oxide capacitance per unit area, W is the channel width and L is the channel length.

Hence it is clear that the maximum absolute value of the current delivered from the node X is I_B. This simplifies the design process (provided that the common mode voltage level allows all transistors to operate in the saturation region).

The voltage transfer function is given by:

$$A_v = \frac{1}{1 + \dfrac{1}{1 + g_m^2 r_0 R_L}} \tag{4}$$

where g_m and r_0 are the transconductance of the differential pair and the resistance seen at the drain of transistor M4 (before connecting it to its gate terminal), respectively. R_L is the load resistance connected at the node X (R_L is replaced by R_X when no load is connected to the node X).

The resistance R_X at node X is given by:

$$R_X = \frac{r_0}{1 + g_m^2 r_0^2}. \tag{5}$$

From Eq. (1), it is clear that the open loop gain of the voltage-follower section of the circuit is very high although the use of a small number of transistors and the simple circuit configuration. This is mainly due to the two local feedback actions across the drains of transistors M3 and

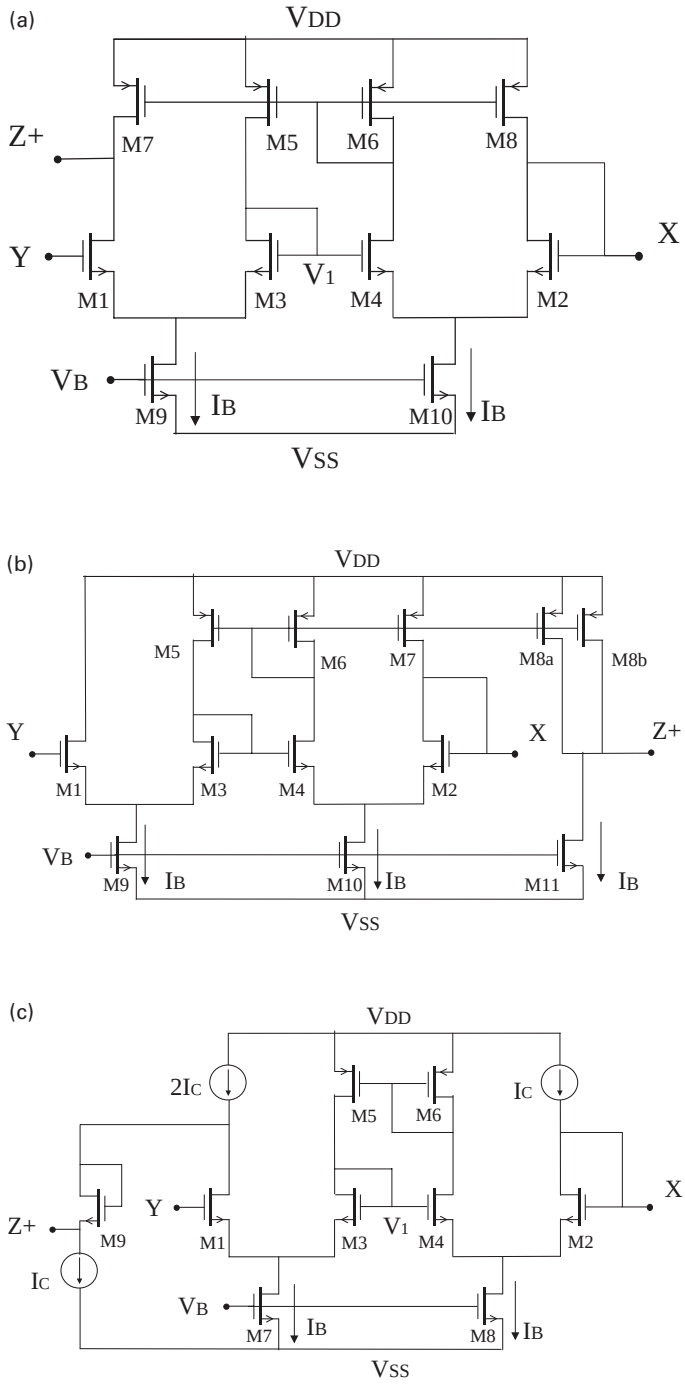


Fig. 3. (a) The circuit configuration of the proposed CCII+. (b) The circuit configuration of the modified CCII+. (c) The improved circuit configuration of the proposed CCII+ for better current following action.

M6, it follows therefore that R_X is very small and V_X follows exactly V_Y [4].

One restriction for the implementation shown in Fig. 3(a) is that, for proper operation, the voltage V_Z must be higher than $(V_Y + V_T)$ which will surely limit the application of the circuit. To overcome this problem, the circuit is modified as shown in Fig. 3(b). By means of the current mirrors M5–M8b, the current I_X is reproduced at the node Z and the voltage V_Z can swing freely over a wide range.

However, the use of PMOS current mirrors results usually in an inaccurate current following action and a relatively limited frequency response which represents a major disadvantage in the majority of the current conveyor circuits ever reported. The FCS proposed by Brunn gives an elegant solution for this problem but only for the CCII− circuits. All the reported circuits implementing the op-amp architecture based CCII+ suffer from this problem. The modified circuit shown in Fig. 3(c) overcomes this problem by solving the

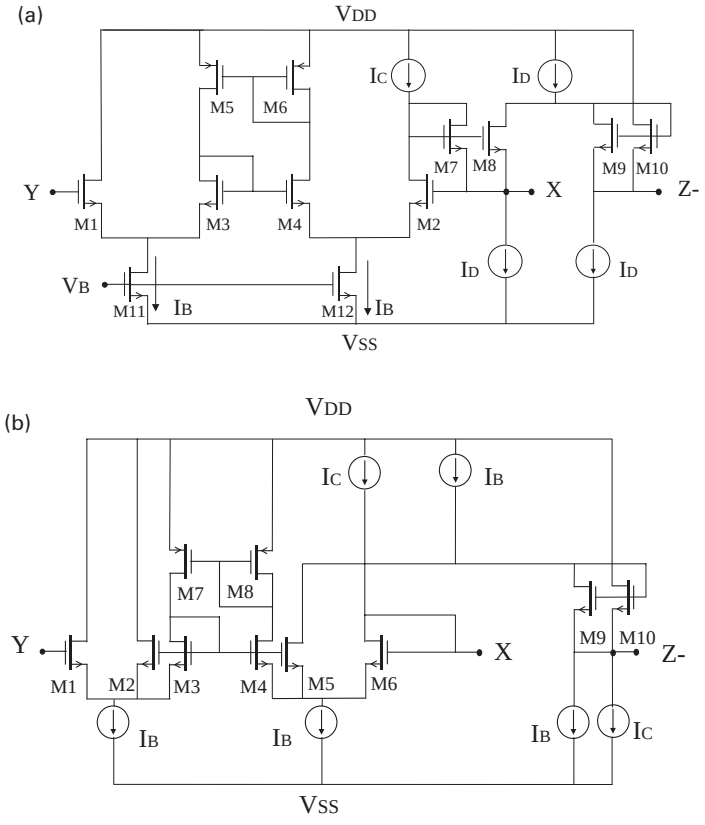


Fig. 4. (a) The circuit configuration of the proposed CCII−. (b) Another proposed circuit configuration of the CCII−.

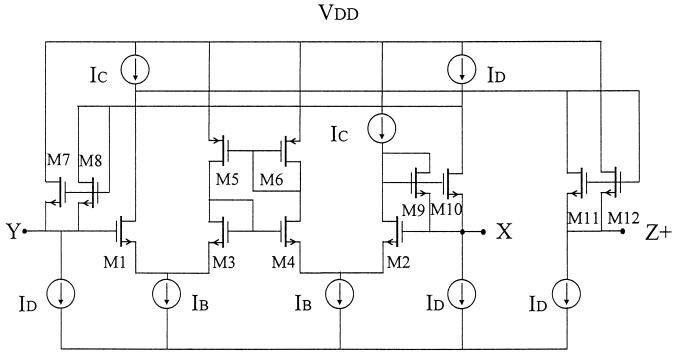


Fig. 5. The circuit configuration of the proposed CCIII+.

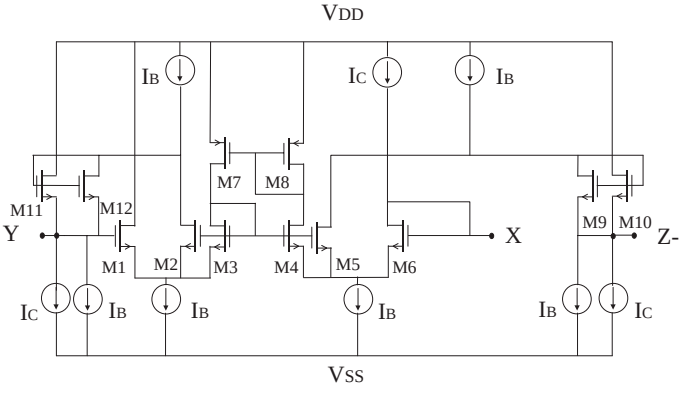


Fig. 6. The circuit configuration of the proposed CCIII−.

Table 1
The *W/L* of the transistors of the circuit shown in Fig. 3(c)

Transistor	Aspect ratio
M1–M4	11/1.5
M5, M6	8/2.5
M7, M8	35/1.5
M9	4/0.5

Table 2
The *W/L* of the transistors of the circuit shown in Fig. 4(a)

Transistor	Aspect ratio
M1–M4	11/1.5
M5, M6	8/2.5
M7, M8, M9, M10	5/3
M11, M12	35/1.5

Table 3
The *W/L* of the transistors of the circuit shown in Fig. 4(b)

Transistor	Aspect ratio
M1–M6	5.5/1.5
M7–M8	8/2
M9–M10	5/3

Table 4
The *W/L* of the transistors of the circuit shown in Fig. 5

Transistor	Aspect ratio
M1–M4	11/1.5
M5, M6	8/2
M7–M12	3/3
M13–M14	35/1.5

Table 5
The *W/L* of the transistors of the circuit shown in Fig. 6

Transistor	Aspect ratio
M1–M6	6.5/1.5
M7, M8	8/2
M9–M12	3/3

limitation of the circuit in Fig. 3(a) by means of a diode-connected transistor M9. The latter is used to prevent M1 from entering in the triode region due to the fluctuations of V_Z while designing amplifiers with gains higher than one. For high-gain amplifiers with wide swing, the number of diode-connected transistors may increase. Despite the use of PMOS current mirrors in the CCI cell (M3–M6), they are not directly used for the current-following action since the current-following action occurs through the voltage-following action, which results in an exceptionally wide frequency response.

3. The new CCII− circuit realizations

The circuit configuration of the proposed CCII− is shown in Fig. 4(a). The analysis of the previous section applies to this circuit since transistors M1–M6 and M11–M12 perform the same action described in the circuit of Fig. 3(a). The negative feedback action from the drain to the gate of M2 is done through the diode-connected transistor M7 which is used as a current sensor in order to reproduce the current I_Z by means of transistors M7–M10 without the need of PMOS current mirrors. Another realization for the CCII− is shown in Fig. 4(b) without the use of this diode-connected transistor that is better in the case of low voltage operation. The current I_Z is reproduced in this circuit by splitting the transistors M3, M4 of Fig. 3(a) into four transistors M2–M5 in Fig. 4(b) (these four transistors can even be chosen to have the same area as the original two transistors). By this way, the current I_Z can be reproduced at Z successfully. It is clear that these circuits give a high flexibility since the information about the current I_X is found in each branch of the two LTPs used in the architecture. These arrangements result in an accurate performance and an excellent frequency response that can be of great use in many applications.

4. The new CCIII circuit realizations

The CCIII is a relatively new current conveyor that was introduced in Ref. [11]. From the describing matrix shown in Eq. (1), it is clear that negative current gain between ports X and Y is its property that seems particularly interesting as it enables the use of the circuit as an integrated floating current-sensing device [12].

The circuit configuration of the proposed CCIII+ is shown in Fig. 5. In this implementation, the same techniques shown in Fig. 3(a) and Fig. 4(a) are used to produce the currents I_Y and I_Z, respectively, from I_X without the need of PMOS current mirrors. Using the same approach used in Fig. 4(b), a realization of the CCIII− can be obtained as shown in Fig. 6. The accurate performance as well as the wide bandwidth of these implementations makes this relatively new building block very attractive to be used in many applications.

5. PSpice simulations

The performances of the proposed current conveyor circuits shown in Figs. 3–6 are simulated using PSpice. Transistors aspect ratios are given in Tables 1–5 and 0.5 μm CMOS process are assumed. Supply voltages are $V_{DD} = -V_{SS} = 3.5$ V and I_B is set to 100 μA.

5.1. Current conveyor characteristics

Fig. 7 shows the voltage following action of the CCII+ at

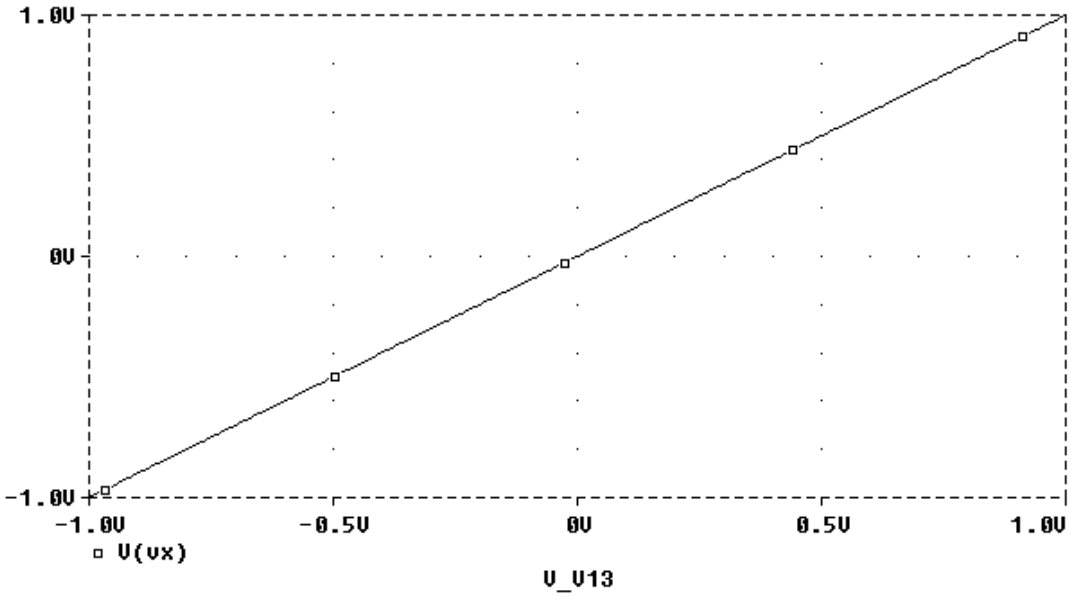


Fig. 7. The DC characteristics at node X for the proposed CCII+.

node X when the input voltage Y is scanned from -1 to 1 V. It can be seen that the offset voltage at node X when Y is grounded is less than 1 mV.

The frequency characteristics of the voltage gain V_X/V_Y when the node X is terminated by $R_X = 10\ \text{k}\Omega$ is shown in Fig. 8. The voltage gain V_Z/V_Y when the node Z is terminated by $R_Z = 10\ \text{k}\Omega$ and $R_Z = 20\ \text{k}\Omega$ are also shown. The resulting frequency characteristics are shown for the cases when the CCII+ of Fig. 3(b) and (c) are used. The bandwidth extends beyond 500 MHz for the case when the CCII+ of Fig. 3(c) is used. It is clear that the bandwidth is not affected by an increase in the gain, which is a main drawback in the op-amp-based architectures. The improvement in the CCII+ current bandwidth due to the absence of the PMOS current mirror is clearly observed. Fig. 9 shows the current I_Y vs. I_X for the CCIII+ circuit. It is shown the negative current-following action between the nodes X and Y is excellent over the wide current range.

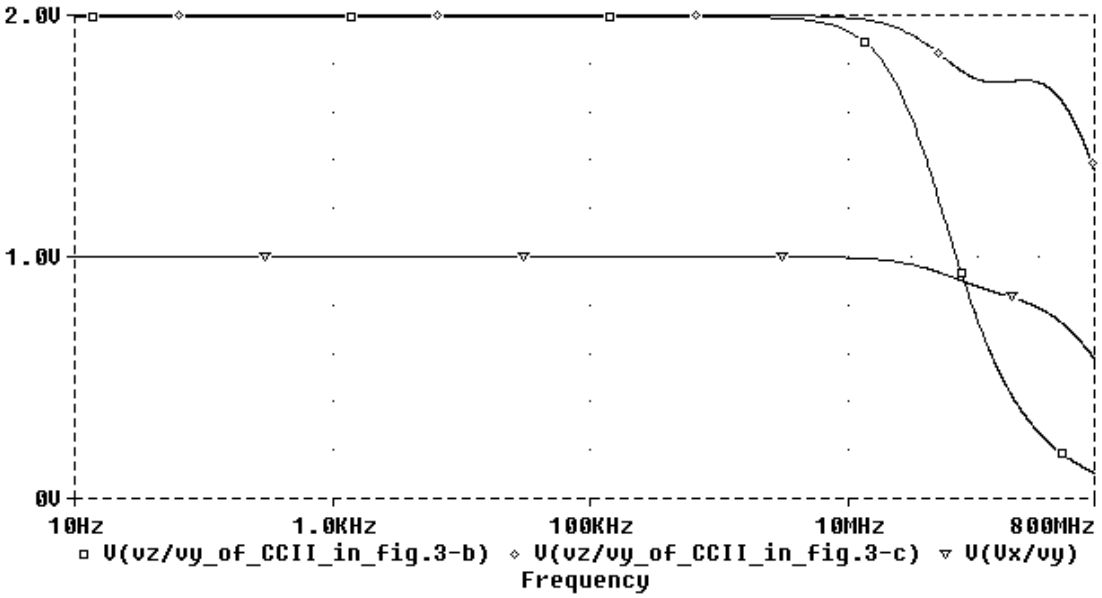


Fig. 8. The frequency characteristics of the voltage transfer functions using CCII+.

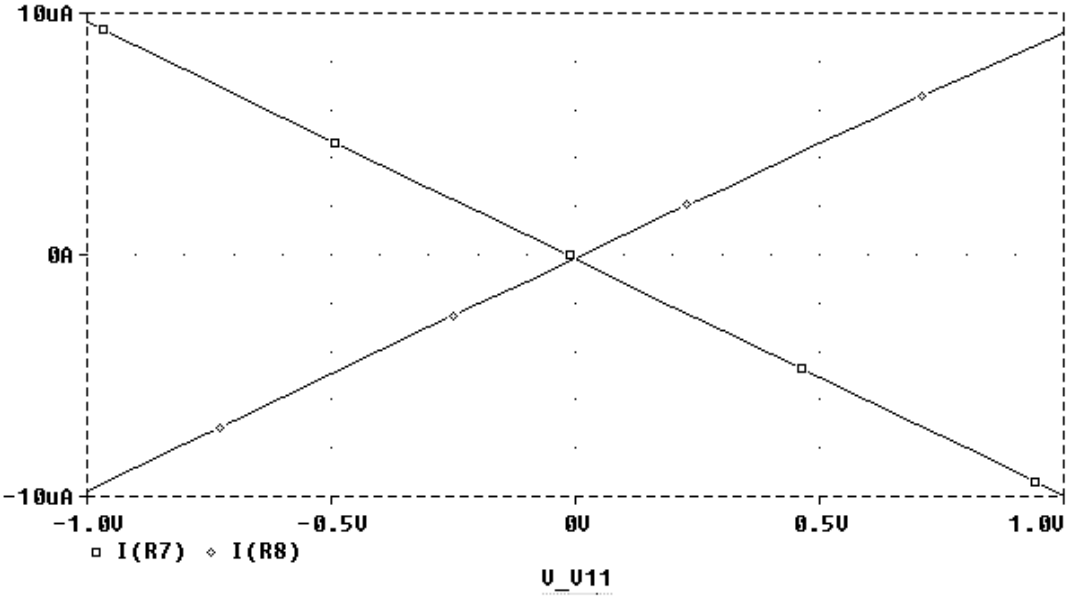


Fig. 9. The currents I_Y versus I_X of the CCIII+.

5.2. Circuit applications

To demonstrate the practicality of the proposed CCII and CCIII in circuit applications, the lowpass filters shown in Fig. 10(a)–(c) are considered [13,14]. The three circuits are equivalent and have the transfer function given by:

$$T(s) = \frac{1}{s^2 C_1 C_2 R_1 R_2 + s(C_1 + C_2)R_2 + 1} \tag{6}$$

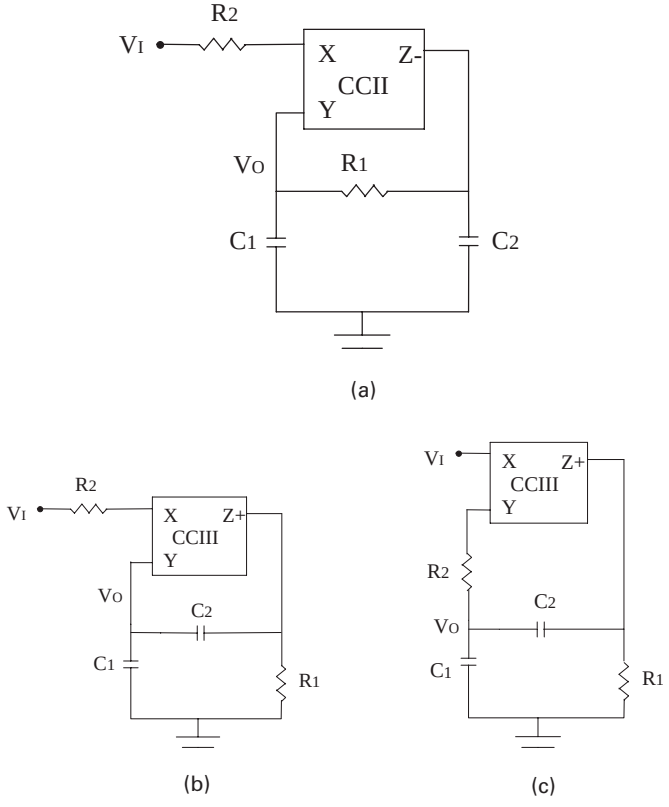
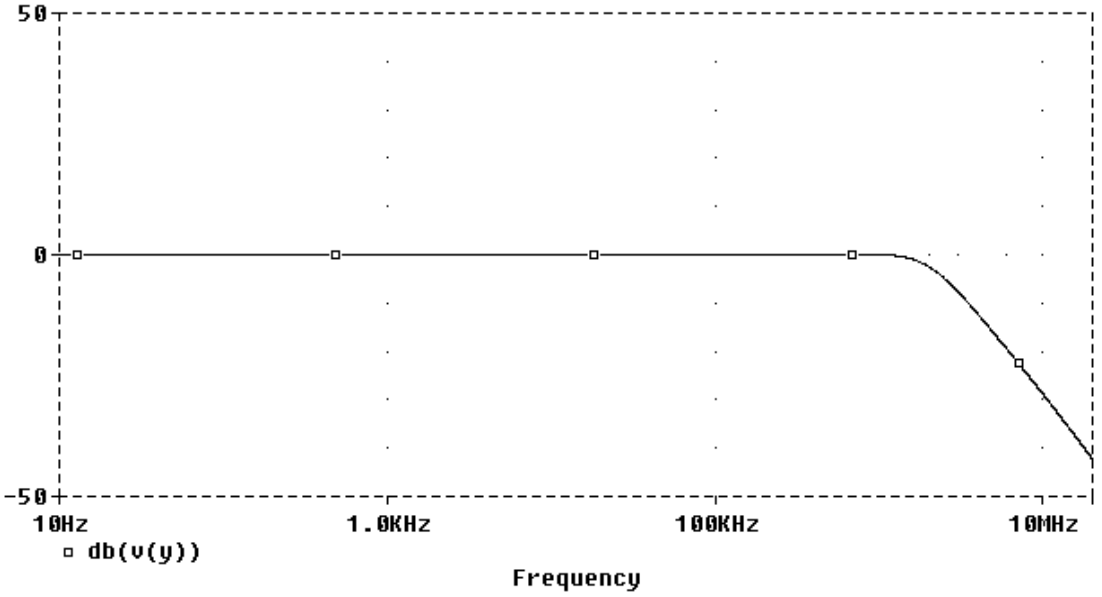
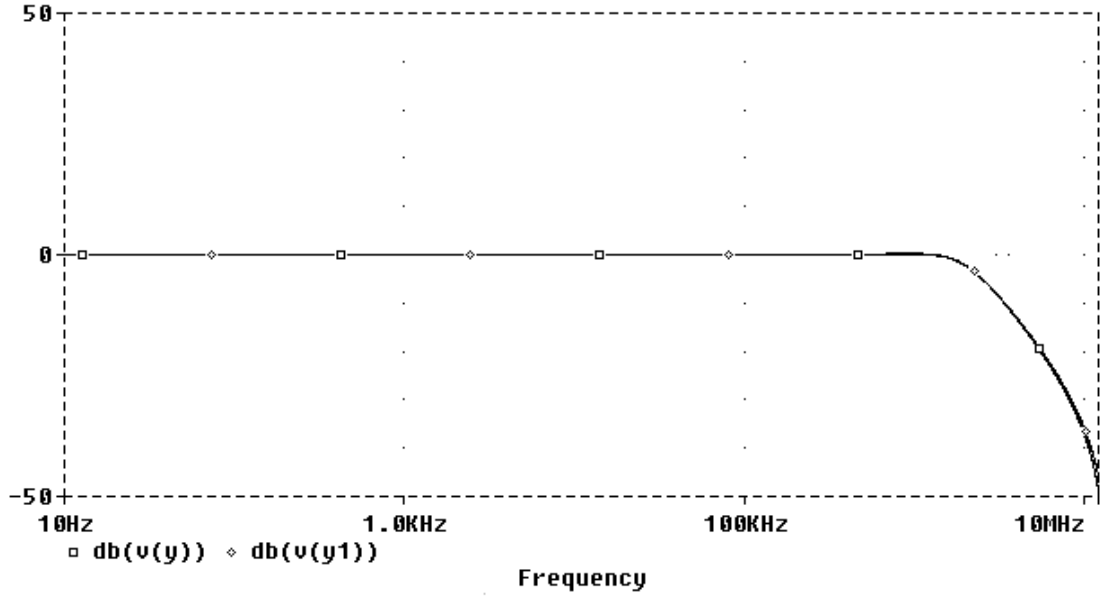


Fig. 10. (a) The low pass filter configuration using CCII−. (b) and (c) Two equivalent low pass filter configurations using CCIII+.



(a)



(b)

Fig. 11. (a) The magnitude characteristics of the CCII− based low pass filter. (b) The magnitude characteristics of the two proposed CCIII+ based low pass filters.

Fig. 11(a) represents the simulated magnitude response of the grounded capacitor lowpass filter of Fig. 10(a), designed for a maximally flat magnitude response and a cut-off frequency of 5 MHz by taking $R_1 = 2.25\,\text{k}\Omega$, $R_2 = 1.125\,\text{k}\Omega$ and $C_1 = C_2 = 20$ pF.

The low-pass filter of Fig. 10(b) and (c) using CCIII+ were also simulated and they provided similar results to that obtained using the lowpass filter of Fig. 10(a) as shown in Fig. 11(b).

6. Conclusion

Novel high accuracy wideband current conveyor circuits based on the current conveyor of the first generation have been presented. Simulation results have shown that their performances are excellent, which makes them very suitable to be used in analog signal processing applications.

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