Hindawi Publishing Corporation
Journal of Electrical and Computer Engineering
Volume 2010, Article ID 108687, 8 pages
doi:10.1155/2010/108687

Review Article

Two Integrator Loop Filters: Generation Using NAM Expansion and Review

Ahmed M. Soliman

Electronics and Communication Engineering Department, Faculty of Engineering, Cairo University, Giza 12613, Egypt

Correspondence should be addressed to Ahmed M. Soliman, asoliman@ieee.org

Received 5 August 2009; Accepted 28 November 2009

Academic Editor: Mohamad Sawan

Systematic synthesis method to generate a family of two integrator loop filters based on nodal admittance matrix (NAM) expansion is given. Eight equivalent circuits are obtained; six of them are new. Each of the generated circuits uses two grounded capacitors and employs two current conveyors (CCII) or two inverting current conveyors (ICCII) or a combination of both. The NAM expansion is also used to generate eight equivalent grounded passive elements two integrator loop filters using differential voltage current conveyor (DVCC); six of them are new. Changing the input port of excitation, two new families of eight unity gain lowpass filter circuits each using two CCII or ICCII or combination of both or two DVCC are obtained.

1. Introduction

Recently, a symbolic framework for systematic synthesis of linear active circuits based on nodal admittance matrix (NAM) expansion was presented in [1, 2]. The matrix expansion process begins by introducing blank rows and columns, representing new internal nodes, in the admittance matrix. Then, nullators and norators are used to move the resulting admittance matrix elements to their final locations, properly describing either floating or grounded passive elements. Thus, the final NAM is obtained including finite elements representing passive circuit components.

In this framework, nullators and norators [3] that ideally describe active elements in the circuit are used. The nullator and norator are pathological elements that possess ideal characteristics and are specified according to the constraints they impose on their terminal voltages and currents. For the nullator $V = I = 0$, while the norator imposes no constraints on its voltage and current. A nullator-norator pair constitutes a universal active two-port network element called the nullor [3], and hence, nullator and norator are also called nullor elements.

Additional pathological elements called mirror elements were introduced in [4, 5] to describe the voltage and current reversing actions. The voltage mirror (VM) is a lossless two-port network element used to represent an ideal voltage reversing action and is described by

$$V_1 = -V_2, \tag{1a}$$

$$I_1 = I_2 = 0. \tag{1b}$$

The current mirror (CM) is a two-port network element used to represent an ideal current reversing action and is described by

$$V_1 \text{ and } V_2 \text{ are arbitrary}, \tag{2a}$$

$$I_1 = I_2 \text{ and they are also arbitrary}. \tag{2b}$$

Very recently the systematic synthesis method based on admittance matrix expansion using nullor elements [1, 2] has been extended to accommodate mirror elements [6–8]. This results in a generalized framework encompassing all pathological elements for ideal description of active elements. Accordingly, more alternative realizations are possible and a wide range of active devices can be used in the synthesis.

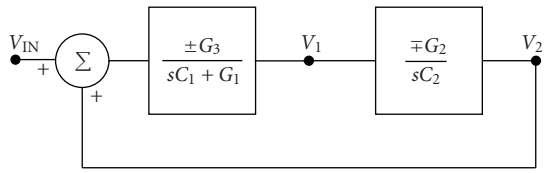


Figure 1: Block diagram of the two integrator loop filters.

In this paper, the conventional systematic synthesis framework using NAM expansion to synthesize two integrator loop filters using CCII [9] or ICCII [5] or combination of both is given. Eight of such two integrator loop filters are generated, six of them are new. An alternative family of eight two integrator loop filters using two DVCCs with very high input impedance and using grounded passive elements is generated; six of them are new. Additional family of eight lowpass circuits using CCII and ICCII is generated by changing input excitation port.

2. NAM Equation of Two Integrator Loop Filters

Figure 1 represents the block diagram representation of the two integrator loop filters with two possible sign polarities of the two integrators.

The denominator $D(s)$ of the transfer function in both cases is given by

$$D(s) = s^2 + \frac{sG_1}{C_1} + \frac{G_2G_3}{C_1C_2}. \tag{3}$$

The block diagram shown in Figure 1 with the upper sign polarities of the two integrators represents a modified simplified form of the Tow Thomas (TT) circuit with the input resistor taken equal to the feedback resistor from V_2 to the inverting input of the first operational amplifier (Op Amp) [10–13]. In the modified TT circuit the inverting lossless integrator and the inverter stage are being exchanged in positions [14, 15].

It is desirable to generate CCII and ICCII grounded capacitor two integrator loop filters having $D(s)$ given by (3).

Consider the block diagram of Figure 1 with the upper signs of the two integrators, and setting $V_{IN} = 0$, the state matrix equation is

$$\begin{bmatrix} sC_1V_1 \\ sC_2V_2 \end{bmatrix} = \begin{bmatrix} -G_1 & G_3 \\ -G_2 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \tag{4}$$

From the above equation and taking the two capacitors to be external elements to the circuit, the admittance matrix defined with ports 1 and 2 as its two ports is obtained as

$$I_i = -sC_iV_i \quad (i = 1, 2). \tag{5}$$

From (4) and (5) the admittance matrix Y is given by

$$Y = \begin{bmatrix} G_1 & -G_3 \\ G_2 & 0 \end{bmatrix}. \tag{6}$$

The two integrator loop filters represented by the above Y matrix are referred to as type-A circuits.

3. Generation of Type-A Conveyor Circuits

Expanding the above matrix by adding a blank third row and third column, and adding a CM between nodes 1 and 3 in order to move $-G_3$ from the 1, 2 position to 3, 2 position, it follows that

$$Y = \left.\begin{bmatrix} G_1 & 0 & 0 \\ G_2 & 0 & 0 \\ 0 & G_3 & 0 \end{bmatrix}\right\}. \tag{7}$$

Adding a nullator between nodes 2 and 3 in order to move G_3 to the diagonal position 3, 3, it follows that

$$Y = \left.\begin{bmatrix} G_1 & \overbrace{0 & 0} \\ G_2 & 0 & 0 \\ 0 & 0 & G_3 \end{bmatrix}\right\}. \tag{8}$$

Next a fourth blank row and column are added and G_2 is moved to the diagonal position 4, 4 by adding a nullator between nodes 1 and 4 and a norator between nodes 2 and 4 as follows:

$$Y = \left.\begin{bmatrix} \overbrace{G_1 & \overbrace{0 & 0} & 0} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & G_3 & 0 \\ 0 & 0 & 0 & G_2 \end{bmatrix}\right\}. \tag{9}$$

The above NAM equation is represented in Figure 2(a) after adding the two capacitors C_1 and C_2 at nodes 1 and 2, respectively.

The circuit is realizable by a CCII+ and a CCII− and the input voltage source is applied to node 5 after disconnecting it from ground.

The NAM can also be expanded as follows:

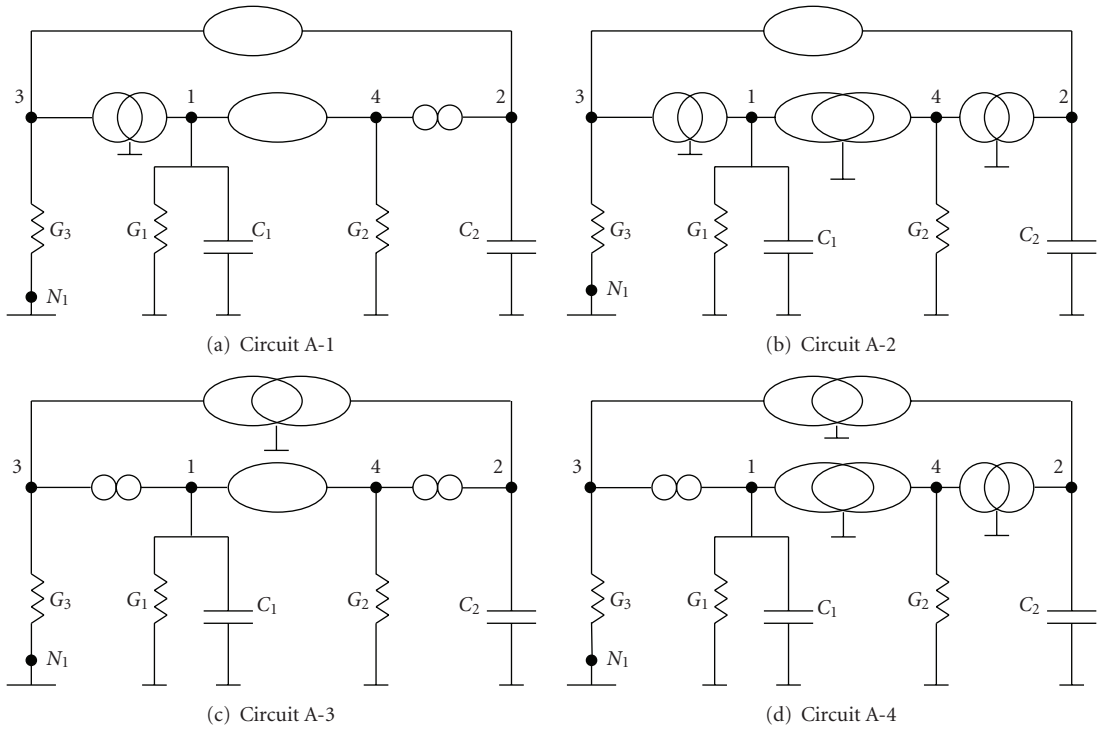
$$Y = \left.\begin{bmatrix} \overbrace{G_1 & \overbrace{0 & 0} & 0} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & G_3 & 0 \\ 0 & 0 & 0 & G_2 \end{bmatrix}\right\}\left.\right\} \tag{10}$$

Figure 2(b) realizes the above equation after adding the two capacitors C_1 and C_2 at nodes 1 and 2, respectively. The circuit is realizable by a CCII+ and an ICCII+.

The NAM can also be expanded as follows:

$$Y = \left.\begin{bmatrix} \overbrace{G_1 & 0 & 0 & 0} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & G_3 & 0 \\ 0 & 0 & 0 & G_2 \end{bmatrix}\right\}\left.\right\} \tag{11}$$

Figure 2(c) realizes the above equation after adding the two capacitors C_1 and C_2 at nodes 1 and 2, respectively. The circuit is realizable by a CCII− and an ICCII−.



(a) Circuit A-1 (b) Circuit A-2

(c) Circuit A-3 (d) Circuit A-4

Figure 2: Realizations of type-A two integrator loop filters.

The NAM can also be expanded as follows:

$$Y = \begin{bmatrix} \overbrace{\begin{bmatrix} G_1 & 0 & 0 & 0 \end{bmatrix}} \\ \begin{bmatrix} 0 & 0 & 0 & 0 \end{bmatrix} \\ \begin{bmatrix} 0 & 0 & G_3 & 0 \end{bmatrix} \\ \begin{bmatrix} 0 & 0 & 0 & G_2 \end{bmatrix} \end{bmatrix} \Bigg\} \tag{12}$$

Figure 2(d) realizes the above equation after adding the two capacitors C_1 and C_2 at nodes 1 and 2, respectively. The circuit is realizable by an ICCII− and an ICCII+.

The circuits can be realized by the generalized current conveyor circuit shown in Figure 3 with the input voltage applied to node N_1.

Table 1 includes the types of the two conveyors used and the polarity of the bandpass and lowpass responses realized in each case. Circuit A-1 has been reported before in [14] and the other three circuits are new.

4. Generation of Type-B Conveyor Circuits

The block diagram shown in Figure 1 with the lower sign polarities of the two integrators represents a simplified form of TT circuit. The simplified TT circuit is obtained by taking the input resistor equal to the feedback resistor from V_2 to the inverting input of the first Op Amp.

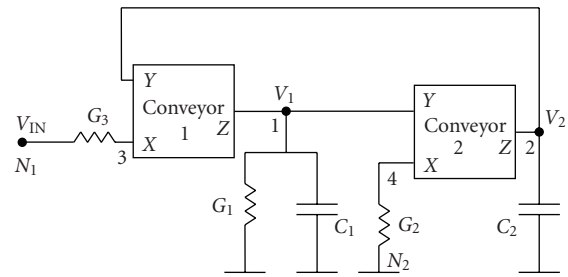


Figure 3: The generalized two conveyor two integrator loop filters.

Consider the block diagram of Figure 1 with the lower signs of the two integrators, and setting $V_{IN} = 0$, the state matrix equation is given by

$$\begin{bmatrix} sC_1V_1 \\ sC_2V_2 \end{bmatrix} = \begin{bmatrix} -G_1 & -G_3 \\ G_2 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \tag{13}$$

From the above equation and taking the two capacitors to be external elements to the circuit, the admittance matrix defined with ports 1 and 2 as its two ports is obtained as

$$Y = \begin{bmatrix} G_1 & G_3 \\ -G_2 & 0 \end{bmatrix}. \tag{14}$$

The above Y matrix can be expanded as in the previous section and will result in four new two integrator loop filters classified as type-B circuits. Adding third blank row and column and connecting a nullator between nodes 2 and 3 and

Table 1: Types of conveyors used in the generalized filter of Figure 3.

Circuit number	Conveyor1	Conveyor2	BP Polarity	LP Polarity	Floating Polarity	Ref.
A-1	CCII+	CCII−	−	+	No	[14]
A-2	CCII+	ICCII+	−	+	No	New
A-3	ICCII−	CCII−	+	−	Yes	New
A-4	ICCII−	ICCII+	+	−	No	New
B-1	CCII−	CCII+	+	+	No	[14]
B-2	CCII−	ICCII−	+	+	Yes	New
B-3	ICCII+	CCII+	−	−	No	New
B-4	ICCII+	ICCII−	−	−	No	New

a norator between nodes 1 and 3 to move G_3 to the diagonal position 3, 3, it follows that

$$Y = \begin{bmatrix} G_1 & \overbrace{0 & 0} \\ -G_2 & 0 & 0 \\ 0 & 0 & G_3 \end{bmatrix}\Bigg]\Bigg]. \tag{15}$$

Next adding a fourth blank row and column and connecting a nullator between nodes 1, 4 and a CM between nodes 2 and 4 to move the $-G_2$ to the diagonal position 4, 4 with positive sign, it follows that

$$Y = \begin{bmatrix} \overbrace{G_1 & \overbrace{0 & 0} & 0} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & G_3 & 0 \\ 0 & 0 & 0 & G_2 \end{bmatrix}\Bigg]\Bigg]\Bigg\} \tag{16}$$

Figure 4(a) represents the realization of the above equation after adding the two capacitors at nodes 1 and 2. The circuit includes two nullators, a norator and a CM which are realizable by a CCII− and a CCII+ as given in Table 1.

Three more new circuits are generated and are shown in Figures 4(b), 4(c), and 4(d) and the types of conveyors used are given in Table 1.

The transfer functions for each of the eight circuits are given by

$$\frac{V_1}{V_{\text{IN}}} = \frac{\pm sG_3/C_1}{s^2 + sG_1/C_1 + G_2G_3/C_1C_2}, \tag{17}$$

$$\frac{V_2}{V_{\text{IN}}} = \frac{\pm G_2G_3/C_1C_2}{s^2 + sG_1/C_1 + G_2G_3/C_1C_2}. \tag{18}$$

The bandpass and lowpass polarities for each circuit are shown in Table 1. From the above equations, therefore

$$\omega o = \sqrt{\frac{G_2G_3}{C_1C_2}}, \qquad Q = \frac{1}{G_1}\sqrt{\frac{C_1G_2G_3}{C_2}}, \tag{19}$$

$$\text{BPGain } (\omega o) = \frac{G_3}{G_1}. \tag{20}$$

The magnitude of the DC gain of the lowpass filter is unity.

5. Two Integrator Loop Filters Using DVCC

5.1. Generation Using Brackets. The NAM expansion introduced in Sections 3 and 4 can also be used to generate high input impedance two-stage two integrator loop filter circuits using the DVCC as the basic building block. The single output differential difference current conveyor (DDCC) has been introduced in [16]. The same circuit defined as the DVCC with a balanced output has also been independently introduced in [17].

The DVCC with a single $Z+$ output is a four-port building block defined by [16, 17]

$$\begin{bmatrix} V_X \\ I_{Y_1} \\ I_{Y_2} \\ I_{Z+} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y_1} \\ V_{Y_2} \\ V_{Z+} \end{bmatrix}. \tag{21}$$

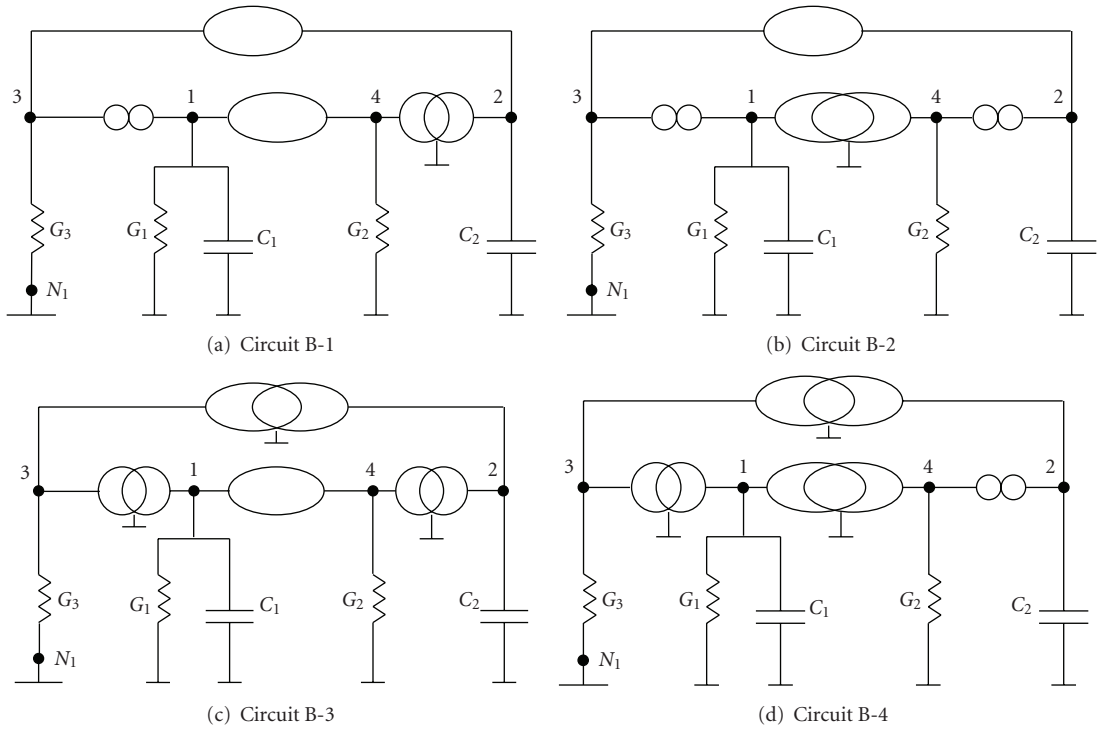
It is seen that the DVCC+ includes CCII+ and ICCII+ as special cases. The DVCC with a single $Z-$ output is defined by [17]

$$\begin{bmatrix} V_X \\ I_{Y_1} \\ I_{Y_2} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y_1} \\ V_{Y_2} \\ V_{Z-} \end{bmatrix}. \tag{22}$$

It is seen that the DVCC− includes CCII− and ICCII− as special cases.

The type-A DVCC-based two integrator loop filter circuits are generated from Figure 2 by following the pathological elements between nodes 2 and 3 to determine the Y input of DVCC-1 and then insert input source at the other Y input of DVCC-1. If the pathological element between nodes 2 and 3 is a nullator, then the feedback to DVCC-1 will be to Y_1 and input source is applied to Y_2 which will represent the additional node in this case. If the pathological element between nodes 2 and 3 is a VM, then the feedback to DVCC-1 will be to Y_2 and input source is applied to Y_1.

The DVCC-2 uses one Y input which is identified from the pathological element between nodes 1 and 4, if it is a nullator, then Y_1 will be input node of DVCC-2 and Y_2 will



(a) Circuit B-1 (b) Circuit B-2

(c) Circuit B-3 (d) Circuit B-4

Figure 4: Realizations of type-B two integrator loop filters.

be grounded; on the other-hand if it is a VM, then Y_2 will be input node of DVCC-2 and Y_1 will be grounded.

The Z polarities will be determined from the pathological elements between nodes 1, 3 and between nodes 2 and 4 as in the case of CCII and ICCII.

For example, in the A-1 circuit a CM is connected between nodes 1 and 3 which implies that $Z+$ polarity for the DVCC-1, and a norator is connected between nodes 2 and 4 which implies that Z-polarity for DVCC-2.

Figure 5 represents the four type-A two DVCC-based two integrator loop filter circuits, and the bandpass and lowpass polarities are given in Table 2. It should be noted that the second stage in each of the four circuits is used as a CCII− or as ICCII+.

Figure 6 represents the four type-B two DVCC-based two integrator loop filter circuits, and the bandpass and lowpass polarities are given in Table 2.

It should be noted that the second stage in each of the four circuits is used as a CCII+ or as ICCII−.

The transfer functions for each of the eight DVCC-based two integrator loop filter circuits are the same as given by (17) to (20).

It should be noted that the block diagram representing the circuits of Figure 5 is the same as that of Figure 1 with upper integrator signs but with a negative sign of the summer input connected to V_{IN}. Similarly the block diagram representing the circuits of Figure 6 is the same as that of Figure 1 with the lower integrator signs but with a negative sign of the summer input connected to V_{IN}.

5.2. Generation Using Brackets and Infinity Parameters. The NAM expansion can also be carried out using both the brackets method and the infinity parameters.

The infinity parameter representation of the DVCC+ is given by [18]

$$\begin{array}{c} \\ X \\ Z+ \end{array} \begin{array}{c} \begin{array}{ccc} X & Y_1 & Y_2 \end{array} \\ \begin{bmatrix} \infty_i & -\infty_i & \infty_i \\ \infty_i & -\infty_i & \infty_i \end{bmatrix} \end{array}. \tag{23}$$

The infinity parameter representation of the DVCC- is given by [18]

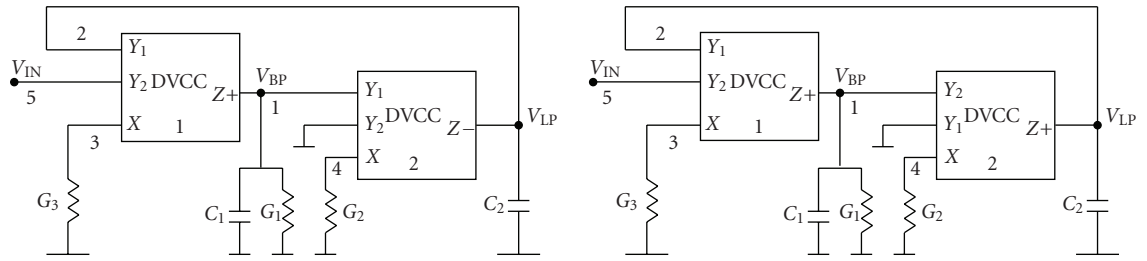
$$\begin{array}{c} \\ X \\ Z- \end{array} \begin{array}{c} \begin{array}{ccc} X & Y_1 & Y_2 \end{array} \\ \begin{bmatrix} \infty_i & -\infty_i & \infty_i \\ -\infty_i & \infty_i & -\infty_i \end{bmatrix} \end{array}. \tag{24}$$

The brackets are used to realize the second stage of the circuit, and the infinity parameters are used next to realize the first stage.

As an example consider the generation of the circuit of Figure 5(a). Starting from (6), add two blank rows and columns and then connect a nullator between nodes 1 and

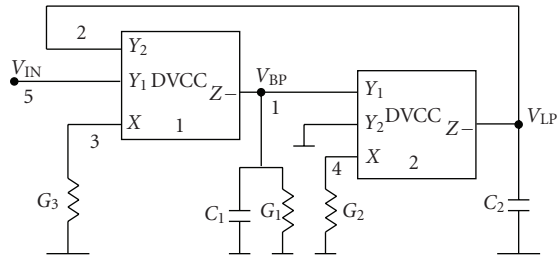
Table 2: Types of the DVCC used in the two integrator loop filters.

Circuit number	DVCC1	DVCC2	BP Polarity	LP Polarity	Floating Polarity	Ref.
A-1	DVCC+	DVCC−	−	+	No	New
A-2	DVCC+	DVCC+	−	+	No	New
A-3	DVCC−	DVCC−	−	+	Yes	New
A-4	DVCC−	DVCC+	−	+	No	[13]
B-1	DVCC−	DVCC+	+	+	No	New
B-2	DVCC−	DVCC−	+	+	Yes	New
B-3	DVCC+	DVCC+	+	+	No	[16]
B-4	DVCC+	DVCC−	+	+	No	New

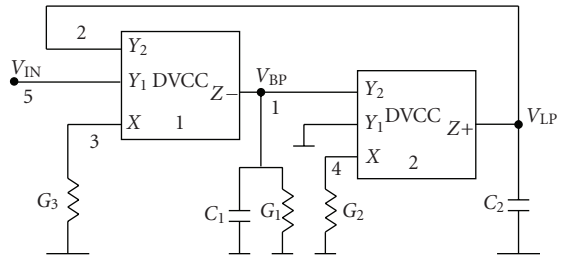


(a) Circuit A-1 using two DVCC

(b) Circuit A-2 using two DVCC

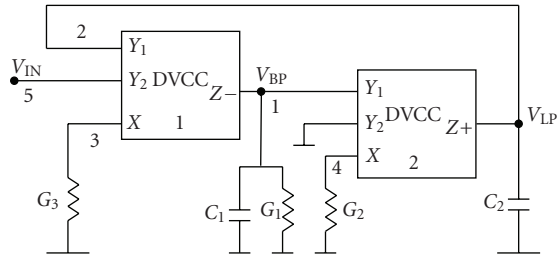


(c) Circuit A-3 using two DVCC

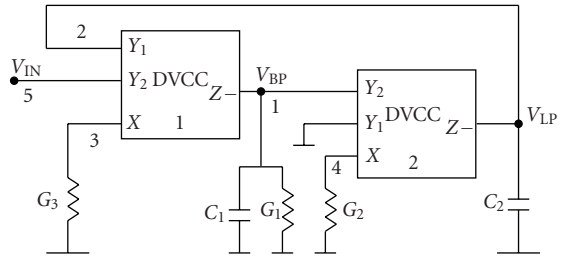


(d) Circuit A-4 using two DVCC

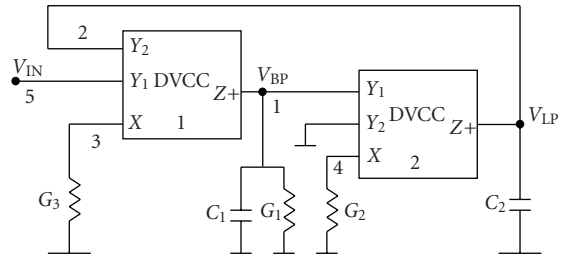
Figure 5



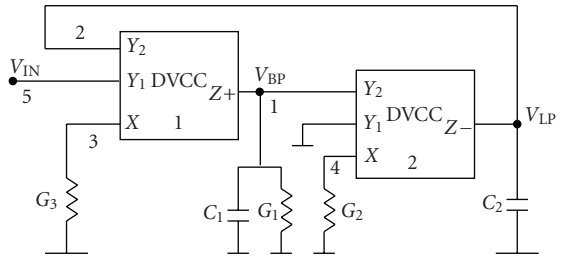
(a) Circuit B-1 using two DVCC



(b) Circuit B-2 using two DVC



(c) Circuit B-3 using two DVCC



(d) Circuit B-4 using two DVCC

Figure 6

4 and a norator between nodes 2 and 4 to move G_2 to the diagonal position 4, 4 as follows:

$$Y = \begin{bmatrix} \overbrace{\begin{matrix} G_1 & -G_3 & 0 & 0 \end{matrix}} \\ \begin{matrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & G_2 \end{matrix} \end{bmatrix}. \tag{25}$$

The nullator and norator added to move G_2 are realizable by a CCII− which is realized by the DVCC− with port X connected to G_2 and with port Y_2 connected to ground. Next G_1 is connected to port 1 and the capacitors C_1 to node 1 and C_2 are connected to nodes 1 and 2, respectively.

To realize a high-input impedance circuit there must be a row with a zero current; adding a fifth blank row and column results in the following expanded NAM:

$$Y = \begin{bmatrix} \overbrace{\begin{matrix} G_1 & -G_3 - \infty_1 & \infty_1 & 0 & \infty_1 \end{matrix}} \\ \begin{matrix} 0 & 0 & 0 & 0 & 0 \\ 0 & -\infty_1 & \infty_1 & 0 & \infty_1 \\ 0 & 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{matrix} \end{bmatrix}. \tag{26}$$

The infinity parameters moves G_3 in a two-step move to the diagonal 3, 3 position as follows:

$$Y = \begin{bmatrix} \overbrace{\begin{matrix} G_1 & -\infty_1 & \infty_1 & 0 & \infty_1 \end{matrix}} \\ \begin{matrix} 0 & 0 & 0 & 0 & 0 \\ 0 & -\infty_1 & G_3 + \infty_1 & 0 & \infty_1 \\ 0 & 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{matrix} \end{bmatrix}. \tag{27}$$

The infinity parameters realizes the first stage DVCC+ with its Y_2 as the high-input impedance node 5, Y_1 as node 2 and X as node 3 connected to G_3 to ground as shown in Figure 5(a).

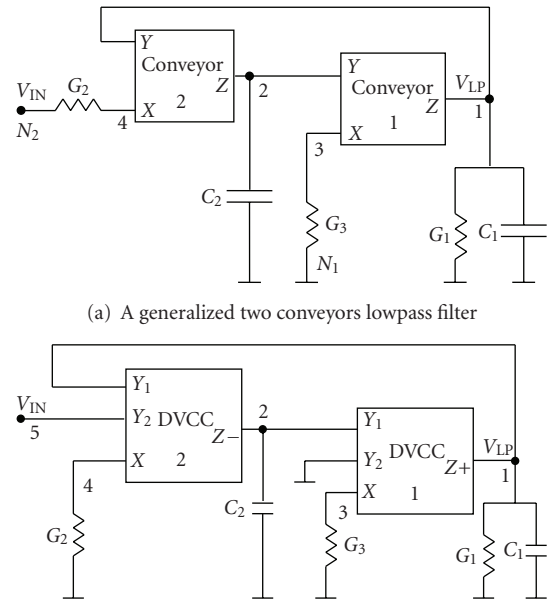
As a second example consider the generation of the circuit of Figure 5(c).

The NAM can also be expanded as follows:

$$Y = \begin{bmatrix} \overbrace{\begin{matrix} G_1 & \infty_1 & \infty_1 & 0 & -\infty_1 \end{matrix}} \\ \begin{matrix} 0 & 0 & 0 & 0 & 0 \\ 0 & -\infty_1 & G_3 - \infty_1 & 0 & \infty_1 \\ 0 & 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{matrix} \end{bmatrix}. \tag{28}$$

The above equation is realized as shown in Figure 5(c) with the first stage as a DVCC− with its Y_1 as the high-input impedance node 5 and connected to input, Y_2 as node 2, and X as node 3 connected to G_3 to ground; the second stage is the same as in Figure 5(a).

The type-B DVCC-based two integrator loop filter circuits can also be generated following the same rules mentioned above.



(a) A generalized two conveyors lowpass filter

(b) Lowpass filter obtained from circuit A-1 in Figure 5(a)

Figure 7

Table 3: Types of conveyors used in the lowpass filter of Figure 7(a).

Circuit Number	Conveyor1	Conveyor2	LP Polarity	Floating Polarity
1	CCII+	CCII−	+	No
2	CCII+	ICCII+	−	No
3	ICCII−	CCII−	+	Yes
4	ICCII−	ICCII+	−	No
5	CCII−	CCII+	+	No
6	CCII−	ICCII−	−	Yes
7	ICCII+	CCII+	+	No
8	ICCII+	ICCII−	−	No

6. Generation of New Lowpass Filters

A new family of lowpass filters can be generated from the generalized circuit of Figure 3 by injecting the input voltage at node N_2 and grounding node N_1. The generalized lowpass filter circuit is shown in Figure 7(a) with the same transfer function as given by (18). The magnitude of the DC gain is unity and the polarity is given in Table 3. Eight new alternative realizations that belong to Figure 7(a) according to the conveyors used are given in Table 3. The generalized block diagram of this family of lowpass filters is obtained from Figure 1 by interchanging the two integrator positions [12, 19]. It is worth noting that the circuit numbers three and six have a floating property.

Similarly eight new DVCC-based lowpass filter circuits can be generated from Figures 5 and 6 by changing the input port of excitation. Figure 7(b) represents the new noninverting lowpass filter circuit generated from Figure 5(a). similarly the other seven lowpass filter circuits can be obtained.

7. Conclusions

The NAM expansion method using nullor elements and pathological mirrors is used to generate eight grounded capacitor conveyor-based two integrator loop filter circuits. Additional eight grounded passive elements DVCC-based two integrator loop filter circuits are given; six of them are new. The CCII circuits A-1 and B-1 have been reported before in [14]. It is worth noting that circuits A-3 and B-2 have a floating property as shown in Table 1.

Additional eight grounded passive elements DVCC-based circuits are given; six of them are new. It is worth noting that circuits A-3 and B-2 have a floating property as shown in Table 2.

It is worth noting that all the reported circuits whether employing CCII and ICCII combinations or using two DVCC can be compensated by subtracting the values of the parasitic resistances R_{X1} and R_{X2} from the design values of R_3 and R_2, respectively. Similarly the parasitic capacitances can be compensated by subtracting the values of C_{Z1} and C_{Z2} from the design values of C_1 and C_2, respectively.

A similar circuit to B-1 using two CCII with different port excitations was given in [20]. Other realizations of two integrator loop filter circuits using ICCII were given in [21]. The importance of the VM-CM pathological elements [22] in the generation of the six new two integrator loop filter circuits using CCII or ICCII or combination of both or two DVCC is demonstrated in this review paper.

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