

MOS Realization of the Double-Scroll-Like Chaotic Equation

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Abstract—This brief presents a new chaotic circuit based on Gm - C integrators. The circuit realizes the double-scroll-like chaotic equation presented in [1], [2]. The mentioned equation describes double-scroll dynamics with a simple mathematical model. The proposed circuit uses a current-mode technique that is suitable for integrated circuit implementation and high-frequency operation using low supply voltage. A general block diagram is presented based on Gm - C integrators. Its realization using MOS transistors and three grounded capacitors is also given. Simulation results to demonstrate the practicality of the circuit are included.

Index Terms—Chaos, CMOS circuits, Gm - C integrators.

I. INTRODUCTION

Chaos as a science has become an important topic in the world of nonlinear dynamics. Applications of chaos have become one of the necessities of our every day life, especially since these applications show commercial benefits [3]–[5]. One of the new applications introduced in this field is the chaotic oscillator. The design of chaotic oscillators has been a subject of increasing interest during the past few years [6]–[10]. The double-scroll attractor is considered one of the most famous chaotic attractors that have appeared until now. Many designs of chaotic oscillators were introduced starting from the use of a coil in Chua's [6] circuit to the use of large blocks such as operational amplifiers [7]–[9]. In both cases, the fabrication area was very large, so if it would be possible to use as few components as possible in the design of these chaotic oscillators—without giving up functionality, therefore, it is possible to minimize the fabrication area. These designs were also dependent on the use of floating capacitors and the use of high supply voltage, which is not preferred in fabrication due to the demanding need for portable devices in our world today.

There are many simple chaotic equations proposed in [1], [2], [11], and [12]. The advantages of these systems appear in: simplicity, absence of multiplication terms, ease to scale over a wide range of frequencies and ease of construction. The proposed circuit is based on the use of MOS transistors and three grounded capacitors for realizing the double-scroll-like chaotic equation, which is the minimum requirement for the implementation of a chaotic oscillator. This circuit operates on low-supply voltage (± 1.5 V). In this sense, the proposed circuit overcomes the previously mentioned drawbacks and can be used in the manufacturing of portable devices. The general block diagram presented in this brief gives a chance for any reader to use any transconductor (Gm) to realize such equations.

II. STRUCTURED DESIGN OF THE EQUATION

The simple equation modeling the double-scroll-like dynamics [1], [2], is described by following differential equation:

$$\ddot{\ddot{X}} = a \left[\ddot{X} + \dot{X} + X - f(X) \right] \quad (1a)$$

where

$$f(X) = \text{sgn}(X) = \begin{cases} 1 & X \geq 0 \\ -1 & X < 0 \end{cases}. \quad (1b)$$

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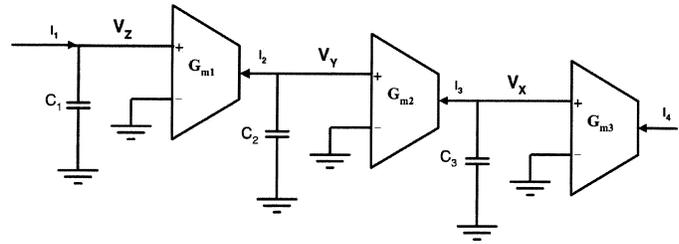


Fig. 1. The block diagram of the cascaded current integrators.

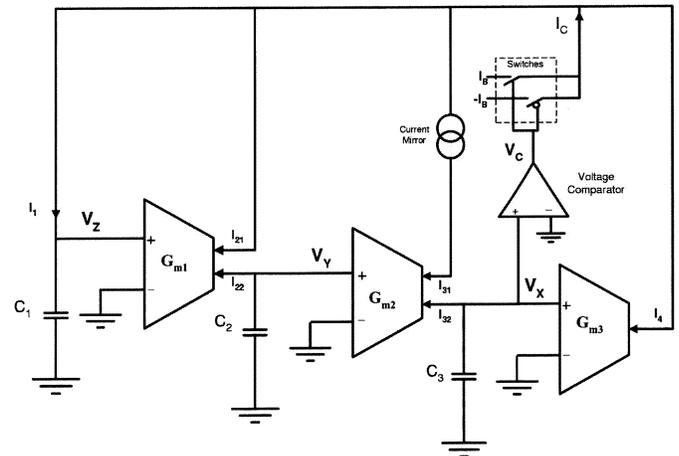


Fig. 2. The general block diagram of the double-scroll chaotic equation.

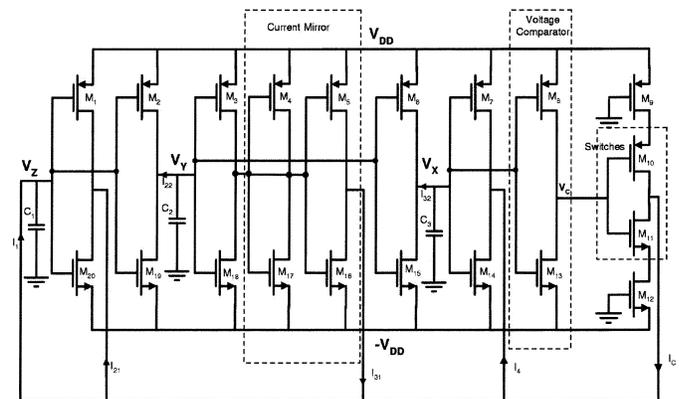


Fig. 3. The MOS circuit realization of the double-scroll chaotic equation.

The double-scroll dynamics are observed when the value of the parameter a lies [2] between 0.48 and 0.98.

A. Transformations

In the pure mathematical domain, equations are dimensionless. But the case is different in the electronic domain, where finding an implementation of an equation requires the use of quantities having dimensions. Hence, the signal X can be transformed into a voltage signal V_X through the equation $X = V_X/V_R$, where V_R is a reference voltage and the dimensionless time τ can be transformed into the time t with dimension [s] through the relation $d/d\tau = (C/g)(d/dt)$, where g is a transconductance and C is a capacitor.

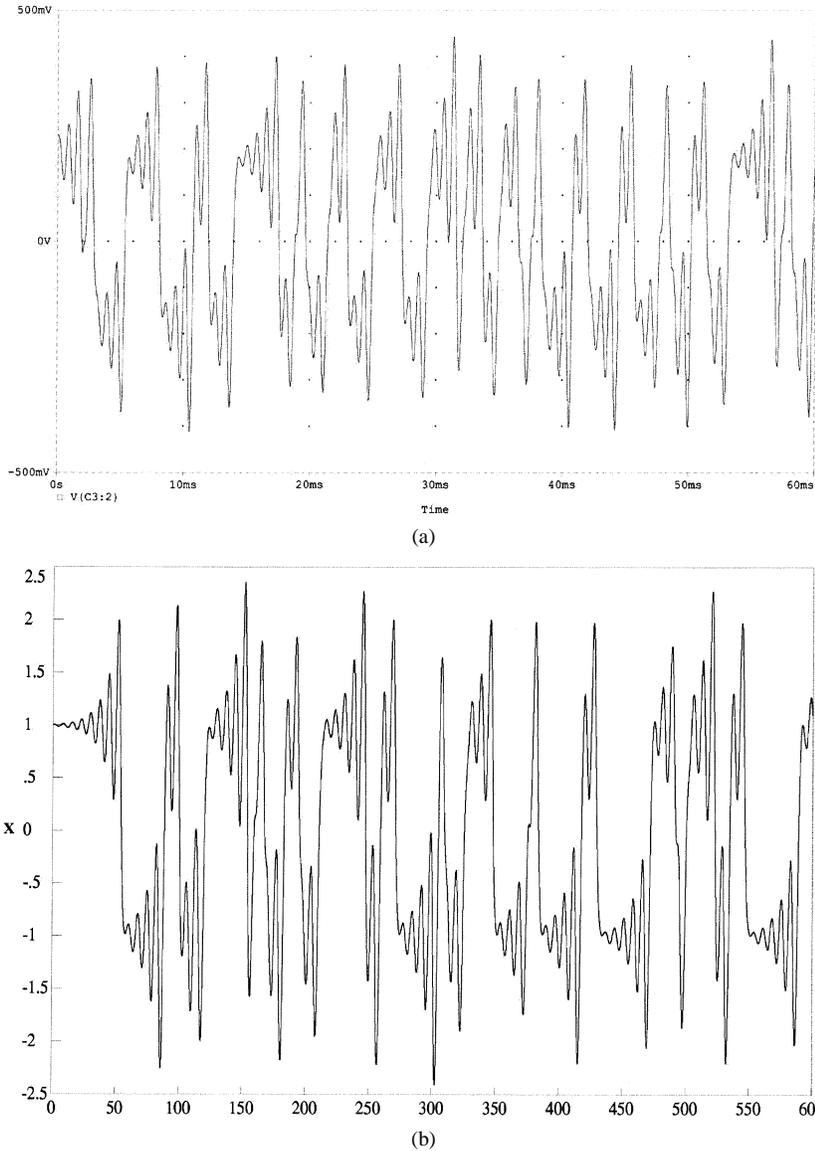


Fig. 4. (a) The PSpice simulation result of V_X . (b) The numerical solution result of X .

Applying the above transformations, the resulting voltage mode third-order differential equation becomes

$$\ddot{V}_x = -a \frac{g}{C} \ddot{V}_x - a \left(\frac{g}{C}\right)^2 \dot{V}_x - a \left(\frac{g}{C}\right)^3 V_x + a V_R \left(\frac{g}{C}\right)^3 f(V_x) \tag{2a}$$

$$f(V_x) = \begin{cases} 1 & V_x \geq 0 \\ -1 & V_x < 0. \end{cases} \tag{2b}$$

B. Cascaded Current Integrators

The general block diagram of the chaotic oscillator is presented based on transconductors, thus imposing the need for the use of a current integrator in the design of the circuit. A simple current integrator is based on the use of $Gm-C$ as shown in Fig. 1

$$I_4 = g_3 V_x \tag{3}$$

$$I_3 = g_2 V_y = -C_3 \dot{V}_x \tag{4}$$

$$\dot{V}_x = -\frac{g_2}{C_3} V_y \tag{5}$$

$$I_2 = g_1 \dot{V}_z = -C_2 \dot{V}_y \tag{6}$$

$$\ddot{V}_x = \left(\frac{g_2}{C_3}\right) \left(\frac{g_1}{C_2}\right) V_z \tag{7}$$

$$I_1 = C_1 \dot{V}_z \tag{8}$$

if $g_1 = g_2 = g_3 = g$ and $C_1 = C/a$ and $C_2 = C_3 = C$.
From (7) and (8), the following is obtained:

$$\ddot{V}_x = a \frac{g^2}{C^3} I_1. \tag{9}$$

Substituting from (5) and (7) in (2a) we therefore get

$$\ddot{V}_x = a \frac{g^3}{C^3} [-V_z + V_y - V_x + V_R f(V_x)]. \tag{10}$$

By comparing (9) and (10), I_1 can fulfill (10) through the following relation:

$$I_1 = -gV_z + gV_y - gV_x + I_C = -I_2 + I_3 - I_4 + I_C \tag{11}$$

$$I_C = \begin{cases} I_B, & V_x \geq 0 \\ -I_B, & V_x < 0 \end{cases} \tag{12}$$

where $I_B = g V_R$ (bias current). The general block diagram of the overall circuit is shown in Fig. 2, which consists of three transduc-

TABLE I
TRANSISTOR ASPECT RATIOS OF THE DOUBLE-SCROLL MOS CIRCUIT

Transistor	Aspect ratio (W/L) ($\mu\text{m}/\mu\text{m}$)
M ₁ , M ₂ , M ₃ , M ₄ , M ₅ , M ₆ , M ₇	20/15
M ₁₄ , M ₁₅ , M ₁₆ , M ₁₇ , M ₁₈ , M ₁₉ , M ₂₀	20/65.5
M ₈	40/15
M ₉	15/15
M ₁₀	40/1
M ₁₁	40/4.5
M ₁₂	15/65.5
M ₁₃	40/65.5

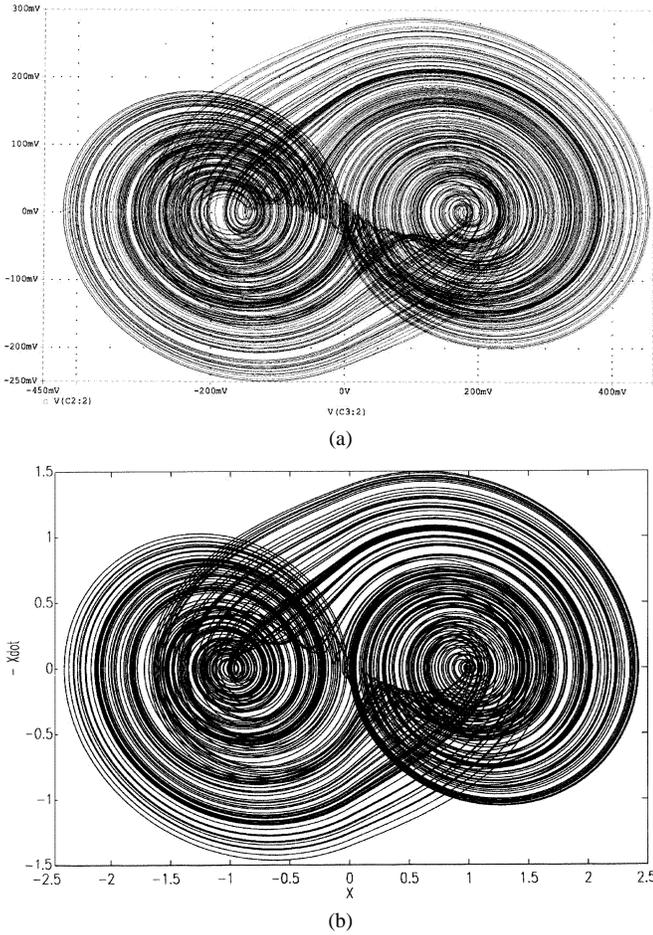


Fig. 5. (a) V_X - V_Y projection of PSpice simulation. (b) $X - (-\dot{X})$ projection of the numerical solution.

tors, a simple current mirror, three grounded capacitors and a voltage comparator.

C. Circuit Implementation

To verify the general block diagram, a typical transconductor (consisting of only two transistors such as M₁ and M₂₀ as shown in Fig. 3) is used as the G_m in Fig. 2. The output current is given by $I_o = g_m V_Z$, where $g_m = 2 K (V_{DD} - V_t)$. This relation was obtained assuming balanced supply voltages and approximately equal threshold voltages, where $V_{tn} = |V_{tp}| = 0.6$ V from the data obtained from Mietec 0.5- μm technology. Therefore $K_1 = K_{20} = K$ which is the condition for proper operation of the G_m . The current mirroring is achieved

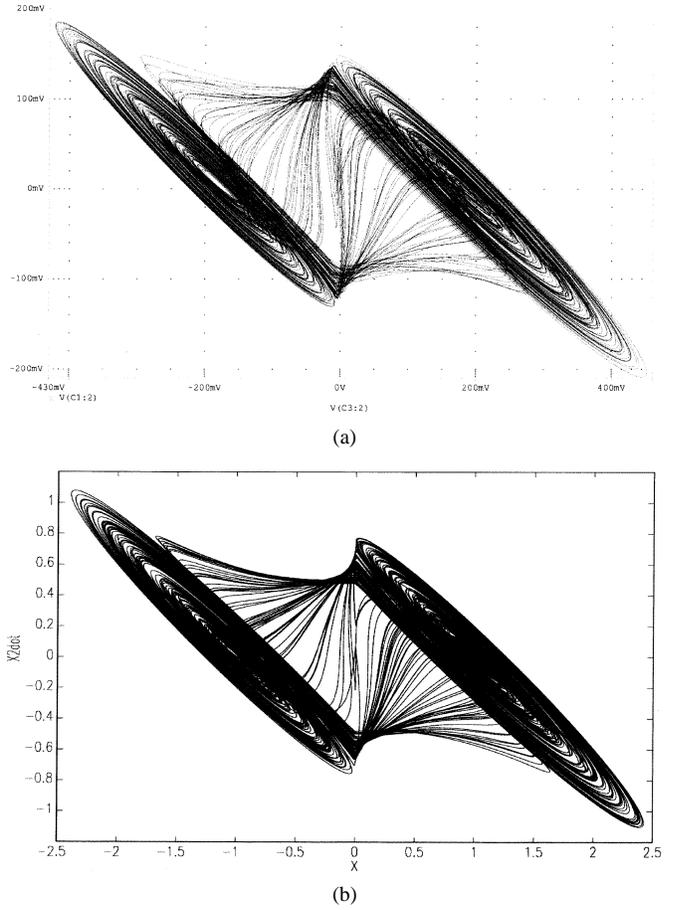


Fig. 6. (a) V_X - V_Z projection of PSpice simulation. (b) $X - \ddot{X}$ projection of the numerical solution.

through transistors M₄, M₅, M₁₆ and M₁₇. The voltage comparison can be achieved through transistors M₈ and M₁₃ (simple inverter) taking advantage of the high gain in the transition region of the inverter. Since the bias current is constant, we can generate it through transistors M₉ and M₁₂ (both of them operate in the saturation region) by connecting the ground and the supply V_{DD} to the gate terminals and changing the aspect ratios of the transistors, the appropriate current value can be obtained. Finally, M₁₀ and M₁₁ operate as switches depending on the value of V_c (output of the comparator). The overall circuit realization consists of MOS transistors and three grounded capacitors is shown in Fig. 3. The circuit operates on low supply voltage (± 1.5 V), which is suitable for portable devices.

III. SIMULATION RESULTS

The proposed MOS circuit is simulated using PSpice simulation and using the model of Mietec 0.5- μm technology. Also the numerical analysis is done using fourth-order Runge-Kutta method with step size of 0.05 [2]. The transistors aspect ratios are stated in Table I using $C_2 = C_3 = C = 6$ nF and $C_1 = C/0.6 = 10$ nF (taking $a = 0.6$). The PSpice simulation of V_X for the proposed circuit is shown in Fig. 4(a) and the numerical solution of the mathematical equation X is shown in Fig. 4(b). The small differences between the two figures are related to their sensitivity to the initial condition, but they have the same dynamics as will be shown. The V_X - V_Y projection for the circuit realization and $X - (-\dot{X})$ numerical result are shown in Fig. 5(a) and (b), respectively [negative sign due to (4)]. The V_X - V_Z for both the

circuit realization and $\ddot{X}-\ddot{X}$ numerical results are shown in Fig. 6(a) and (b), respectively. The frequency response of the proposed circuit can be varied over a wide range from 1 Hz up to 100 MHz by changing either g or C or both of them.

IV. CONCLUSION

This brief presents the general block diagram of the double-scroll-like chaotic equation based on $Gm-C$ integrators using current-mode techniques and operating on low supply voltage. The implementation of such general block diagram using a typical transistor to form the overall circuit based only on MOS transistors and three grounded capacitors, is given. The effectiveness of the proposed circuit is demonstrated through PSpice simulations.

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Globally Exponential Stability of Neural Networks With Variable Delays

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Abstract—In this brief, the conditions ensuring existence, uniqueness, and globally exponential stability of the equilibrium point of neural networks with variable delays are studied. Applying idea of vector Liapunov function, and M -matrix theory, the sufficient conditions for global exponential stability of neural networks are obtained.

Index Terms—Asymptotically stability, globally exponential stability, neural network, variable delays.

I. INTRODUCTION

Neural networks have been extensively studied in the past decade and successfully applied to signal-processing systems, especially in static image treatment, and to solve nonlinear algebraic equations. Such applications rely on the existence of equilibrium points or of a unique equilibrium point, and qualitative properties of stability [1], [2]. In hardware implementation, time delays occur due to finite switching speeds of the amplifiers and communication time. Time delays may lead to an oscillation and furthermore, to instability of networks. Therefore, the study of stability of neural networks with delay is practically required. The conditions ensuring the asymptotic stability of neural networks are given in [3]–[13]. Exponential stability is discussed in [14]–[16]. Delays of systems in [3]–[16] are fixed, i.e., independent on time. The stability of neural networks with variable time delays is discussed in [17]–[19], but exponential stability is not discussed.

In this brief, we study the globally exponential stability of neural networks with variable delays described by the delayed differential equations

$$\frac{du_i(t)}{dt} = -d_i u_i(t) + \sum_{j=1}^n [a_{ij} g_j(u_j(t)) + b_{ij} g_j(u_j(t - \tau_{ij}(t)))] + J_i, \quad i = 1, 2, \dots, n \quad (1)$$

where u_i is the state of neuron i , $i = 1, 2, \dots, n$, and n is the number of neurons; $A = (a_{ij})_{n \times n}$, $B = (b_{ij})_{n \times n}$ are connection matrices, $J = (J_1, J_2, \dots, J_n)^T$ is the constant input vector. $g(u) = (g_1(u_1), g_2(u_2), \dots, g_n(u_n))^T$ is the activation function of the neurons, and $D = \text{diag}(d_1, d_2, \dots, d_n) > 0$. The variable delays $\tau_{ij}(t)$ ($i, j = 1, 2, \dots, n$) are bounded functions, i.e., $0 \leq \tau_{ij}(t) \leq \tau$. The initial conditions of (1) are of the form $u_i(s) = \phi_i(s)$, $-\tau \leq s \leq 0$, where ϕ_i is bounded and continuous on $[-\tau, 0]$.

We consider the activation functions of the neurons satisfying the following assumptions.

Assumption 1: For each $j \in \{1, 2, \dots, n\}$, $g_j: R \rightarrow R$ is globally Lipschitz with Lipschitz constant L_j , i.e.

$$|g_j(u_j) - g_j(v_j)| \leq L_j |u_j - v_j|$$

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