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# HISTORY AND PROGRESS OF THE TOW–THOMAS BIQUADRATIC FILTER PART II: OTRA, CCII, AND DVCC REALIZATIONS

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The realization of the Tow–Thomas (TT) circuit using the Operational Transresistance Amplifier (OTRA) is reviewed. The circuit employs two OTRA, and all passive elements are floating as the original Tow–Thomas circuit. The Current Conveyor (CCII) TT circuits are reviewed next. The progress in the realization of the TT circuit using CCII is demonstrated clearly by summarizing eight different circuits. One of the circuits has the advantage of very high input impedance using all grounded resistors and capacitors. The Differential Voltage Current Conveyor (DVCC) as the active building block in realizing the TT circuit is also considered. Finally, current mode TT circuits using balanced output CCII are summarized. Top Spice (level 49), simulation results using technology SCN 05 feature size 0.5 $\mu$m from MOSIS vendor: AGILENT are included to demonstrate the magnitude and phase frequency response of the TT circuits. Additional simulation results for the total power dissipation, total harmonic distortion, intermodulation IM3, input and output referred noise spectral densities are also included for comparison purposes.

*Keywords*: Tow–Thomas circuit; operational transresistance amplifier; current conveyor.

## 1. Introduction

This section reviews the history of Tow–Thomas (TT)[1,2] second-order filter.[3] Two alternative generation methods of the TT filter were discussed in Ref. 3. The first is a generation method from the second-order passive RLC filter and the second is from the multiple feedbacks inverting low-pass filter using a single op amp. Several forms of the circuit using op amps were briefly reviewed in Ref. 3. Passive and active compensation methods to improve the circuit performance for high $Q$ designs were also given in Ref. 3. It was concluded that the classical TT circuit using op amps has frequency limitations due to the finite gain-bandwidth of the op amps.

In this paper the progress in the realization of the TT circuit using the operational transresistance amplifiers,[4] current conveyors,[5] and the differential voltage

current conveyor[6] is reviewed. The current mode version of the TT circuit using balanced output current conveyors is also reviewed.

In Sec. 2 a brief summary of the TT circuit using three op amps together with the basic circuit equations and its block diagram is given.

## 2. The Tow–Thomas Circuit Using Op Amps

The TT circuit using three op amps is shown in Fig. 1(a). The transfer functions are given by

$$\frac{V_{BP}}{V_I} = \frac{\frac{-s}{C_1 R_4}}{s^2 + \frac{s}{C_1 R_1} + \frac{1}{C_1 C_2 R_2 R_3}}, \tag{1}$$

$$\frac{V_{LP1}}{V_I} = \frac{\frac{1}{C_1 C_2 R_2 R_4}}{s^2 + \frac{s}{C_1 R_1} + \frac{1}{C_1 C_2 R_2 R_3}}, \tag{2a}$$

$$\frac{V_{LP2}}{V_I} = \frac{\frac{-1}{C_1 C_2 R_2 R_4}}{s^2 + \frac{s}{C_1 R_1} + \frac{1}{C_1 C_2 R_2 R_3}}. \tag{2b}$$

From the above equations, it is seen that $\omega_0$ and $Q$ are given by

$$\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_2 R_3}}, \quad Q = R_1 \sqrt{\frac{C_1}{C_2 R_2 R_3}}. \tag{3}$$

Taking $C_1 = C_2 = C, R_2 = R_3 = R$, the design equations for a specified $\omega_0$ and $Q$ are given by

$$R_1 = QR, \quad R = \frac{1}{\omega_0 C}. \tag{4}$$

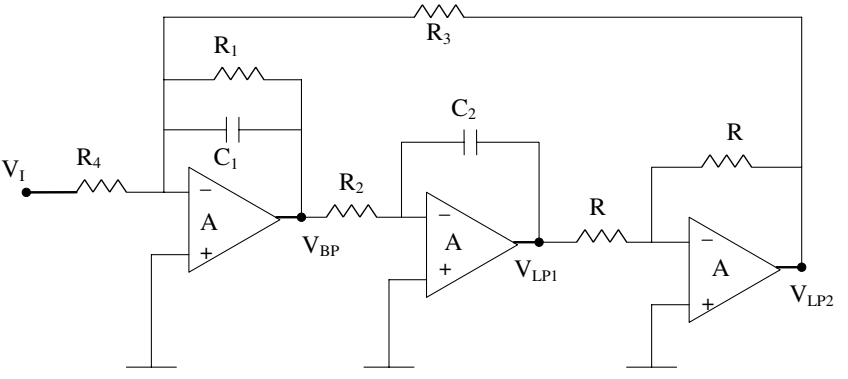


Fig. 1(a). The TT circuit.[1,2]

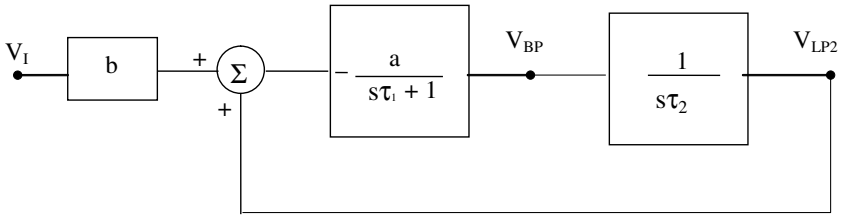


Fig. 1(b). Block diagram of the TT circuit.[3]

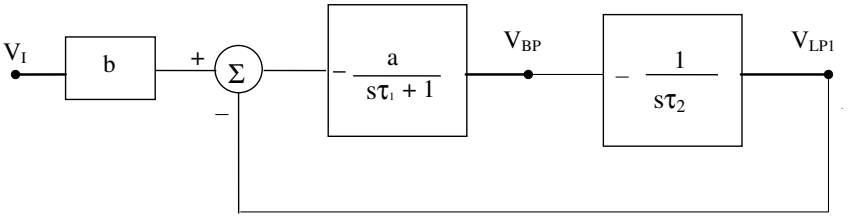


Fig. 1(c). Equivalent block diagram of the TT circuit.

Figure 1(b) represents the equivalent block diagram of the circuit shown in Fig. 1(a), where the parameters $\tau_1$, $\tau_2$, $a$, and $b$, are related to the circuit components by

$$\tau_1 = C_1 R_1\,, \quad \tau_2 = C_2 R_2\,, \quad a = \frac{R_1}{R_3}\,, \quad b = \frac{R_3}{R_4}\,. \tag{5}$$

Figure 1(c) represents an equivalent block diagram of the TT circuit. Although the TT circuit has very low passive sensitivities to all passive circuit components, it suffers from a rather drastic $Q$-factor enhancement effect due to the op amp finite gain bandwidth.

In this paper, several circuits realizing the TT biquad using other active devices[4–18] in order to avoid the op amp limitations and achieve higher frequencies are reviewed.

## 3. The Active Building Blocks

A brief summary of the three active building blocks that are considered in this paper is given next.

The operational transresistance amplifier (OTRA) is a three-terminal analog building block shown symbolically in Fig. 2(a) and is defined by the following equations

$$V_+ = 0\,, \quad V_- = 0 \quad \text{and} \quad V_0 = R_m(I_1 - I_2)\,. \tag{6}$$

$R_m$ is the transresistance gain. Ideally, $R_m$ approaches infinity, and on applying negative feedback it will force the two currents $I_1$ and $I_2$ to be equal. Both the input

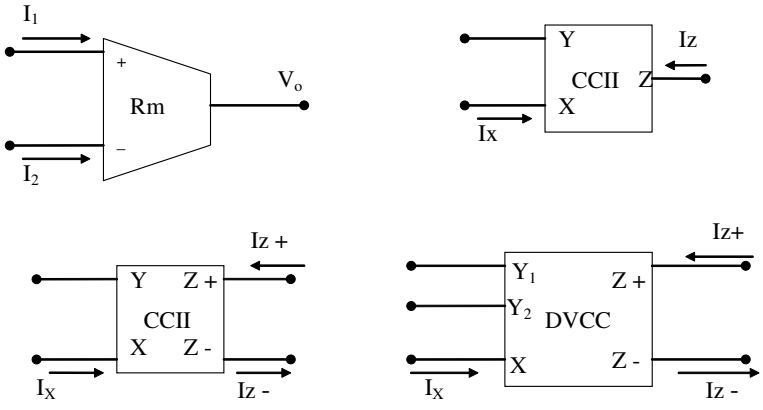


Fig. 2(a). Symbols of the OTRA, CCII, balanced output CCII, and DVCC.

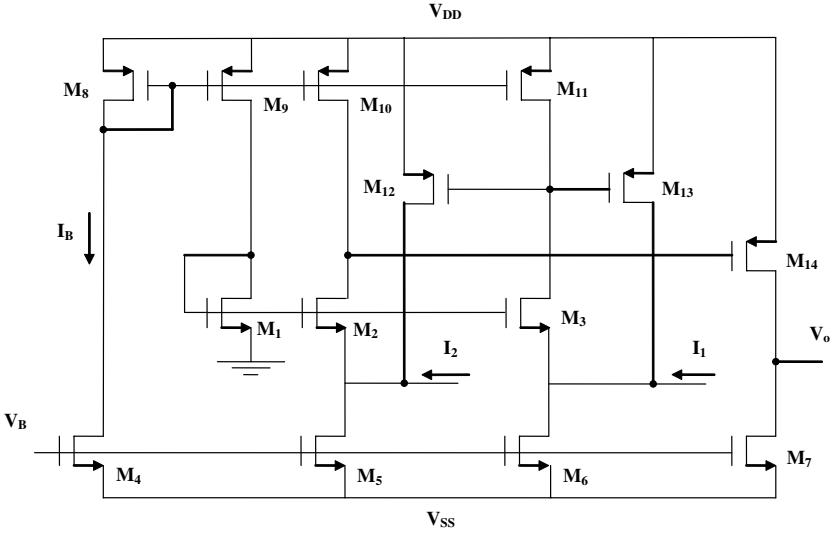


Fig. 2(b). CMOS circuit of the OTRA given in Ref. 4.

and output terminals are characterized by low impedance. The input terminals are virtually grounded leading to circuits that are insensitive to stray capacitances.

The OTRA is not slew limited as the op amp. It does not suffer from gain-bandwidth product like the op amp circuits.

A CMOS circuit realizing the OTRA is shown in Fig. 2(b),[4] with the transistor aspect ratios given in Table 1(a).

The second building block used in this paper is the second generation current conveyor CCII[18] which is shown symbolically in Fig. 2(a) and is defined by

$$I_Y = 0\,, \quad V_X = V_Y\,, \quad I_Z = \pm I_X\,. \tag{7}$$

Table 1(a). Aspect ratios of OTRA of Fig. 2(b).

| MOS transistors | W($\mu$m)/L($\mu$m) |
|---|---|
| $M_1, M_2, M_3$ | 100/2.5 |
| $M_4, M_7$ | 10/2.5 |
| $M_5, M_6$ | 30/2.5 |
| $M_8, M_9, M_{10}, M_{11}$ | 50/2.5 |
| $M_{12}, M_{13}$ | 100/2.5 |
| $M_{14}$ | 50/0.5 |

Table 1(b). Aspect ratios of the CCII+ circuit of Fig. 2(c).

| MOS transistors | W($\mu$m)/L($\mu$m) |
|---|---|
| $M_1, M_2$ | 20/1 |
| $M_3$ | 50/2.5 |
| $M_4, M_5$ | 60/2.5 |
| $M_6$ | 40/0.5 |
| $M_7, M_8$ | 20/2.5 |
| $M_9, M_{10}$ | 20/2.5 |

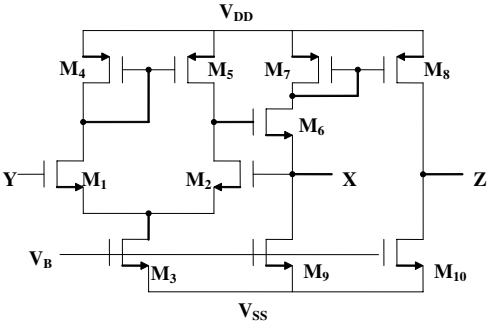


Fig. 2(c). CMOS circuit of the CCII given in Ref. 5.

The positive sign applies to CCII+ and the negative sign applies to CCII−. A CMOS circuit realizing the CCII+ is shown in Fig. 2(c),[5] with the transistor aspect ratios given in Table 1(b).

The balanced output CCII is shown symbolically in Fig. 2(a) and is defined by the following equations (assuming all currents to be inwards):

$$I_Y = 0\,, \quad V_X = V_Y\,, \quad I_{Z^+} = I_X\,, \quad I_{Z^-} = -I_X\,. \tag{8}$$

For $I_X$ flowing inward to the $X$ port, the actual directions for $I_{Z^+}$ and $I_{Z^-}$ are inward and outward from the $Z$ ports, as shown in Fig. 2(a).

The differential voltage current conveyor (DVCC) having balanced output currents has been introduced in Ref. 6. In Ref. 14 the DVCC has also been independently introduced and defined as a single output differential difference current conveyor.

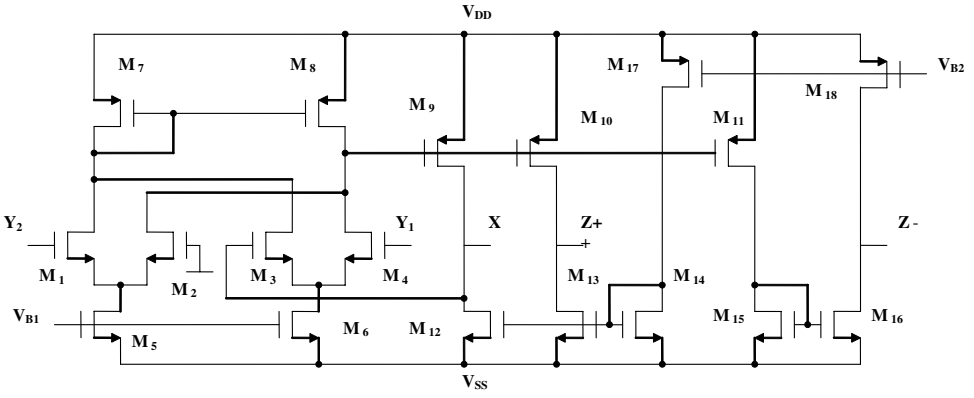


Fig. 2(d). CMOS circuit of the DVCC given in Ref. 6.

Table 1(c). Aspect ratios of the DVCC circuit of Fig. 2(d).

| MOS transistors | W($\mu$m )/L($\mu$m) |
|---|---|
| $M_1, M_2, M_3, M_4$ | 25/0.5 |
| $M_5, M_6$ | 8/0.5 |
| $M_7$ and $M_8$ | 10/0.5 |
| $M_{12}, M_{13}, M_{14}, M_{15}, M_{16}$ | 20/2.5 |
| $M_9, M_{10}, M_{11}, M_{17}, M_{18}$ | 40/2 |

The DVCC is a five-port building block shown symbolically in Fig. 2(a) and is defined by (assuming all currents to be inwards):

$$I_{Y_1} = I_{Y_2} = 0\,, \quad V_X = V_{Y_1} - V_{Y_2}\,, \quad I_{Z^+} = I_X\,, \quad I_{Z^-} = -I_X\,. \tag{9}$$

A CMOS circuit realizing the balanced output DVCC is shown in Fig. 2(d),[6] with the transistor aspect ratios given in Table 1(c).

The modified TT circuit using these active building blocks is given in the following sections of the paper.

## 4. Tow–Thomas Circuit Using OTRA

Figure 3(a) represents the TT circuit using OTRA,[7] the circuit realizes an inverting band-pass noninverting low-pass using two OTRA, four floating resistors, and two floating capacitors as summarized in Table 2. It is equivalent to the TT circuit, and Eqs. (1) and (2a) apply to this circuit. The block diagram of this circuit is the same as Fig. 1(c). It has independent control on $Q$ by $R_1$ and independent control on the gain by $R_4$. For a specified band-pass center frequency gain $T(\omega_0)$, the design equation for $R_4$ is given by

$$R_4 = \frac{R_1}{T(\omega_0)}\,. \tag{10}$$

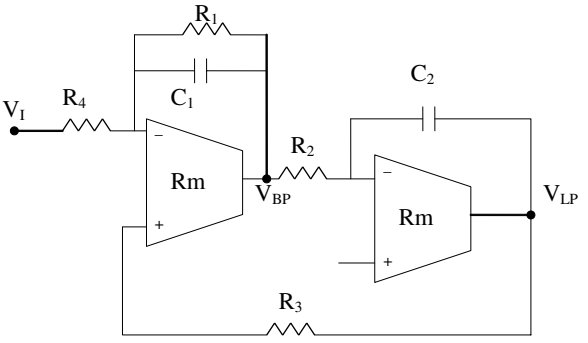


Fig. 3(a). The TT equivalent circuit using two OTRA.[7]

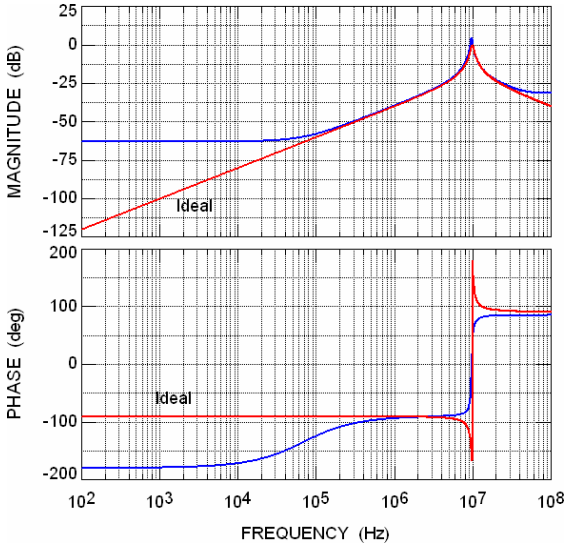


Fig. 3(b). Magnitude and phase responses of the circuit of Fig. 3(a).

For a specified DC gain $T(0)$, the design equation for $R_4$ is given by

$$R_4 = \frac{R_3}{T(0)}\,. \tag{11}$$

It is seen that the OTRA is used in a negative feedback configuration similar to the op amp. For ideal operation the transresistance $R_m$ of the OTRA approaches infinity forcing the input currents to be equal.

Spice simulation for the circuit of Fig. 3(a) using the CMOS OTRA of Fig. 2(b) biased with $V_{\rm DD} = 1.5\,{\rm V}$, $V_{\rm SS} = -1.5\,{\rm V}$, $V_{\rm B} = -0.529\,{\rm V}$, and with transistor aspect ratios as given in Table 1(a) has been performed.

The TT circuit is designed for $f_0 = 10\,{\rm MHz}$, $Q = 10$, band-pass gain = 1, by taking $C_1 = C_2 = 10\,{\rm pF}$, $R_2 = R_3 = 1.59\,{\rm k\Omega}$, $R_1 = R_4 = 15.9\,{\rm k\Omega}$.

Table 2. Comparison of the different TT circuits using different active devices.

| Circuit figure | Ref. | Active element | $R$ | $C$ | Floating $R$ | Floating $C$ | BP polarity | LP polarity | Polarity # | Indepen. gain control |
|---|---|---|---|---|---|---|---|---|---|---|
| 1(a) | 1, 2 | 3 OA | 6 | 2 | 6 | 2 | Inv. | Both | 2 | Yes |
| 3(a) | 7 | 2 OTRA | 4 | 2 | 4 | 2 | Inv. | Non-inv. | 4 | Yes |
| 4(a) | 8 | 3 CCII | 4 | 2 | 4 | 2 | Inv. | Non-inv. | 1 | Yes |
| 4(b) | 9 | 3 CCII | 4 | 2 | 3 | 1 | Inv. | Inv. | 1 | Yes |
| 4(c) | 9 | 3 CCII | 4 | 2 | 2 | 1 | Inv. | Inv. | 2 | Yes |
| 5(a) | 10 | 3 CCII | 4 | 2 | 2 | 0 | Inv. | Inv. | 2 | Yes |
| 5(b) | 10 | 3 CCII | 4 | 2 | 1 | 0 | Inv. | Inv. | 4 | Yes |
| 6(a) | 11 | 3 CCII | 4 | 2 | 0 | 0 | Non-inv. | Non-inv. | 4 | Yes |
| 7(c) | — | 4 CCII | 6 | 2 | 0 | 0 | Both | Inv. | 2 | Yes |
| 8(c) | 12 | 2 CCII | 3 | 2 | 1 | 0 | Inv. | Non-inv. | 2 | No |
| 9(a) | 14 | 2 DVCC | 3 | 2 | 0 | 0 | Non-inv. | Non-inv. | 2 | No |
| 10(a) current | 12 | 2 CCII-2 outputs | 3 | 2 | 0 | 0 | Inv. | — | 1 | No |
| 11(a) current | 15 | 2 CCII-2 outputs | 3 | 2 | 0 | 0 | Inv. | Non-inv. | 2 | No |
| 12(a) current | 17 | 3 CCII-2 outputs | 3 | 2 | 0 | 0 | Non-inv. | Non-inv. | 2 | No |

Figure 3(b) represents the band-pass magnitude and phase responses which are close to the ideal responses except for a slight increase of the gain at the center frequency.

Three more TT circuits[7] using OTRA to provide the other polarities of the band-pass and low-pass can be generated from Fig. 3(a) by OTRA ports interchange.

## 5. Tow–Thomas Circuit Using Single Output CCII

Figure 4(a) represents the TT circuit using three CCII as given in Ref. 8. The generation method used in Ref. 8 is based on replacing each op amp by its nullor equivalent circuit; an RC-nullor circuit $N_1$ is obtained. Rearranging nullators and norators of $N_1$ to form an RC–nullor circuit $N_2$ equivalent to $N_1$ is obtained. The circuit $N_2$ can be implemented by RC and CCII, and several equivalent circuits can be obtained, and the circuit in Fig. 4(a) is one of them which is given in Ref. 8. It has the same transfer functions given by Eqs. (1) and (2) as that of the original TT circuit with a positive sign for $V_{LP}$ (assuming ideal op amps and ideal CCIIs). The first two stages realize the two inverting integrators and the third stage uses the CCII as a negative impedance converter NIC[18] to transfer the same current to the first CCII in a similar way as is done by the unity gain inverter in Fig. 1(a). This circuit is of theoretical interest as it uses the CCII as an op amp, and it uses grounded $X$ ports for realizing the two integrators. It is noted that grounding the CCII port $X$ results in the loss of the current transfer property which is the basic feature of CCII. The circuit uses all floating resistors and capacitors as the two previous circuits, and it uses two resistors less than the circuit of Fig. 1(a). It has five feedback paths as in the classical TT circuit. The block diagram of Fig. 1(c) applies to this circuit.

Figure 4(b) represents the TT circuit using CCII, which was introduced in Ref. 9 based on a transformation theorem from op amps to CCII+ circuits,[9] and it uses one grounded $R$ and one grounded $C$ in the second stage realizing a noninverting integrator. The advantage of the grounded capacitor in integrated circuits is that it can absorb the stray capacitance resulting in self-compensation.[19] The third stage

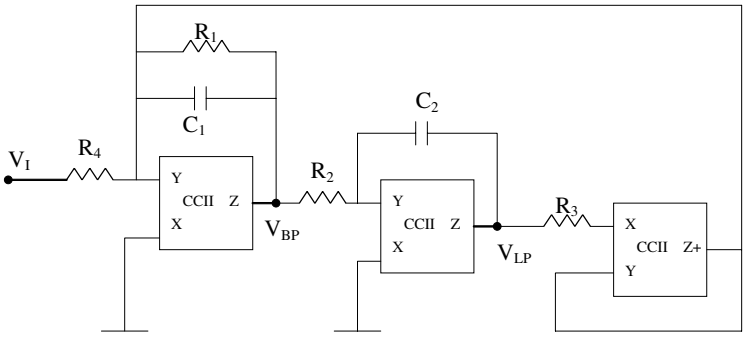


Fig. 4(a). The TT equivalent circuit using three CCII.[8]

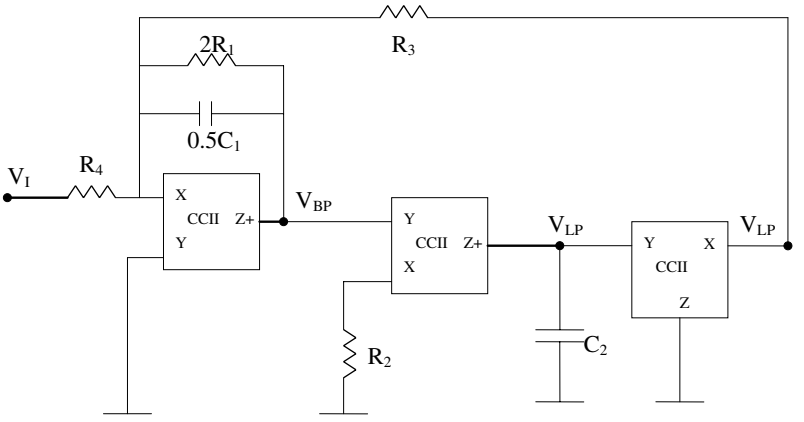


Fig. 4(b). TT equivalent circuit using three CCII.[9]

is used as a voltage follower, and the number of feedback paths has been reduced to three instead of five in the circuits of Figs. 1(a) and 4(a). The band-pass transfer function is given by Eq. (1), and the low-pass is available at two outputs, both inverting, and is given by Eq. (2b). The block diagram of Fig. 1(b) applies to this circuit.

A modified version of the circuit of Fig. 4(b) was also introduced in Ref. 9 and is shown in Fig. 4(c), which is based on replacing the voltage follower and the floating $R_3$ by a transconductor stage having a grounded $R_3$, thus reducing the floating resistors to two. The circuit is equivalent to the circuit of Fig. 4(b) and realizes both inverting responses, and the block diagram of Fig. 1(b) applies to this circuit. If the second and third CCIIs are replaced by CCII−, then a noninverting low-pass response is obtained. Of course, the band-pass response remains inverting, and the block diagram of Fig. 1(c) applies to the circuit in this case.

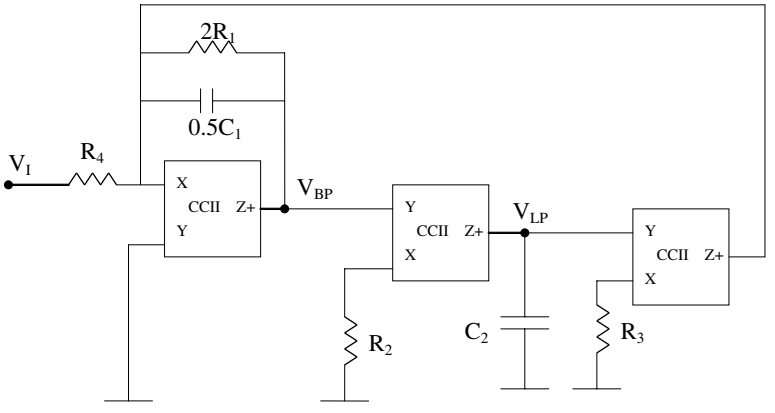


Fig. 4(c). TT equivalent circuit using three CCII.[9]

Spice simulation for the circuit of Fig. 4(c) has been performed using the CMOS CCII+ of Fig. 2(c) biased with $V_{DD} = 1.5\,V$, $V_{SS} = -1.5\,V$, $V_B = -0.56\,V$ and with transistor aspect ratios as given in Table 1(b).

The TT circuit is designed for $f_0 = 1\,MHz$, $Q = 10$, band-pass gain = 1, by taking $C_1 = C_2 = 100\,pF$, $R_2 = R_3 = 1.59\,k\Omega$, $R_1 = R_4 = 15.9\,k\Omega$.

Figure 4(d) represents the band-pass magnitude and phase responses which agree well with the ideal responses except for a slight increase in the gain magnitude at the center frequency. This circuit is of limited practicality due to the floating capacitor, and the simulation results at frequencies of the order of 10 MHz deviate slightly from the ideal response.

A grounded capacitor TT circuit using three CCIIs was introduced in Ref. 10 and is shown in Fig. 5(a). This circuit realizes inverting low-pass and band-pass

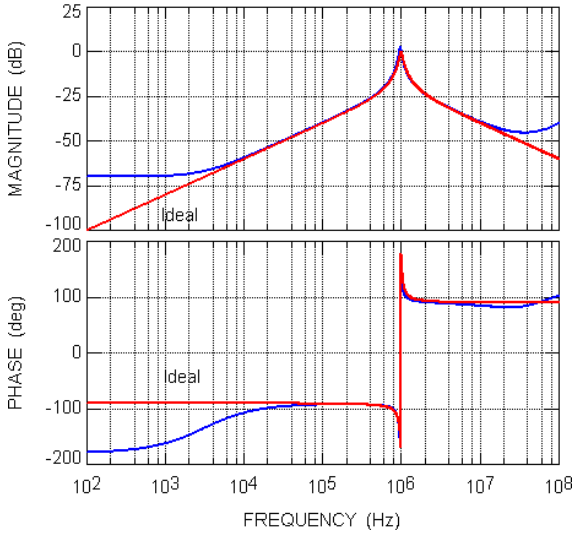


Fig. 4(d). Magnitude and phase responses of the circuit of Fig. 4(c).

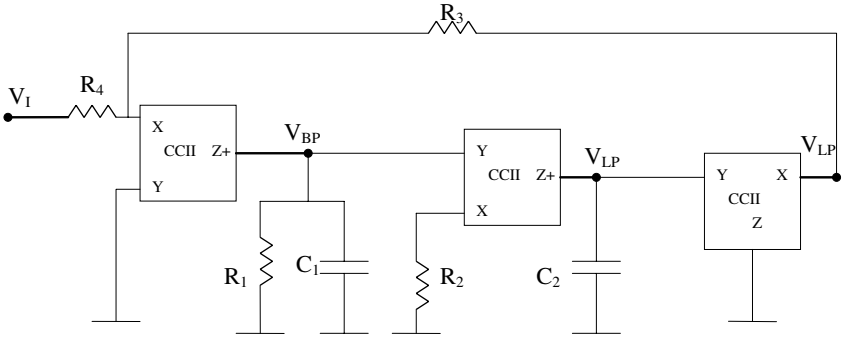


Fig. 5(a). TT equivalent circuit using three CCII.[10]

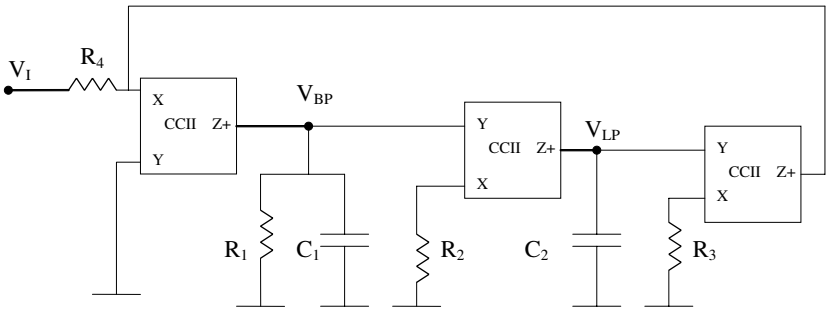


Fig. 5(b). TT equivalent circuit using three CCII.[10]

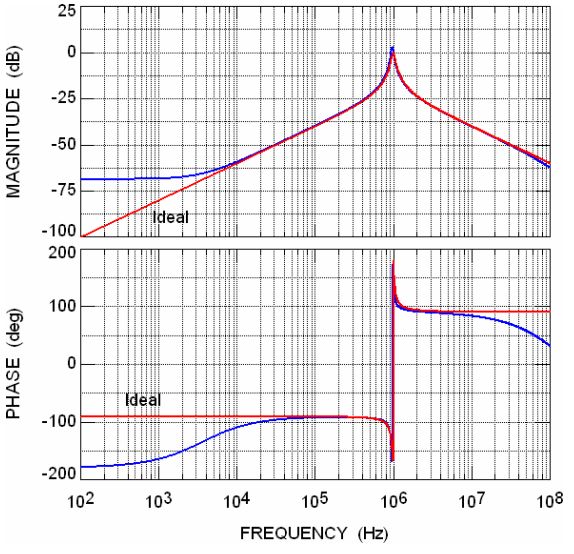


Fig. 5(c). Magnitude and phase responses of the circuit of Fig. 5(b).

responses represented by Eqs. (1) and (2b), respectively. If the first two CCIIs are taken as CCII−, then a noninverting band-pass response is obtained, and the low-pass remains inverting. Note that for stability reasons the first two CCIIs must have identical $Z$-polarity. The number of feedback paths has been reduced to only one path.

The circuit of Fig. 5(b) is generated from that of Fig. 5(a) by replacing the voltage follower and the feedback resistor $R_3$ by a voltage-controlled current source (Transconductor) realized by the third CCII and the grounded resistor $R_3$. This circuit realizes inverting band-pass and low-pass responses; however, all possible four polarity combinations can be achieved by proper choice of the three CCII $Z$-polarities, as given in Ref. 10. The circuit uses all grounded passive elements except $R_4$, which controls the gain and is floating.

Spice simulation has been carried out for the circuit of Fig. 5(b) using the CMOS CCII+ of Fig. 2(c) with the same design values as before. Figure 5(c) represents the band-pass magnitude and phase responses which are very close to the ideal responses.

A grounded resistor–grounded capacitor TT circuit with very high input impedance and using three CCIIs was introduced in Ref. 11, and is shown in Fig. 6(a). The circuit is generated from the circuit of Fig. 5(b) by port transformation method given in Ref. 20; thus, it has opposite band-pass and low-pass polarities to the circuit of Fig. 5(b) as given in Table 2. The four possible sign combinations of the band-pass and low-pass polarities can be achieved by proper choice of the three CCII $Z$-polarities.[11]

Spice simulation has been performed for the circuit of Fig. 6(a) using the CMOS CCII+ of Fig. 2(c) with the same design values as before. Figure 6(b)

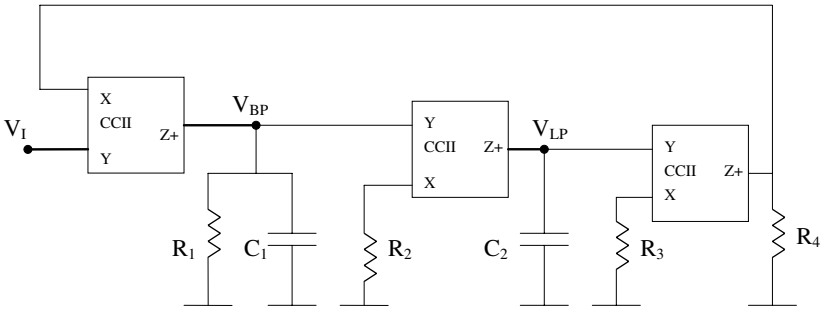


Fig. 6(a). TT equivalent circuit using three CCII.[11]

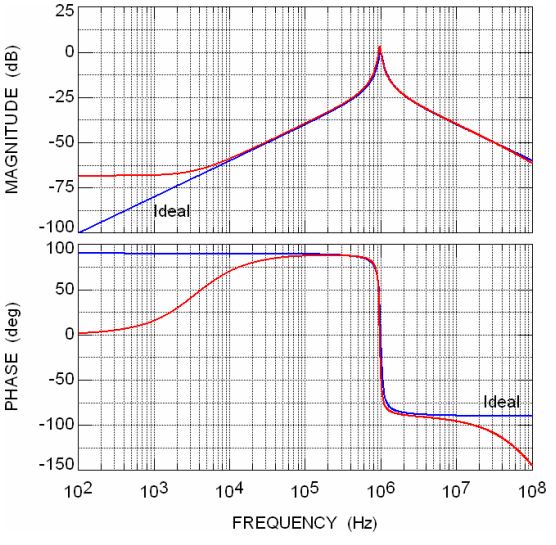


Fig. 6(b). Magnitude and phase responses of the circuit of Fig. 6(a).

represents the band-pass magnitude and phase responses which are very close to the ideal responses.

### 5.1. *The feed-forward universal filter*

The generalized form of the TT circuit using three op amps realizing a generalized transfer function is shown in Fig. 7(a).[21,22] Note that the positions of the inverter and lossless integrator are interchanged as compared to Fig. 1(a) to provide a convenient solution to the synthesis equations.[21] In Ref. 23, this circuit was realized using CCIIs, grounded $R$ and $C$, and three input current sources to represent the feed-forward paths in a one-to-one correspondence to the three op amp biquad of Fig. 7(a). By realizing the three input current sources included in the CCII circuit in Ref. 23 by three voltage-controlled current sources as suggested in Ref. 23, the three CCII+, three CCII-generalized biquad circuit shown in Fig. 7(b) is obtained.

Figure 7(c) is a modified special case from Fig. 7(b) after removing the feed-forward paths and taking $R_8 = R_7 = R$. The circuit realizes band-pass and low-pass functions, and is considered to be the CCII version of the TT circuit given in Ref. 24, which employs the same number of resistors namely six and has one inverting low-pass output. The second stage uses a CCII− to realize the inverter, and the circuit has two opposite polarity band-pass outputs and one inverting low-pass. The block diagram of Fig. 1(b) applies to this circuit. If the $Z$-polarity of the third and fourth CCII is changed to CCII+ as in Ref. 23, the circuit will realize a noninverting low-pass response.

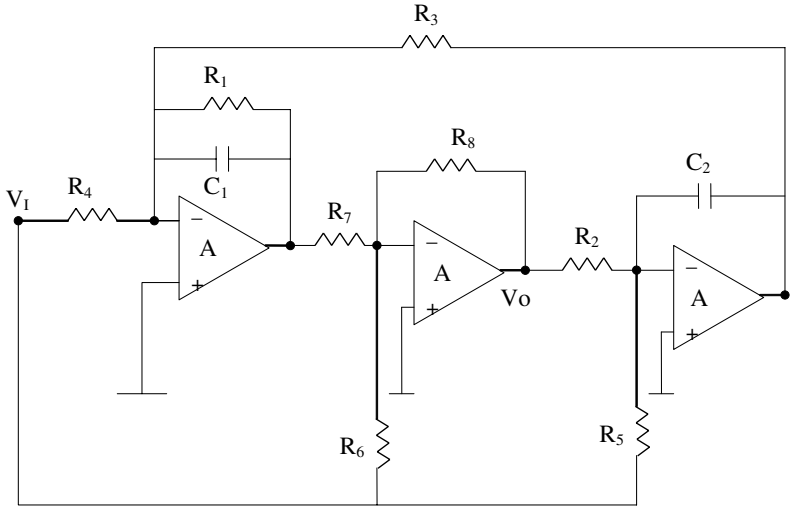


Fig. 7(a). Feed-forward three amplifier biquad based on TT circuit.[21,22]

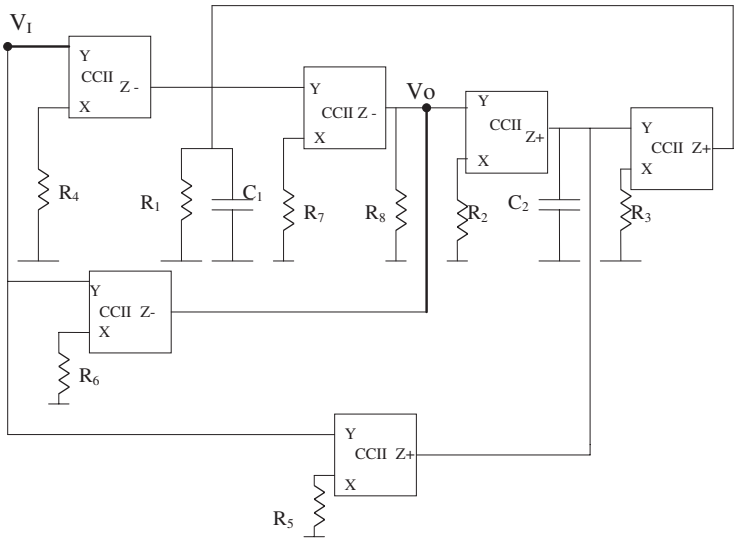


Fig. 7(b). Feed-forward 3CCII+ and 3CCII− biquad generated from the circuit of Fig. 7(a).[23]

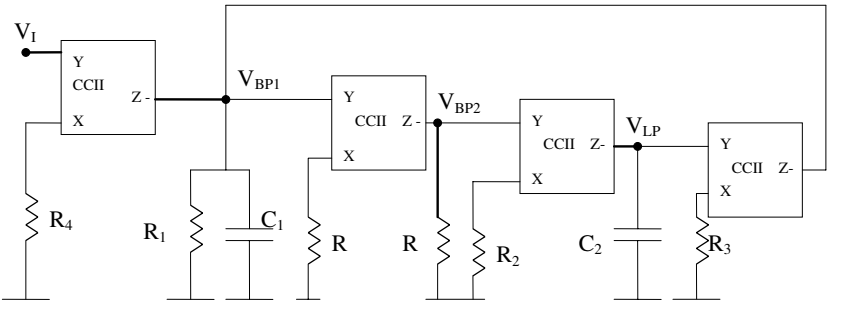


Fig. 7(c). Simplified circuit obtained from Fig. 7(b) realizing band-pass and low-pass responses.

## 6. Tow–Thomas Circuit Using Two Opposite Polarity CCIIs

In this section simplified TT circuits using three resistors and two capacitors are reviewed. The circuits are represented by the block diagrams shown in Figs. 8(a) and 8(b), which are generated from passive RLC low-pass filters.[12]

Figure 8(c) represents one of two possible circuits and is obtained from Fig. 8(a), and has the following transfer functions:

$$\frac{V_{BP}}{V_I} = \frac{\frac{-s}{C_1 R_3}}{s^2 + \frac{s}{C_1 R_1} + \frac{1}{C_1 C_2 R_2 R_3}}, \tag{12}$$

$$\frac{V_{LP}}{V_I} = \frac{\frac{1}{C_1 C_2 R_2 R_3}}{s^2 + \frac{s}{C_1 R_1} + \frac{1}{C_1 C_2 R_2 R_3}}. \tag{13}$$

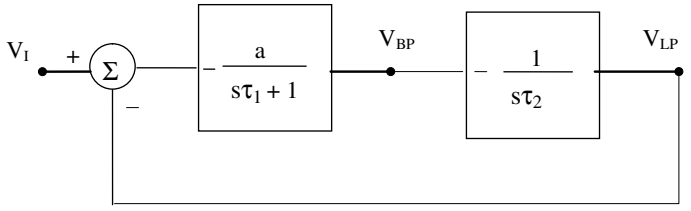


Fig. 8(a). Simplified block diagram of the TT circuit.[12]

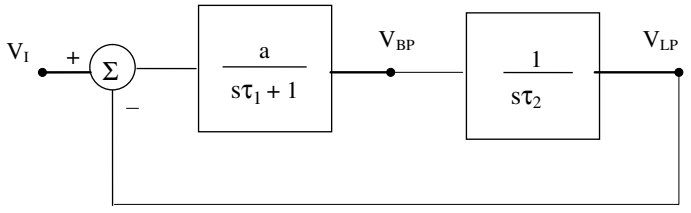


Fig. 8(b). Another simplified block diagram of the TT circuit.[12]

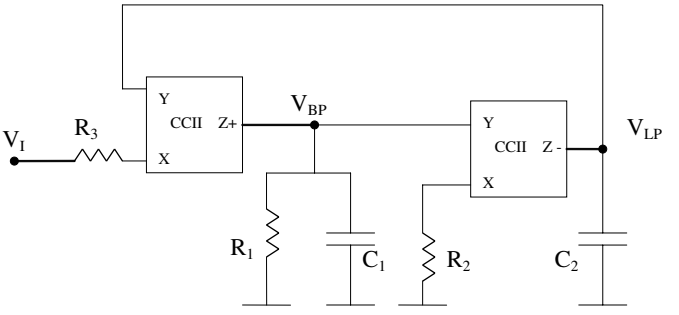


Fig. 8(c). Two opposite polarity CCII circuit realizing the block diagram of Fig. 8(a).[12]

The parameters $a, \tau_1, \tau_2$, are related to the circuit components by

$$a = \frac{R_1}{R_3}\,, \quad \tau_1 = C_1 R_1\,, \quad \tau_2 = C_2 R_2\,. \tag{14}$$

There is no independent control on the gain as a result of saving one resistor in the circuit realization. The band-pass center frequency gain is equal to $Q$ and the low-pass DC gain is unity.

Similarly, the block diagram of Fig. 8(b) can be realized from the circuit of Fig. 8(c) by interchanging the two CCII polarities resulting in noninverting band-pass and noninverting low-pass responses. It is worth noting that one of the circuits reported in Ref. 13 has the same generalized structure as that given in Fig. 8(c) with different ports of excitations.

Spice simulation has been performed for the circuit of Fig. 8(c) using the CMOS DVCC of Fig. 2(d) to realize the CCII+ and the CCII− biased with $V_{\rm DD} = 1.5\,\rm V$,

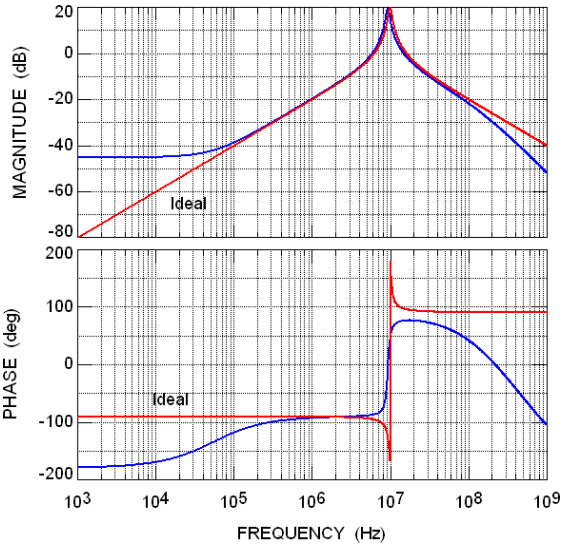


Fig. 8(d). Magnitude and phase responses of the circuit of Fig. 8(c).

$V_{SS} = -1.5\,\text{V}$, $V_{B1} = -0.52\,\text{V}$, $V_{B2} = 0.33\,\text{V}$ with the transistor aspect ratios as given in Table 1(c). The circuit is designed for $f_o = 10\,\text{MHz}$, $Q = 10$ by taking $C_1 = C_2 = 10\,\text{pF}$, $R_2 = R_3 = 1.59\,\text{k}\Omega$, $R_1 = 15.9\,\text{k}\Omega$. Figure 8(d) represents the band-pass magnitude and phase responses which agree well with the ideal responses, and it is seen that the center frequency gain is exactly equal to the theoretical value of 10.

## 7. Tow–Thomas Circuit Using DVCC

The DVCC has been used in realizing the TT circuit using grounded passive elements as shown in Fig. 9(a).[14] The circuit is represented by the block diagram of Fig. 8(b) and has noninverting polarities for the band-pass and low-pass responses. Equations (12) and (13) apply to this circuit except for the sign of Eq. (12) which

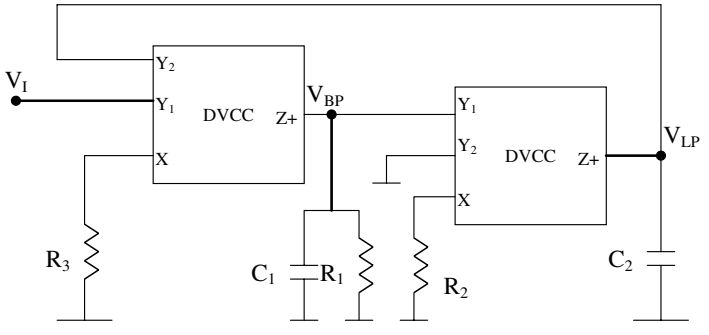


Fig. 9(a). The TT circuit using two DVCC realizing block diagram of Fig. 8(b).[14]

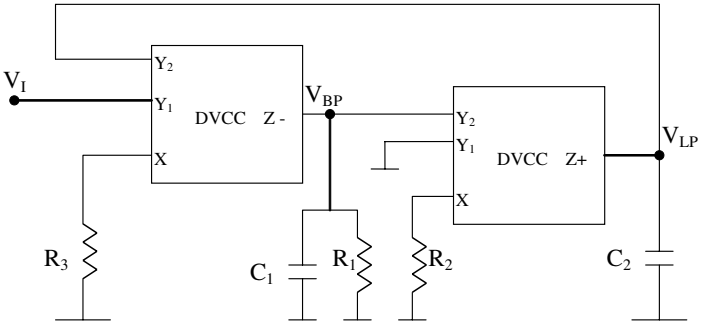


Fig. 9(b). The TT circuit using two DVCC realizing block diagram of Fig. 8(a).

is positive in this circuit. Interchanging the $Z$-polarity of the first DVCC and the $Y$-polarities of the second DVCC results in the circuit shown in Fig. 9(b). This circuit has the same equations as (12) and (13) and is represented by the block diagram shown in Fig. 8(a). Although the port interchange results in four possible circuits there are only two sets of sign combinations as summarized in Table 2.

Spice simulation has been performed for the circuit of Fig. 9(a) using the CMOS DVCC of Fig. 2(d) biased with $V_{DD} = 1.5\,V$, $V_{SS} = -1.5\,V$, $V_{B1} = -0.52\,V$, $V_{B2} = 0.33\,V$ with transistor aspect ratios as given in Table 1(c). The circuit is designed for $f_0 = 1\,MHz$, $Q = 10$ by taking same values as in the previous circuit. Figure 9(c) represents the band-pass magnitude and phase responses which are very close to the ideal responses.

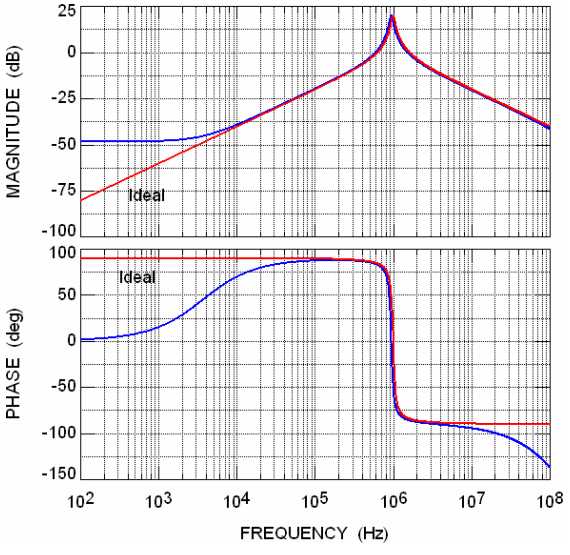


Fig. 9(c). Magnitude and phase responses of the circuit of Fig. 9(a).

## 8. Current Mode Tow–Thomas Circuit Using Balanced Output CCIIs

In this section three current mode circuits realizing current transfer functions similar to Eqs. (12) and (13) are reviewed. All of the reported circuits employ grounded resistors and capacitors and do not have independent control on gain since they use one resistor less than the TT circuit.

Figure 10(a) represents a current mode band-pass circuit[12] and is obtained directly from that of Fig. 8(c) by source transformation. The current transfer function is given by

$$\frac{I_{BP}}{I_I} = \frac{\frac{-s}{C_1R_2}}{s^2 + \frac{s}{C_1R_1} + \frac{1}{C_1C_2R_2R_3}}. \tag{15}$$

Although the current in $R_3$ is of low-pass in nature it cannot be used unless a current follower is added and in this case $R_3$ will not be grounded. Figure 10(b) represents the block diagram of this circuit.

Figure 11(a) represents a current mode TT circuit[15] using two balanced output CCII. Figure 11(b) represents the block diagram of the circuit. The band-pass current transfer function is the same as given by Eq. (15) and the low-pass current

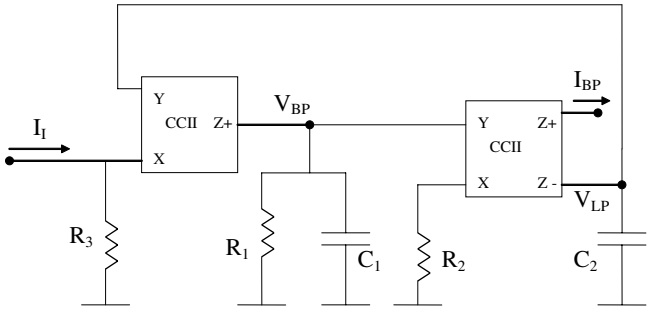


Fig. 10(a). Grounded $R$ and $C$ current mode TT circuit.[12]

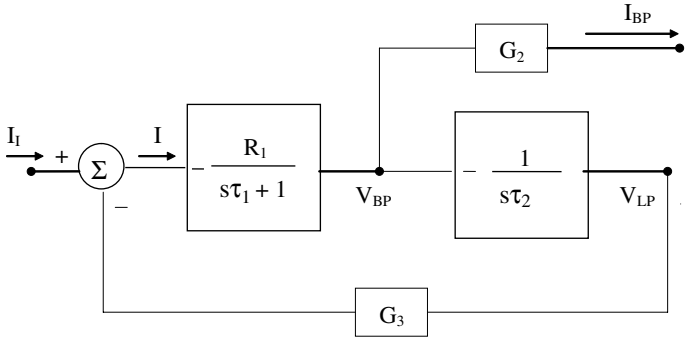


Fig. 10(b). Block diagram of the current mode TT circuit of Fig. 10(a).

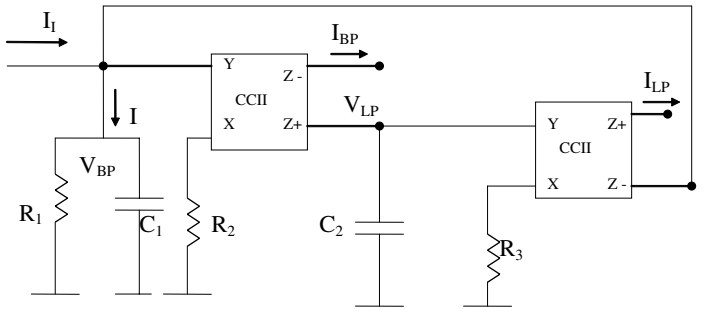


Fig. 11(a). Grounded $R$ and $C$ current mode TT circuit.[15]

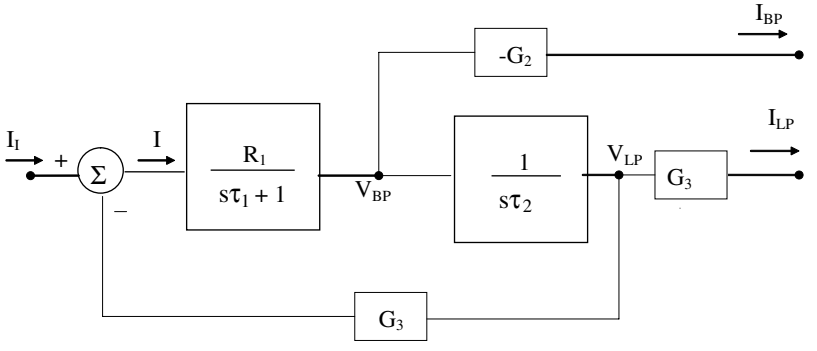


Fig. 11(b). Block diagram of the current mode TT circuit of Fig. 11(a).

transfer function is given by

$$\frac{I_{LP}}{I_I} = \frac{\frac{1}{C_1C_2R_2R_3}}{s^2 + \frac{s}{C_1R_1} + \frac{1}{C_1C_2R_2R_3}} \,. \tag{16}$$

It is to be noted that the two opposite polarity single CCII output version of this circuit was reported in Ref. 16 which requires two current followers to use the band-pass and low-pass currents. The circuit is designed for $f_0 = 10\,\text{MHz}$, $Q = 10$ by taking $C_1 = C_2 = 10\,\text{pF}$, $R_2 = R_3 = 1.59\,\text{k}\Omega$, $R_1 = 15.9\,\text{k}\Omega$. Figure 11(c) represents the band-pass magnitude and phase responses which are very close to the ideal responses.

The very low input impedance current mode TT circuit is shown in Fig. 12(a).[17] It uses two balanced output CCIIs and one single output CCII. The block diagram is shown in Fig. 12(b). Equations (15) and (16) apply to this circuit with a positive sign in Eq. (15).

Spice simulation has been performed for the circuit of Fig. 12(a) using the CMOS DVCC of Fig. 2(d) biased with $V_{\text{DD}} = 1.5\,\text{V}$, $V_{\text{SS}} = -1.5\,\text{V}$, $V_{\text{B1}} = -0.52\,\text{V}$, $V_{\text{B2}} = 0.33\,\text{V}$ with transistor aspect ratios as given in Table 1(c). The circuit is designed for $f_0 = 1\,\text{MHz}$, $Q = 10$ by taking the same values as in the previous

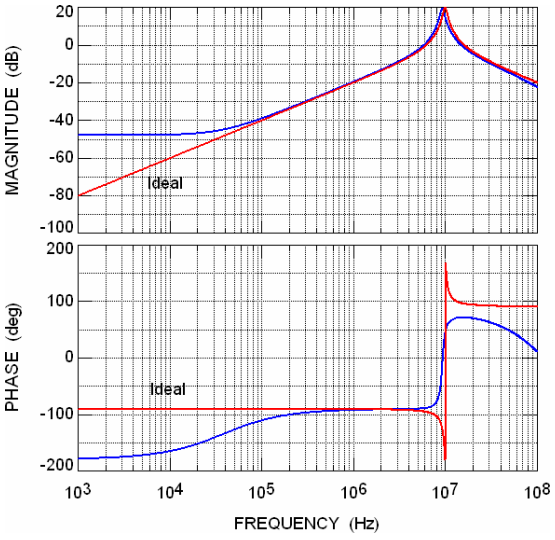


Fig. 11(c). Magnitude and phase responses of the circuit of Fig. 11(a).

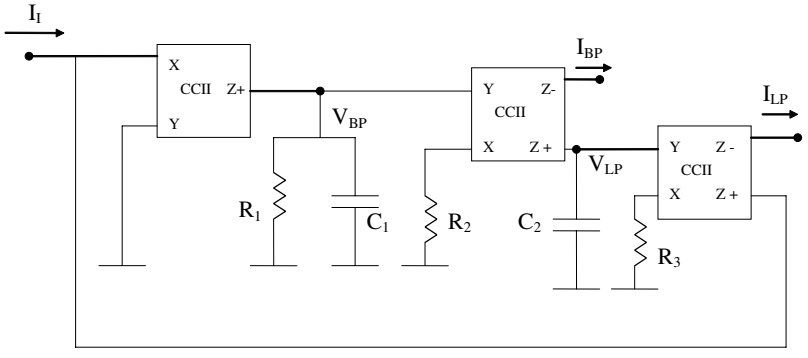


Fig. 12(a). Very low input impedance current mode TT circuit.[17]

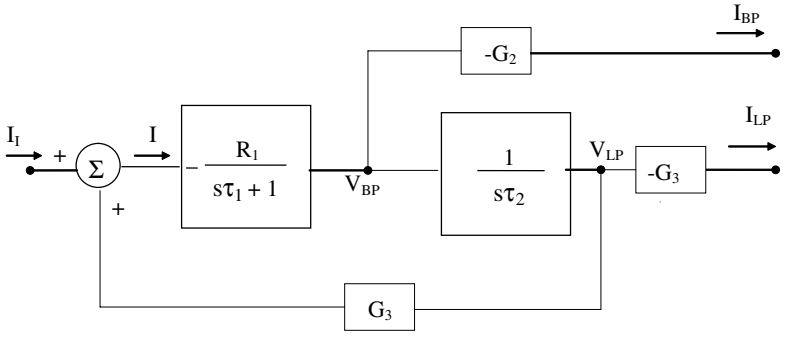


Fig. 12(b). Block diagram of the current mode TT circuit of Fig. 12(a).

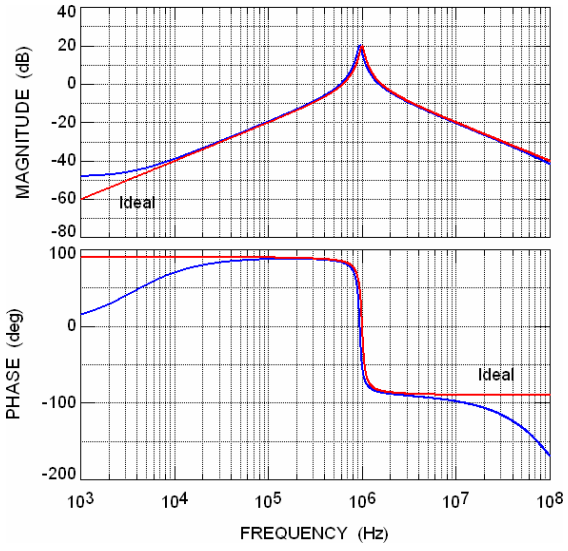


Fig. 12(c). Magnitude and phase responses of the circuit of Fig. 12(a).

circuit. Figure 12(c) represents the band-pass magnitude and phase responses from which it is seen that $f_0 = 0.95\,\text{MHz}$ (error equal to – 5%) and the center frequency gain = 10.4 (error equal to +4%). The parasitic parameters affecting this circuit are mainly $R_x$ of the first CCII and $C_z$ of the third CCII forming a first-order low-pass circuit at the input port. This parasitic effect cannot be self-compensated and needs new compensation methods to enable higher frequency circuit operation.

## 9. Nonideal Effects and Discussion

It is well known that the practical operation of the TT circuit using op amps is limited to frequencies controlled by the unity gain band-width of the op amps used.[1,2] Methods of passive and active compensation to increase the frequency of operation and reduce error in the $Q$ factor have been summarized in Ref. 3. There are four TT circuits using the OTRA; one of them is shown in Fig. 3(a). The OTRA circuits must be used with negative feedback in a way that is similar to the op amps. At high frequencies, the transresistance gain is represented by the single pole model[7]

$$R_m = \frac{R_0}{1 + \frac{s}{\omega_0}} \approx \frac{1}{sC_p}\,, \tag{17a}$$

where

$$C_p = \frac{1}{R_0\omega_0}\,. \tag{17b}$$

As demonstrated in Ref. 7 the integrating capacitors $C_1$ and $C_2$ of the TT circuit should be chosen much larger than the parasitic capacitance $C_p$ in order to eliminate its effect. Thus, the TT circuits using OTRA can be self-compensated.

### 9.1. *Frequency limitations of the TT circuits using CCII or DVCC*

There are two main factors affecting the performance of the current conveyor circuits at high frequencies.[25] The first is the single pole model of the voltage transfer from port $Y$ to port $X$ and the single pole model of current transfer from port $X$ to port $Z$. The second factor is the parasitic elements which are mainly $R_X, C_Z, C_Y$. These three most important parameters depend on the type of the CCII circuit used and they limit the frequency of operation of the TT circuit as will be explained next.

Consider the TT circuit of Fig. 4(c). The parasitic parameters affecting this circuit are mainly $R_X$ of the first CCII and $C_Z$ of the third CCII. Terminal $X$ of the first CCII will be affected by the first-order low-pass filter formed from $R_{X_1}$ and $C_{Z_3}$ as seen from the simulation results in Fig. 13(a) which shows an error magnitude of 3.6 mV at 10 MHz. This explains the deviation of the magnitude response of the TT circuit of Fig. 4(c) when operated at 10 MHz or higher. The magnitude response of Fig. 13(b) is in volts rather than decibels to enable easy identification of the magnitude error at the center frequency. From Fig. 13(b) it is seen that the band-pass center frequency voltage is reduced from 1 V to 0.48 V due to the nonzero value of $V_{X_1}$.

On the other hand, the TT circuit shown in Fig. 8(c) has the advantage that all the stray parameters can be absorbed in the external circuit components. For example, $R_{X_1}$ is added to $R_3$; so, if $R_3$ is taken much larger than $R_{X_1}$ it will absorb its effect, otherwise the design value of $R_3$ can be taken as the calculated value minus $R_{X_1}$. Similarly, $R_{X_2}$ can be self-compensated by $R_2$, $[C_{Z_1} + C_{Y_2}]$ can be

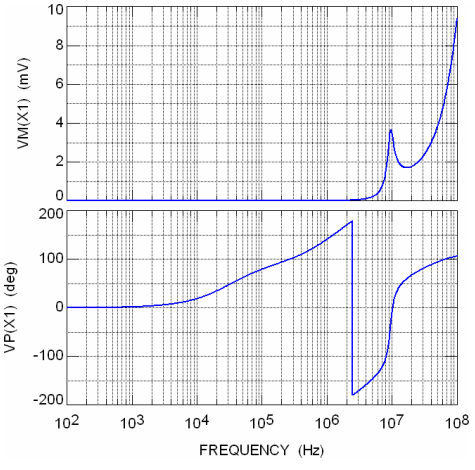


Fig. 13(a). Voltage at the $X$-terminal of the first CCII in circuit Fig. 4(c).

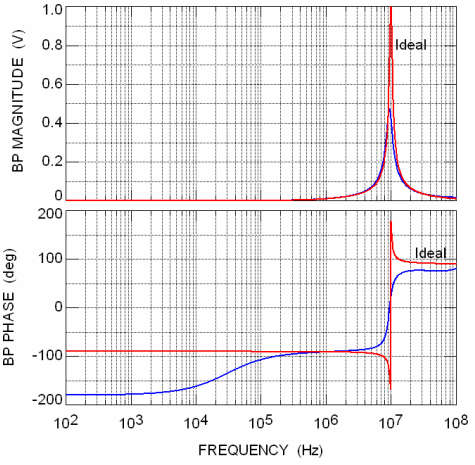


Fig. 13(b). Magnitude and phase of the band-pass output of the circuit Fig. 4(c) at 10 MHz.

self-compensated by $C_1$, $[C_{Y_1} + C_{Z_2}]$ can be self-compensated by $C_2$. This circuit is an example of the self-compensated TT circuits using CCII or DVCC.

### 9.2. *Total power dissipation*

Table 3 includes the total power dissipation of different TT circuits. Of course the TT using op amps has the largest power dissipation since the supply voltages are $\pm 12$ V. Among all circuits the TT using OTRA seems to have the lowest power dissipation.

### 9.3. *Total harmonic distortion*

Table 4(a) represents the total harmonic distortion (THD) for different active devices TT circuits at the low-pass outputs with $Q = 0.707$, DC gain $= 1$, and for input sinusoidal signal of 0.5 V peak-to-peak at 1 kHz.

Table 3. Total power dissipation for different TT circuits.

| Circuit | Reference | Frequency $f_0$ | Total power dissipation in mW |
|---|---|---|---|
| Figure 1(a) | 1, 2 | 100 kHz | 95.794 |
| Figure 3(a) | 7 | 1 MHz | 1.09325 |
| Figure 3(a) | 7 | 10 MHz | 1.09038 |
| Figure 4(c) | 9 | 100 kHz | 1.91666 |
| Figure 4(c) | 9 | 1 MHz | 1.91472 |
| Figure 5(b) | 10 | 1 MHz | 1.90666 |
| Figure 6(a) | 11 | 1 MHz | 1.90666 |
| Figure 8(c) | 12 | 1 MHz | 3.1901 |
| Figure 9(a) | 14 | 1 MHz | 3.2323 |
| Figure 11(a) | 15 | 10 MHz | 3.26212 |
| Figure 12(a) | 17 | 1 MHz | 4.91426 |

Table 4(a). Total harmonic distortion (THD) for different TT circuits at the low-pass outputs.

| Active device | Circuit | Supply voltages (V) | Frequency $f_0$ | THD at LP output (%) |
|---|---|---|---|---|
| Op Amp | Figure 1(a) | ±12 | 100 kHz | 1.5518 |
| OTRA | Figure 3(a) | ±1.5 | 1 MHz | 33.22 |
| CCII | Figure 8(c) | ±1.5 | 1 MHz | 1.52995 |
| DVCC | Figure 9(a) | ±1.5 | 1 MHz | 27.4275 |

Table 4(b). Total harmonic distortion (THD) for different active devices TT circuits at the band-pass outputs.

| Active device | Circuit | Supply voltages (V) | Frequency $f_0$ | Gain at $f_0$ | THD at BP output (%) |
|---|---|---|---|---|---|
| Op Amp | Figure 1(a) | ±12 | 100 kHz | 1 | 3.03892 |
| OTRA | Figure 3(a) | ±1.5 | 1 MHz | 1 | 6.74213 |
| CCII | Figure 8(c) | ±1.5 | 1 MHz | 10 | 6.04910 |
| DVCC | Figure 9(a) | ±1.5 | 1 MHz | 10 | 57.5163 |

Table 4(b) represents the THD for different active devices TT circuits at the band-pass outputs with $Q = 10$ and for input sinusoidal signal of 0.5 V peak-to-peak at 10 kHz.

### 9.4. *Intermodulation*

While harmonic distortion is often used to describe nonlinearities of analog circuits, certain cases require other measures of nonlinear behavior namely intermodulation distortion in a two-tone test.[26] When two signals with different frequencies are applied to a nonlinear system, the output in general exhibits some components that are not harmonics of the input frequencies, called intermodulation (IM). This phenomenon arises from mixing of two signals when their sum is raised to a power greater than unity. Of particular interest is the third-order intermodulation products.

Table 5 includes a comparison of the $IM_3$ factor for four different TT circuits calculated for a two-tone test at 10 kHz and 20 kHz with a sinusoidal signal of 0.1 V peak-to-peak. It is seen that the circuit of Fig. 8(c) provides the lowest $IM_3$ factor.

Table 5. The $IM_3$ factor calculated for four different TT circuits.

| Circuit | Reference | Filter output | $IM_3$ (dB) |
|---|---|---|---|
| Figure 3(a) | 7 | LP | −8.5 |
| Figure 5(b) | 10 | LP | −14.7 |
| Figure 8(c) | 12 | LP | −40 |
| Figure 9(a) | 14 | LP | −38 |

### 9.5. *Input and output referred noise*

Noise can be defined as any random interference unrelated to the signal of interest.[26] This definition distinguishes between noise and deterministic phenomena such as harmonic distortion and IM discussed in the previous sections. Figure 14 represents the input and output referred noise spectral densities simulated for different TT circuits with $f_0 = 1\,\text{MHz}$. It is seen that there are only slight differences between the different circuits.

## 10. Conclusions

The realization of the TT circuit using OTRA, CCII and DVCC is reviewed. First, the OTRA TT circuit which employs two OTRA with all passive elements being floating is summarized with equations and Spice simulations. The CCII TT circuits are reviewed next. Eight different CCII circuits showing the progress of the

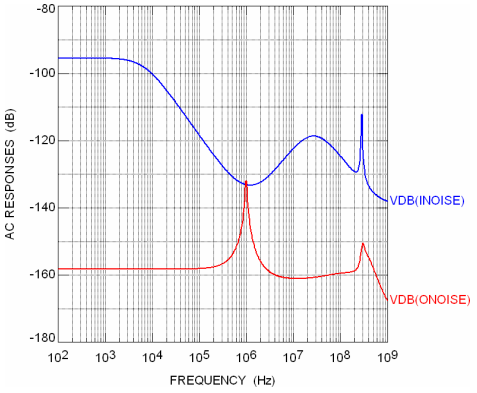


Fig. 14(a). Input and output referred noise voltage spectral densities for the circuit of Fig. 3(a).

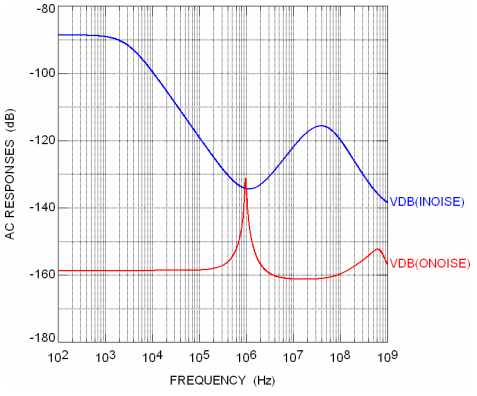


Fig. 14(b). Input and output referred noise voltage spectral densities for the circuit of Fig. 4(c).

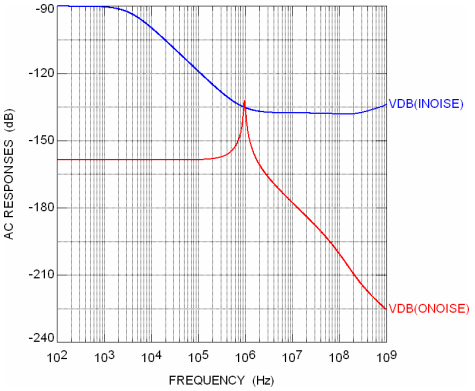


Fig. 14(c). Input and output referred noise voltage spectral densities for the circuit of Fig. 5(b).

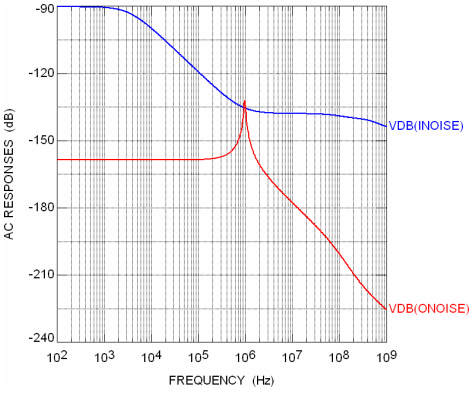


Fig. 14(d). Input and output referred noise voltage spectral densities for the circuit of Fig. 6(a).

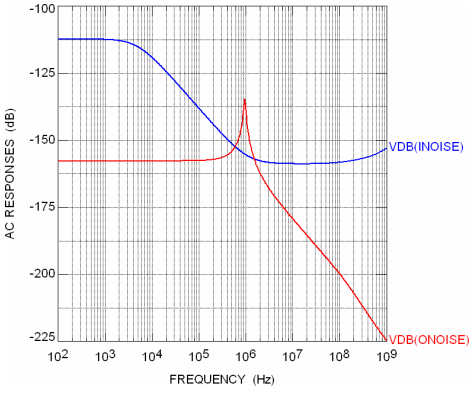


Fig. 14(e). Input and output referred noise voltage spectral densities for the circuit of Fig. 8(c).

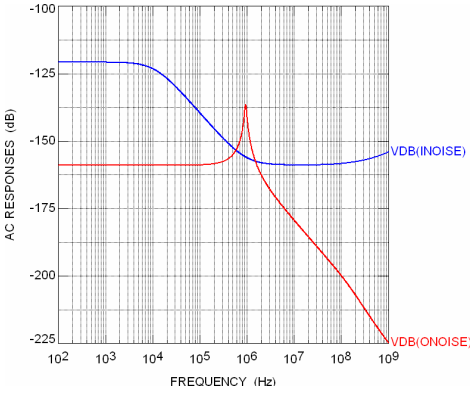


Fig. 14(f). Input and output referred noise voltage spectral densities for the circuit of Fig. 9(a).

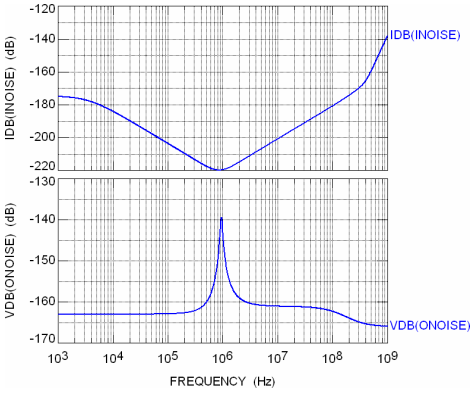


Fig. 14(g). Input and output referred noise voltage spectral densities for the circuit of Fig. 12(a).

TT circuits using CCII are summarized. The circuit of Fig. 4(a) is of theoretical interest. The circuits of Figs. 4(b) and 4(c) have the disadvantage of employing one floating capacitor. The circuit of Fig. 5(b) is affected by the parasitic parameters $R_{X_1}$ and $C_{Z_3}$. The circuit of Fig. 6(a) has the advantage of very high input impedance with all passive elements being grounded. It is also affected by the parasitic parameters $R_{X_1}$ and $C_{Z_3}$. The circuit of Fig. 7(c) is affected by $C_{Z_2}$ and $C_{Y_3}$; it can however absorb all other stray parameters. The circuit of Fig. 8(c), although has a finite input resistance, is the best as it can be self-compensated by absorbing all stray parameters in the passive circuit components. The DVCC as the active building block in realizing the TT circuit is also considered. Finally, current mode TT circuits using balanced output CCII are summarized. The circuit of Fig. 11(a) is self-compensated and can absorb all stray parameters. Spice simulation results using technology SCN 05 feature size 0.5 $\mu$m from MOSIS vendor: AGILENT are included to prove the practicality of the TT circuits. Additional simulation results

for the total power dissipation, total harmonic distortion, intermodulation $IM_3$, input and output referred noise spectral densities are also included for comparison purposes.

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