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CMOS Differential Current Conveyors and Applications for Analog VLSI

HASSAN O. ELWAN AND AHMED M. SOLIMAN

Electronics and Comm. Engineering Dept., Cairo University, Egypt

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Abstract. Novel differential current conveyor building blocks are defined. CMOS realizations of these blocks are then given. One of the proposed conveyor circuits is seen to be insensitive to the threshold voltage variation due to the body effect. The properties of the differential current conveyors are shown to be suitable for VLSI applications employing MOS transistors operating in the ohmic region. This is demonstrated by realizing four quadrant multiplier cells, current mode and mixed mode continuous time MOSFET-C filters based on the proposed blocks. PSPICE simulations indicate the excellent performance of the differential current conveyor circuits.

Key Words: current conveyors, filters

1. Introduction

The differential current conveyor is a powerful current mode building block with properties that make it ideal for designing all MOS analog circuits which can be integrated on a single chip. The proposed analog block is an extension to the second generation current conveyor (CCII) proposed by Sedra and Smith [1]. Although the CCII can be used to realize many analog functions [2–7], the circuits employing the CCII often relies on floating resistors and capacitors that are difficult to integrate on chip. The proposed differential current conveyor on the other hand can be used with MOS transistors operating in the ohmic region to implement the required analog functions where the even and the odd nonlinearties associated with the transistors operating in this mode are both canceled out. Thus one of the applications of the differential current conveyor is the realization of current mode as well as mixed mode continuous time MOSFET-C filters. Furthermore one of the proposed circuits is compatible with digital semicustom sea of gates integrated circuits. CMOS digital semicustom integrated circuits are used for a variety of applications, mainly to reduce the design time. The sea of gates (SOG) concept was introduced recently [8]. In these chips the interconnections are placed over the active region, this leads to flexible designs and effective use of chip area. Recently digital CMOS sea of gates has been used to realize high performance analog functions [9] which allow for effective implementation of mixed digital analog systems. One of the drawbacks of realizing analog cells on the sea of gates is that all transistors are in the same well hence the threshold voltage varies due to the body effect, thus causing distortion.

In this paper the differential current conveyor properties are described. New CMOS realizations of the suggested blocks are given. One of the proposed circuits is seen to be independent of the threshold voltage variation due to the body effect and hence is a versatile block for implementing analog functions on the digital SOG chips. Applications of the proposed blocks are, four quadrant multiplier cells, current mode and mixed mode MOSFET-C continuous time filters.

2. The Differential Current Conveyor

The differential current conveyor (DCC) is a five-terminal analog building block as shown in Fig. 1(a) with a describing matrix of the form:

$$\begin{bmatrix} V_{X_1} \\ V_{X_2} \\ I_{Z_1} \\ I_{Z_2} \\ I_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 \\ 1 & -1 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X_1} \\ I_{X_2} \\ V_{Z_1} \\ V_{Z_2} \\ V_Y \end{bmatrix} \quad (1)$$

The MOS realization of the DCC is shown in Fig. 1(b). All transistors are assumed to be operating in the saturation region with the sources connected to their substrates. The Y terminal voltage is applied to

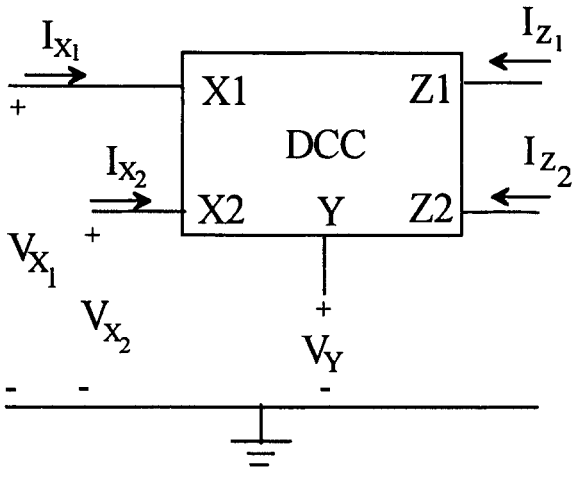

Fig. 1a. The differential current conveyor.

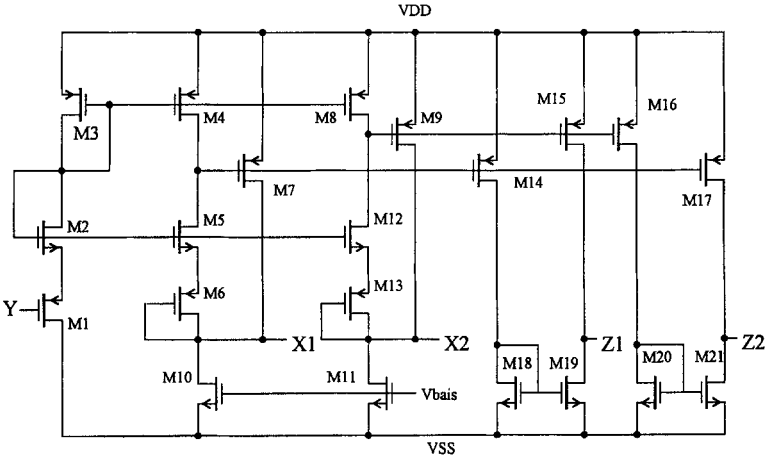

Fig. 1b. The DCC circuit realization.

the gate of transistor M1 which together with M2 forms a CMOS pair. The current through this pair is mirrored by M3, M4 and M8 to the CMOS pairs formed by M5, M6 and M12, M13 and since the gate voltage of M2, M5 and M12 are the same therefore:

$$V_{X_1} = V_{X_2} = V_Y \tag{2}$$

The negative feedback operation of the transistors M7 and M9 with the bias currents flowing through transistors M10 and M11 insure that the voltage at X1 and X2 remain independent of the current withdrawn from the X terminals. The difference between the X1 and the X2 currents is conveyed to the Z1 terminal by the mirroring action of transistors M14, M15 and the current mirror formed by transistors M18, M19. The inversion of this current is obtained at the Z2 terminal by repeating the above circuit with interchanged current mirror transistors.

The above analysis assumes that the sources of the transistors are connected to their substrates. This is necessary in order to make the threshold voltage constant for all transistors, however this requires that the NMOS transistors and the PMOS transistors be separable in different wells. Although twin well CMOS technology is available it is not a standard VLSI technology. Another disadvantage is that the use of separate wells increases the layout area because every time separate wells are used, guard rings have to surround each well to prevent latch-up.

3. The Modified Differential Current Conveyor

A second useful building block is the modified differential current conveyor (MDCC) shown in Fig. 2(a). This analog block is similar to the DCC except that the Y terminal is replaced by a biasing terminal B. The current from the B terminal is not zero and is of no interest. The B terminal is used only for biasing. The describing matrix of the modified differential current conveyor is given by:

$$\begin{bmatrix} V_{X_1} \\ V_{X_2} \\ I_{Z_1} \\ I_{Z_2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ -1 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X_1} \\ I_{X_2} \\ V_{Z_1} \\ V_{Z_2} \end{bmatrix} \quad (3)$$

The proposed CMOS circuit realization of the MDCC is shown in Fig. 2(b). This circuit realization has the advantage of being insensitive to the threshold voltage variation due to the body effect. Therefore all the N transistors are placed in the same well which decreases the layout area and makes the circuit realizable in any CMOS technology. It can also be seen that the circuit realization of the DCC is simplified by replacing the CMOS pairs M1, M2, M5, M6 and M12, M13 of Fig. 1(b) by NMOS-transistors and using the source of M1 as the biasing terminal to which the biasing voltage VB is applied.

Assuming that all the transistors are operating in the saturation region, thus the current of the NMOS transistor equals to:

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2 \quad (4)$$

where

$$K = \mu_n C_{ox} \frac{W}{L}$$

and
V_T is the threshold voltage which equals to:

$$V_T = V_{T_o} + \gamma(\sqrt{V_{SB} + 2\phi_f} - \sqrt{2\phi_f}) \quad (5)$$

Therefore the current through transistor M1 is given by:

$$I_1 = \frac{K}{2}(V_G - V_B - V_{T_1})^2 \quad (6)$$

similarly the current through M2 is given by:

$$I_2 = \frac{K}{2}(V_G - V_{X_1} - V_{T_2})^2 \quad (7)$$

Table 1. Aspect ratios for the DCC.

Transistors	Aspect ratio (W/L)
M1,M6,M13	2/4
M2,M5,M12	2/4
M3,M4,M8	20/2
M7,M14,M17	24/2
M9,M15,M16	24/2
M18,M19,M20,M21	10/2

Since $I_1 = I_2$ by the current mirroring action of the transistors M3 and M4 therefore the voltage offset is given by:

$$\Delta V = V_{X_1} - V_B \quad (8)$$

from the above equations ΔV is obtained as:

$$\Delta V = \gamma(\sqrt{V_B - V_{SS} + 2\phi_f} - \sqrt{V_B - V_{SS} + 2\phi_f + \Delta V}) \quad (9)$$

Thus the obvious solution is:

$$\Delta V = 0 \quad (10)$$

Similarly the offset voltage between the biasing terminal B and the terminal X2 is also zero. Hence the circuit operation is independent of the threshold voltage variation due to the body effect.

Fig. 3(a) shows the voltage conveying property of the DCC where the voltage at the X-terminal is plotted against the voltage applied to the Y-terminal. The transistors aspect ratios are given in Table 1. The supply voltages used are ±5 volts and the biasing current is adjusted to $160\mu A$. Fig. 3(b) shows the current from the Z terminal of the MDCC where two resistors of 40K are connected between the X-terminals and the two inputs V_{i_1} and V_{i_2}. The voltage V_{i_1} is scanned for different values of V_{i_2} with the biasing terminal B grounded resulting in the shown family of curves. It is worth noting that that MDCC can operate from supply voltages down to −1 to 3 volts however the output swing is reduced to about 2.2 volts.

4. Four Quadrant Multiplier Cells

The DCC and the MDCC can be used to realize multiplier/transconductance cells as shown in Fig. 4(a) and Fig. 4(b) respectively. The transconductance multiplying action is achieved by the transistors M11 and M12

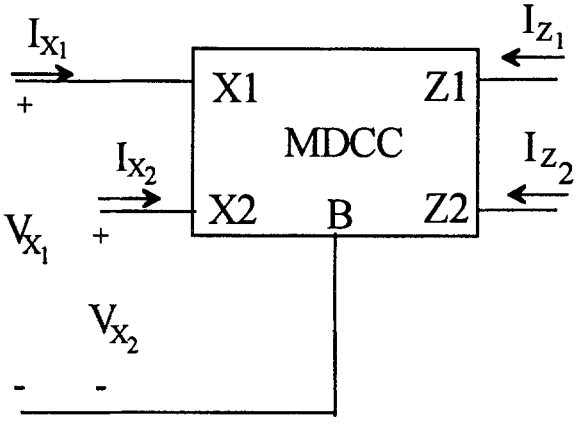

Fig. 2a. The modified differential current conveyor.

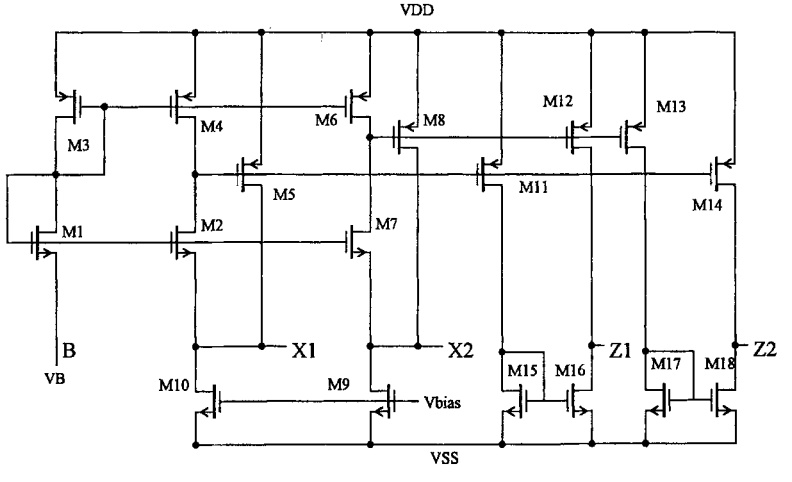

Fig. 2b. The MDCC circuit realization.

which are operating in the ohmic region [10]. The configuration shown cancels both the even and the odd nonlinearities as discussed next.

The current in the ohmic region is given by:

$$I = K(V_G - V_T)(V_D - V_S) + a_1(V_D^2 - V_S^2) + a_2(V_D^3 - V_S^3) + \cdots \quad (11)$$

Since transistors M11 and M12 have equal drain and equal source voltages by the action of the DCC therefore the output currents I_{Z_1} and I_{Z_2} are given by

$$I_{Z_1} = K(V_{G_1} - V_{G_2})(V_1 - V_2) \quad (12)$$

$$I_{Z_2} = K(V_{G_1} - V_{G_2})(V_2 - V_1) \quad (13)$$

Table 2. Aspect ratios for the MDCC.

Transistors	Aspect ratio (W/L)
M1,M4,M7	2/4
M2,M3,M6	12/2
M5,M11,M14	6/2
M8,M12,M13	6/2
M15,M16,M17,M18	10/2

Thus the cells can be used as a four quadrant multiplier/transconductance. Fig. 4(c) represents the multiplier output current when the voltage V1 is scanned for different values of the differential gate voltage. To realize a multiplier with a high impedance the cell of

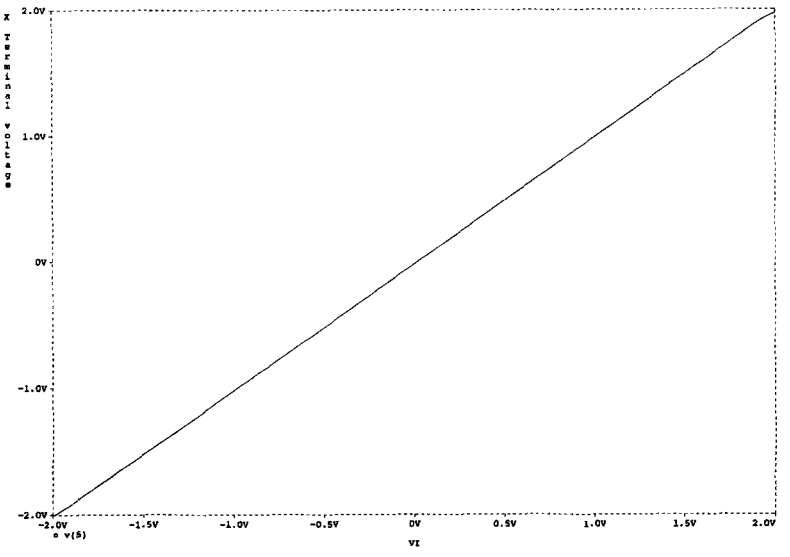

Fig. 3a. PSPICE simulation of the voltage conveying property of the differential current conveyor.

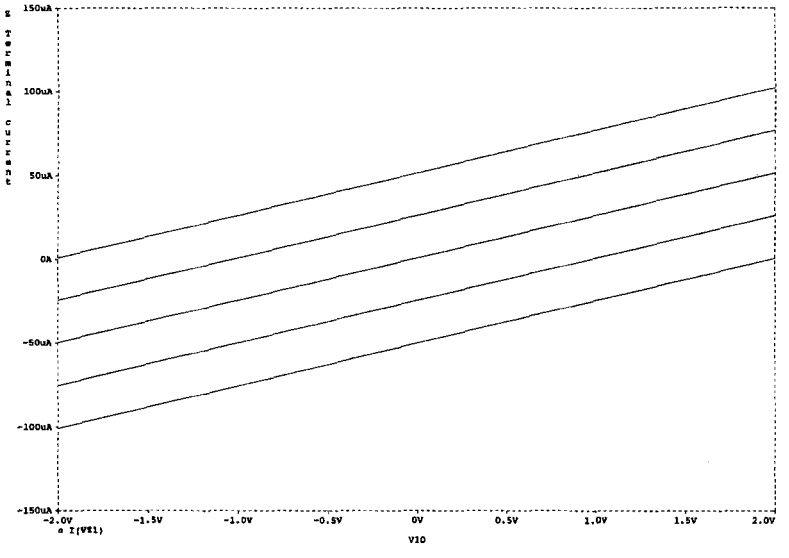

Fig. 3b. PSPICE simulation of the differential current conveying property of the modified differential current conveyor.

Fig. 4(a) should be used with V1 set to zero and the signal applied to the single ended input V2.

Recently analog multipliers have been used in implementing artificial neural networks [11] these parallel processing networks require a number of inputs to be added with different weights (weighted sum). This can be realized using the MDCC as shown in Fig. 4(d) where the output current is given by:

$$I_o = \sum_{i=1}^{n} (K_i V_{G_i}) V_i \tag{14}$$

5. Integrated Continuous Time Filters using the DCC and MDCC

Integrated continuous time filters are now widely accepted in industry [12,13] where they are used in applications involving direct signal processing especially for medium dynamic range applications in cases where high speed and/or low power dissipation are needed. The DCC is a suitable building block for the realization of MOSFET-C current mode filters. Although MOSFET-C filters can be implemented in the voltage

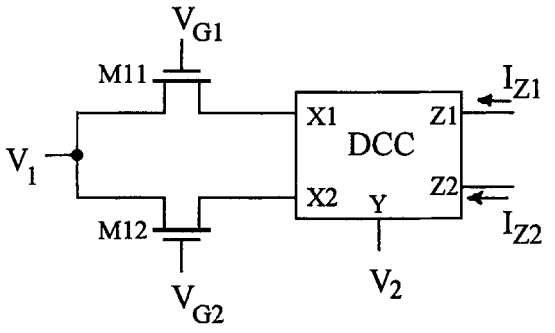

Fig. 4a. A four quadrant multiplier using the DCC.

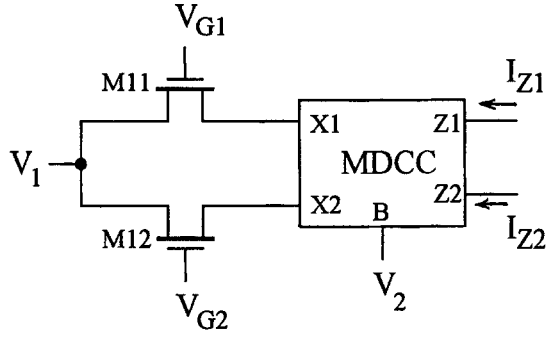

Fig. 4b. A four quadrant multiplier using the MDCC.

mode using op-amps, they usually suffer from the finite gain-bandwidth product of the operational amplifiers used which limits the frequency range. The circuit shown in Fig. 5(a) represents a mixed mode second order bandpass filter based on the DCC. Transistors M_{i1} and M_{i2} (i = 1, 2) are operating in the ohmic region with their nonlinearities canceled out as shown in the previous section. The input to this filter section is a voltage while the output is a current and the transfer function is given by:

$$\frac{I_{BP}}{V_i} = \frac{S\frac{G_1G_2}{C_2}}{S^2 + S\frac{G_1}{C_1} + \frac{G_1G_2}{C_1C_2}} \tag{15}$$

where

$$G_1 = K_1(V_{G_{11}} - V_{G_{12}}) \tag{16}$$

$$G_2 = K_2(V_{G_{21}} - V_{G_{22}}) \tag{17}$$

the bandpass response of the above filter is shown in Fig. 5(b) with C1 − C2 = 0.1nf, $V_{G_{11}} = V_{G_{21}} = 4V$, $V_{G_{12}} = V_{G_{22}} = 2V$ and $K_1 = 15\mu A/V^2$, $K_2 = 240\mu A/V^2$

A second order current mode lowpass filter employing the MDCC is shown in Fig. 6(a). The lowpass current transfer function is given by:

$$\frac{I_{LP}}{I_i} = \frac{\frac{G_1G_2}{C_1C_2}}{S^2 + S\frac{G_1}{C_1} + \frac{G_1G_2}{C_1C_2}} \tag{18}$$

The ω_o and the Q factor are given by:

$$\omega_o = \sqrt{\frac{G_1G_2}{C_1C_2}} \qquad Q = \sqrt{\frac{G_2C_1}{G_1C_2}} \tag{19}$$

where

$$G_1 = K_1(V_{B_{11}} - V_{B_{12}}) \tag{20}$$

$$G_2 = K_2(V_{B_{21}} - V_{B_{22}}) \tag{21}$$

Fig. 6(b) represents the lowpass current response of the filter designed to give a Butterworth response where: C1 = C2 = 0.05nF, $V_{B_{11}} = V_{B_{21}} - 2.5V$, $V_{B_{12}} = V_{B_{22}} = -3.5V$, $K_1 = 60\mu A/V^2$ and $K_2 = 30\mu A/V^2$.

Finally a universal current mode biquad is shown in Fig. 7(a). The lowpass, bandpass and highpass current transfer functions are given respectively by:

$$\frac{I_{HP}}{I_i} = \frac{S^2}{D(s)}, \quad \frac{I_{BP}}{i_i} = \frac{-\frac{G_2}{C_1}S}{D(s)} \quad \text{and} \quad \frac{I_{LP}}{I_i} = \frac{\frac{G_3G_2}{C_1C_2}}{D(s)} \tag{22}$$

where

$$D(s) = S^2 + \frac{G_1}{C_1}S + \frac{G_1G_2}{C_1C_2} \tag{23}$$

and

$$G_i = K_i(V_{B_{i2}} - V_{B_{i1}}) \qquad \text{(i, 1, 2, 3)} \tag{24}$$

Fig. 7(b) shows the highpass and lowpass current responses of this filter with C1 = 0.1nf, C2 = 0.05nf, K1 = K2 = K3 = $30\mu A/V^2$ and $V_{B_{i2}} = -2V$, $V_{B_{i1}} = -5V$ for i = 1, 2, 3.

It can also be seen that a notch response can be realized by connecting the highpass and the lowpass output terminals.

6. Conclusion

New current mode analog building blocks are proposed. CMOS circuit realizations of the proposed blocks are given. It is then shown the the properties of

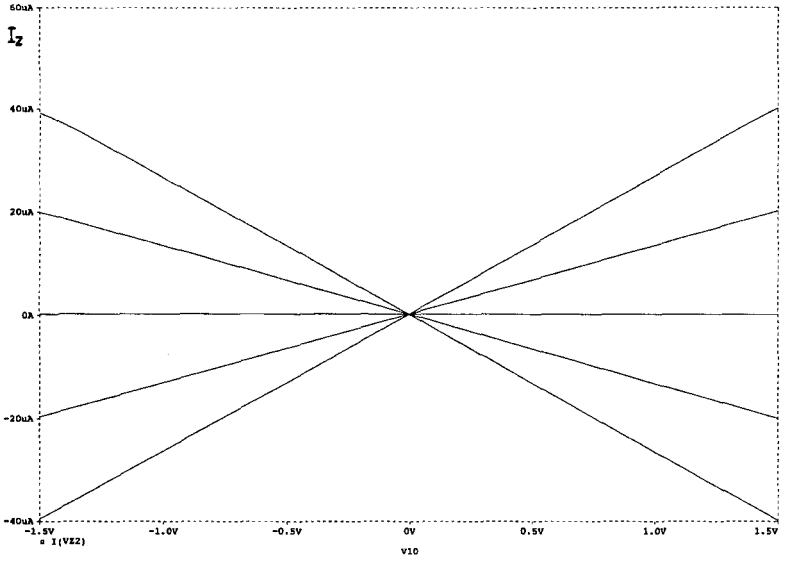

Fig. 4c. PSPICE simulation of the multiplier shown in Fig. 4(b).

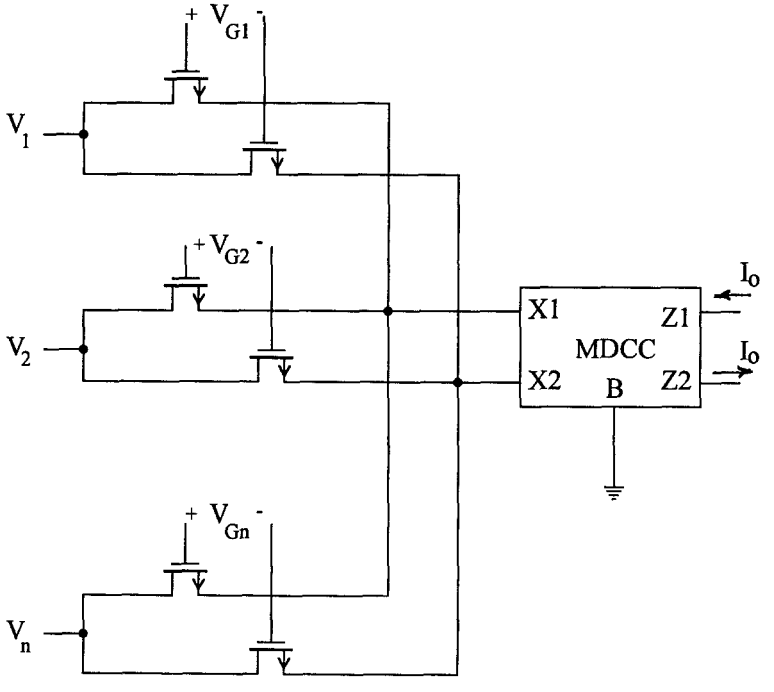

Fig. 4d. Weighted sum multiplier circuit.

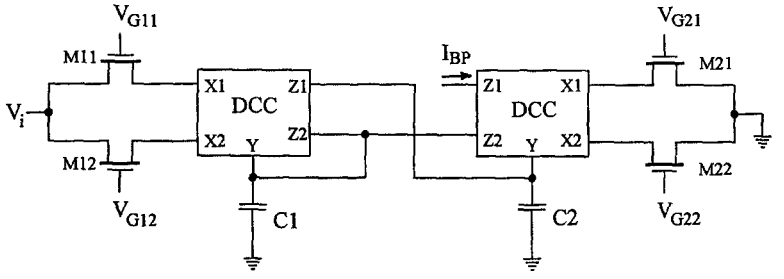

Fig. 5a. A mixed mode second order band-pass filter.

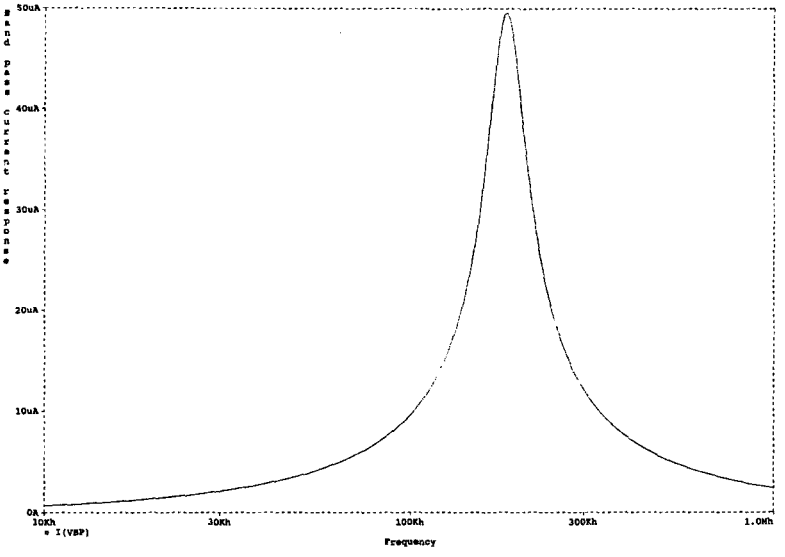

Fig. 5b. The band-pass frequency response of the filter shown in Fig. 5(a).

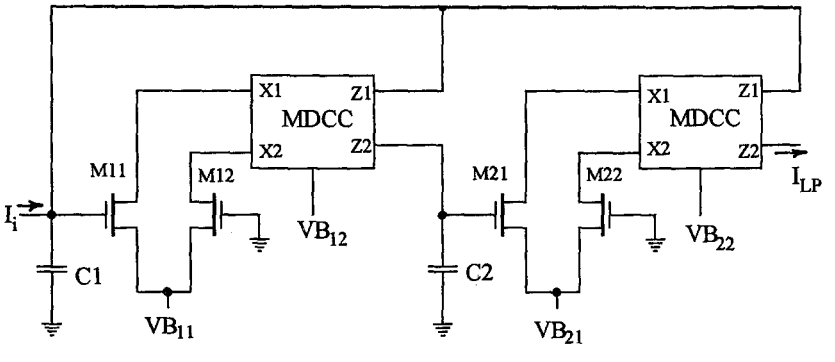

Fig. 6a. A current mode low pass filter using MDCC.

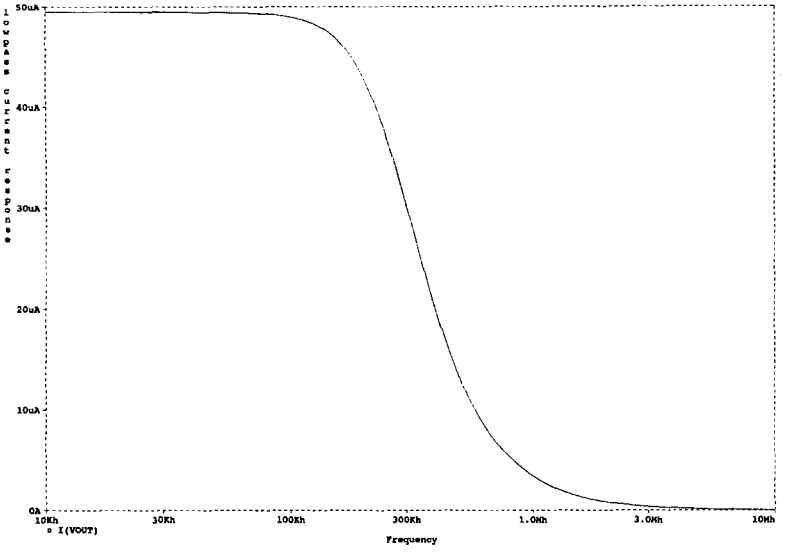

Fig. 6b. The frequency response of the low-pass current mode filter shown in Fig. 6(a).

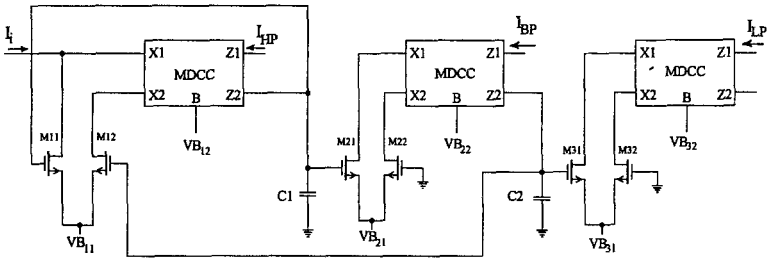

Fig. 7a. A universal current mode filter based on the MDCC.

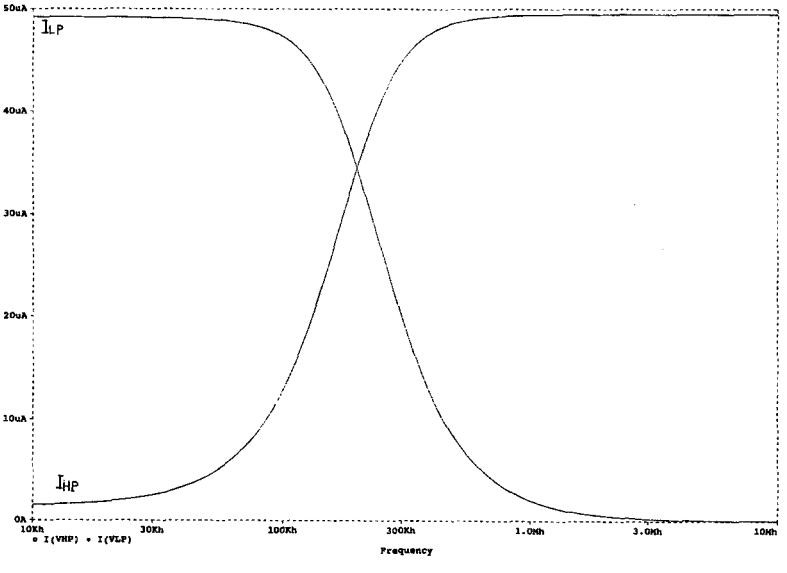

Fig. 7b. The low-pass and high-pass frequency responses of the filter shown in Fig. 7(a).

these blocks are suitable for designing current mode circuits using CMOS technology. The proposed MDCC circuit is insensitive to the threshold voltage variation due to the body effect and hence can be implemented on digital sea of gates integrated circuits. The main advantage of the proposed DCC and MDCC is that they can implement different analog circuits without the need of resistors, since the blocks can be easily used to cancel the even and the odd nonlinear terms associated with MOS transistors operating in the ohmic region. The proposed applications which employ this concept are MOSFET-C continuous time filters (both current mode and mixed mode) and four quadrant analog multipliers. The use of the suggested blocks for low voltage low power applications is currently under investigation [14].

Acknowledgements

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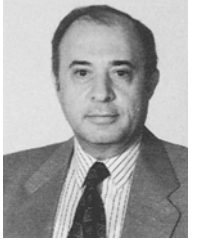
Hassan O. Elwan was born in Cairo, Egypt in 1971. He received his B.Sc. degree with honors from the electronics and communication department Cairo University 1994. He was appointed as a T.A. in the same year and is now working to receive his M.Sc. degree. His research interests include current mode circuit design, filtering, mixed D/A systems and VLSI design and test.



Ahmed M. Soliman was born in Cairo Egypt, on November 22, 1943. He received the B.S. degree from Cairo University, Egypt, in 1964, and the M.S. and Ph.D. degrees from the University of Pittsburgh, PA., U.S.A. in 1967 and 1970, respectively, all in electrical engineering.

He is currently Professor and Head Electronics Group, Electronics and Communications Engineering Department, Cairo University, Egypt.

Dr. Soliman served as Professor and Chairman of the Electrical Engineering Department, United Arab

Emirates University (1985–1987), and as the Associate Dean of Engineering at the same University (1987–1991).

He has held visiting academic appointments at the American University in Cairo (1982–1983), Florida Atlantic University, FL. (1979–1980) and San Francisco State University, CA. (1978–1979).

Dr. Soliman served also as Associate Professor of Electrical Engineering at Florida Atlantic University, U.S.A. (1980–1981).

He was a visiting scholar at the Technical University of Wien, Austria (Summer 1987) and at Bochum University, Germany (Summer 1985).

He was a Research Analyst at the Central Research, Rockwell Manufacturing Company, Pittsburgh, PA., U.S.A. (Summer 1970).

Dr. Soliman received the First Class Science Medal, from the President of Egypt in 1977, for his services to the field of Engineering and Engineering Education.