path and the parasitic node capacitances on the nodes with capacitors can also be absorbed by the corresponding circuit capacitances. However, the nonideal DO-OTA input and parasitic node capacitances related to the resistive nodes in the feedback path(s) in these circuits will cause an increase in the system order, a change influencing the filter characteristics in very high frequency designs. The DO-OTA output capacitances and conductances can cause parasitic zeros, especially the output impedance of the g_1 DO-OTA in Figs. 4(a) and 5(a)–(c). The output capacitances associated with the resistive nodes in Figs. 4(a)–(d) and 5(a) and (b) may also produce parasitic poles.

Using the single pole model $g(s) = g/(1+sT_b)$, where $\omega_b = 1/T_b$ is the finite bandwidth of the OTA, the effects of transconductance frequency dependence are formulated as

$$H'(s) = \frac{\omega_o^2}{s^4 T_{b1}T_{b2} + s^3(T_{b1}+T_{b2}) + s^2\left(1+\frac{T_{b2}\omega_o}{Q}\right) + s\frac{\omega_o}{Q} + \omega_o^2}$$

which indicates a shift from (12). Generally such effects increase with the number of DO-OTA's in the circuit, which should be considered when choosing a filter structure.

III. Conclusion

A number of novel current-mode continuous-time two integrator loop DO-OTA-C filter architectures have been developed. The various features of the structures have been discussed and compared. Unlike conventional OTA-C filters which are based on voltage integrators and amplifiers, the new DO-OTA-C realizations are based on current integrators and amplifiers. Between some voltage-mode OTA-C and current-mode DO-OTA-C filters an adjoint circuit relationship [14], [15] may exist. Among other correspondence relations, a differential input and single output OTA in the voltage-mode circuit may correspond to a differential output and single input OTA in the current-mode counterpart. Practical implementation of the proposed architectures are currently being investigated.

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A Novel CMOS Current Conveyor Realization with an Electronically Tunable Current Mode Filter Suitable for VLSI

Hassan O. Elwan and Ahmed M. Soliman

***Abstract*—A novel CMOS realization of the second generation current conveyor is given. A circuit which compensates the voltage offset due to channel length modulation effect is then developed. The CCII is then used to realize a new electronically tunable low-pass–band-pass filter suitable for VLSI. Simulation results taking the second-order effects into account indicate the excellent performance of both the CCII circuit and the filter over a wide dynamic range.**

I. Introduction

The second generation current conveyor (CCII) was first introduced by Sedra and Smith in 1970 [1]. The CCII is a versatile analog device which is used to implement many analog signal processing functions [2], [3]. Recently a MOS realization of the CCII which is suitable for VLSI has been reported [4] The purpose of this brief is to give a new MOS realization for the CCII with a wide operating range. Voltage offset resulting from the channel length modulation effect is then compensated by using a suitable dynamic biasing circuit. The current conveyor is then used to realize a new electronically tunable second-order current mode low-pass–band-pass filter employing only grounded elements such that the entire filter circuit can be easily integrated on one chip. Finally the circuit is modified to realize a voltage conveyer which is another useful building block [5].

II. The New CCII Circuit Realization

The CCII+ is a three terminal analog block with a describing matrix of the form

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad (1)$$

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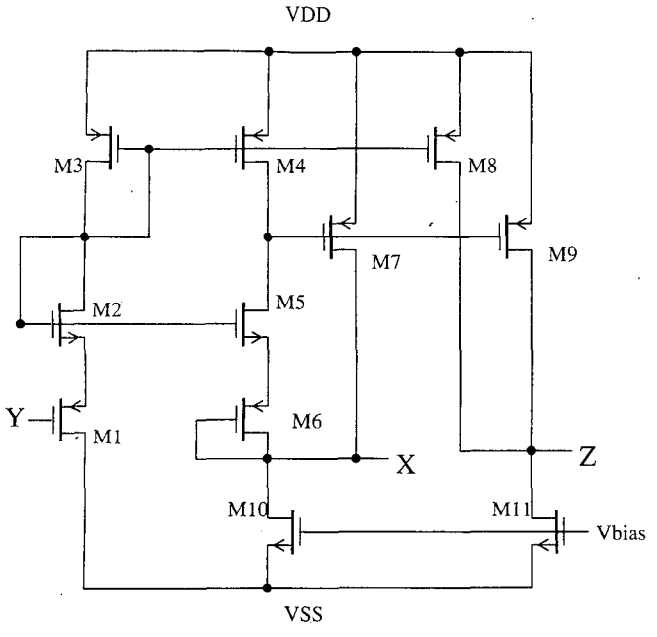
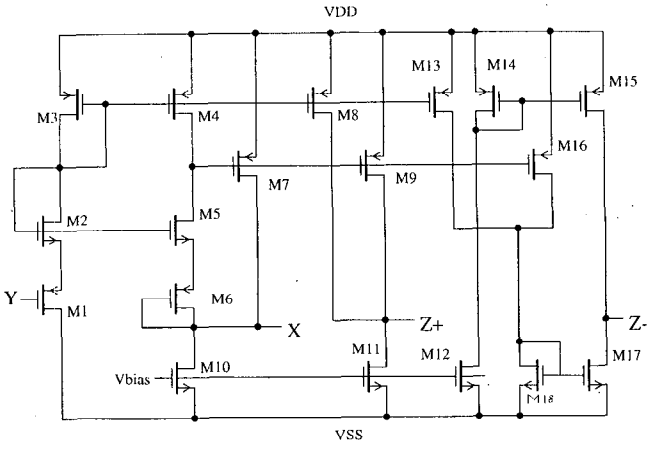


(a)



(b)

Fig. 1. (a) The current conveyor circuit. (b) The CCII+ and CCII− circuit realization.

The proposed MOS realization for the CCII+ is shown in Fig. 1(a).

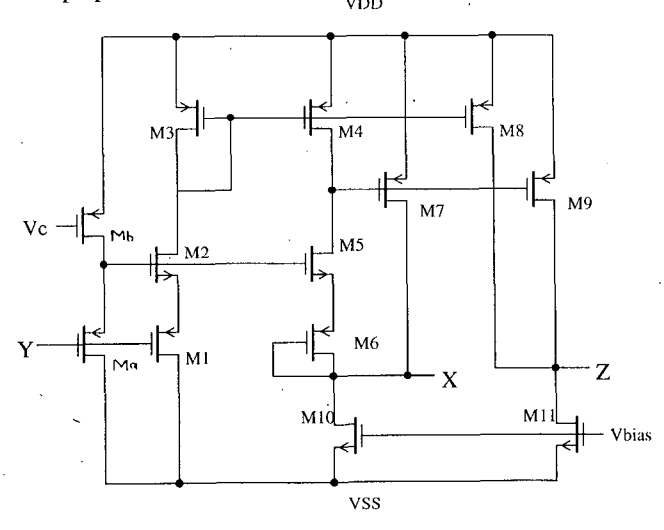
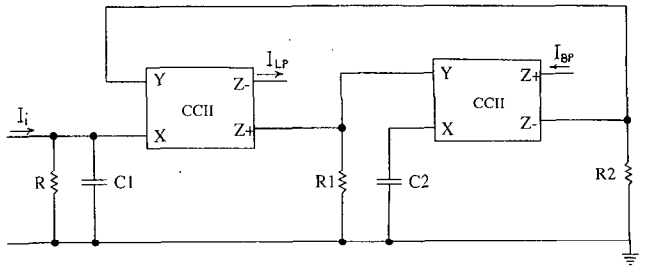
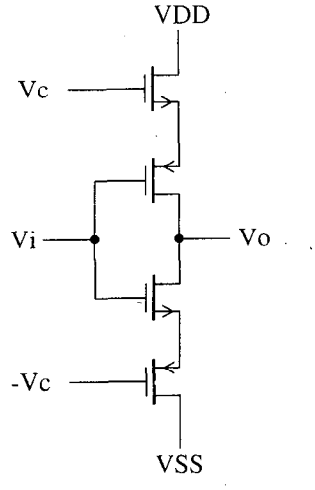


Fig. 2. The compensated current conveyor circuit.



(a)



(b)

Fig. 3. (a) The current mode low-pass band-pass filter. (b) The tunable transconductance used to realize the grounded resistor.

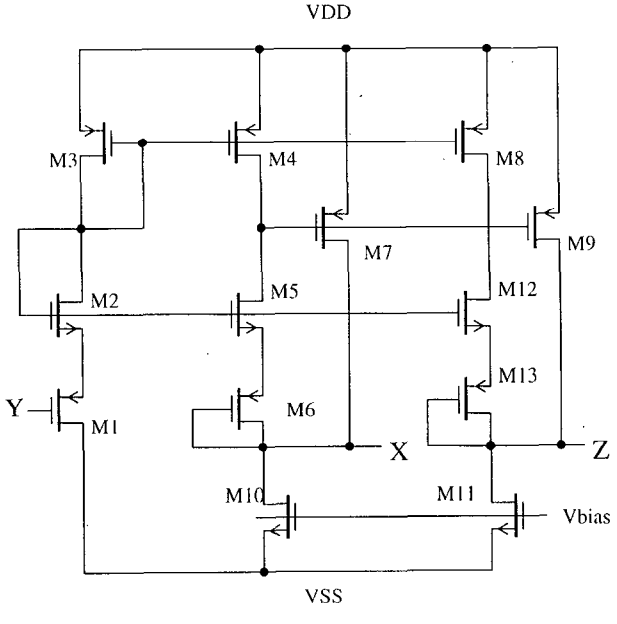


Fig. 4. The voltage conveyor circuit.

All transistors are assumed to be operating in the saturation region with their sources connected to the bulk/substrate. The Y terminal voltage is applied to the gate of transistor M1 which together with M2 forms a CMOS pair [6]. The current through this pair is mirrored by M3 and M4 to the CMOS pair formed by M5 and M6 and since

TABLE I
SPICE PARAMETERS

```
.MODEL NENH NMOS (LEVEL=2 VTO=0.9 KP=8.0E-05 GAMMA=1.1 PHI=0.6
+ LAMBDA=.01 RD=40 RS=40 PB=0.7 CGSO=4E-10 CGDO=4E-10 NEFF=5
+ CGBO=5E-10 RSH=25 CJ=.00044 MJ=0.5 CJSW=4E-10 MJSW=0.3 JS=1E-05
+ TOX=5E-08 NSUB=1.7E+16 TPG=1 UO=775 UEXP=0.1 UTRA=0.3
+VMAX=110000)

.MODEL PENH PMOS (LEVEL=2 VTO=-0.9 KP=4.0E-05 GAMMA=0.6 PHI=0.6
+ LAMBDA=.01 RD=39 RS=39 PB=0.6 CGSO=3.5E-10 CGDO=3.5E-10
CGBO=5E-10
+ RSH=80 CJ=.00015 MJ=.6 CJSW=4E-10 MJSW=0.6 JS=1E-05 TOX=5E-08
+ NSUB=5E+15 UO=250 TPG=-1 UEXP=0.1 UTRA=0.3 VMAX=80000 NEFF=5)
```

the gate voltage of M5 and M2 are the same, therefore, $V_x = V_y$. The negative feedback operation of the transistor M7 with the bias current I_B flowing through transistor M10 insures that the voltage V_x remains independent of the current withdrawn from the X terminal. This current is conveyed to the Z terminal by the mirroring action of transistors M4, M8 and M7, M9 and the bias current through M11. This current can be mirrored in an inverting manner if additional current mirrors are used. Thus both I_X and $-I_X$ can be produced by the circuit hence both the CCII+ and the CCII− can be realized simultaneously by the same circuit as shown in Fig. 1(b).

III. VOLTAGE OFFSET COMPENSATION

The previous analysis of the circuit operation neglects the second-order effects which causes small voltage offsets between the X and the Y terminals of the CCII..This offset is mainly due to the channel length modulation effect. Although this offset voltage is small, a circuit is developed to compensate this offset voltage. The current equation in the saturation region taking the channel length modulation into account is given by

$$I = \frac{K}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{2}$$

where $K = \mu C_{ox}(W/L)$ and λ is the channel length modulation parameter. Therefore the two equal currents through transistors M2 and M1 are given by

$$I_n = \frac{K_n'}{2}(V_{Gn} - V_{Sn} - V_{Tn})^2 \tag{3}$$

$$I_p = \frac{K_p'}{2}(V_{Sn} - V_y - |V_{Tp}|)^2 \tag{4}$$

where

$$K_n' = K_n[1 + \lambda(V_{Dn} - V_{Sn})] \tag{5}$$

$$K_p' = K_p[1 + \lambda(V_{Sn} - V_{SS})]. \tag{6}$$

Therefore the current I_1 in the transistors M2 and M1 is given by [6],[7]:

$$I_1 = \frac{K_{\text{eff}1}}{2}(V_{Gn} - V_y - V_{T\text{eff}})^2 \tag{7}$$

where

$$K_{\text{eff}1} = \frac{K_n' K_p'}{(\sqrt{K_n'} + \sqrt{K_p'})^2} \quad \text{and} \quad V_{T\text{eff}} = V_{Tn} + |V_{Tp}|. \tag{8}$$

TABLE II

Transistors	Aspect ratio $\frac{W\mu_m}{L\mu_m}$
M1,M6	16/2
M2,M5	2/4
M3,M4,M8	20/2
M7,M9	16/2

Assuming that the current mirror has an error of ϵ. The current I_1 will be mirrored to the M5 and M6 CMOS pair as I_2 which is given by

$$I_2 = \epsilon I_1. \tag{9}$$

Similarly, the current I_2 is obtained as

$$I_2 = \frac{K_{\text{eff}2}}{2}(V_{Gn} - V_x - V_{T\text{eff}})^2. \tag{10}$$

Therefore from (7), (9), and (10) the voltage offset between the X and the Y terminals is given by

$$\Delta V = V_y - V_x \tag{11}$$

$$\Delta V = (V_{Gn} - V_y - V_{Teq})\left(\sqrt{\frac{\epsilon K_{\text{eff}1}}{K_{\text{eff}2}}} - 1\right). \tag{12}$$

The above equation indicates that the offset voltage will depend on V_y. Although this error is small it can be easily compensated and made nearly independent of V_y if a circuit is used to dynamically bias the gate of transistor M2 such that

$$V_{Gn} = V_B + V_y. \tag{13}$$

The error in this case is given by

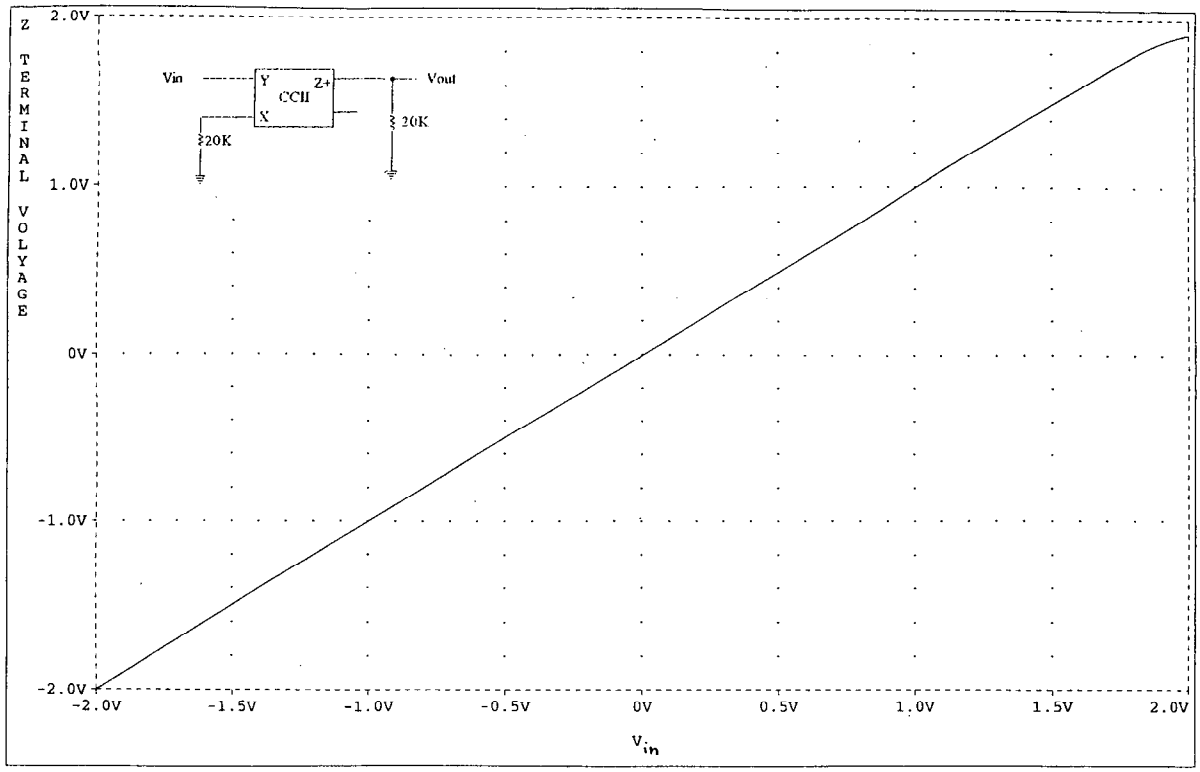
$$\Delta V = (V_B - V_{T\text{eff}})\left(\sqrt{\frac{\epsilon K_{\text{eff}1}}{K_{\text{eff}2}}} - 1\right). \tag{14}$$

Thus by adding the two matched transistors Ma and Mb as shown in Fig. 2 the gate voltage of transistor M2 is given by

$$V_{Gn} = (V_{DD} - V_C) + V_y \tag{15}$$

and hence by adjusting the control voltage V_c the voltage offset between the X and the Y terminals can be easily compensated.

Simulation results showing that the originally small offset voltage is compensated by the circuit shown in Fig. 2 is given in Section VI.



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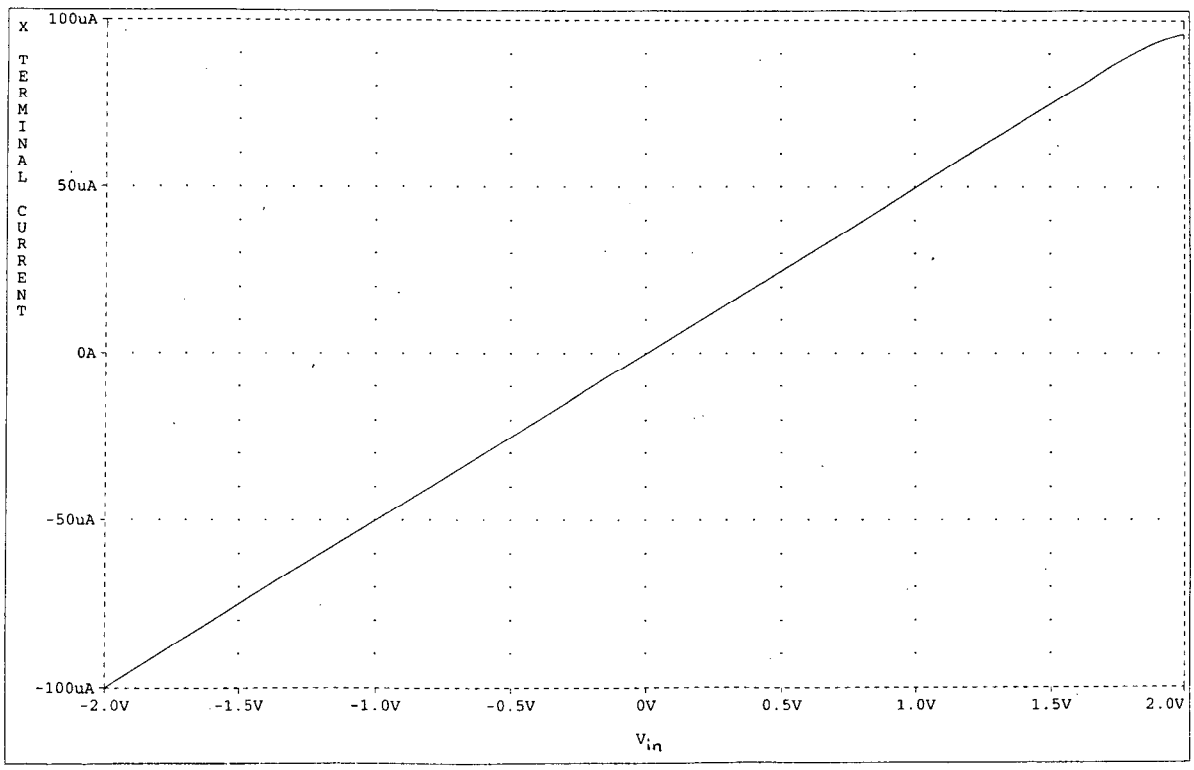
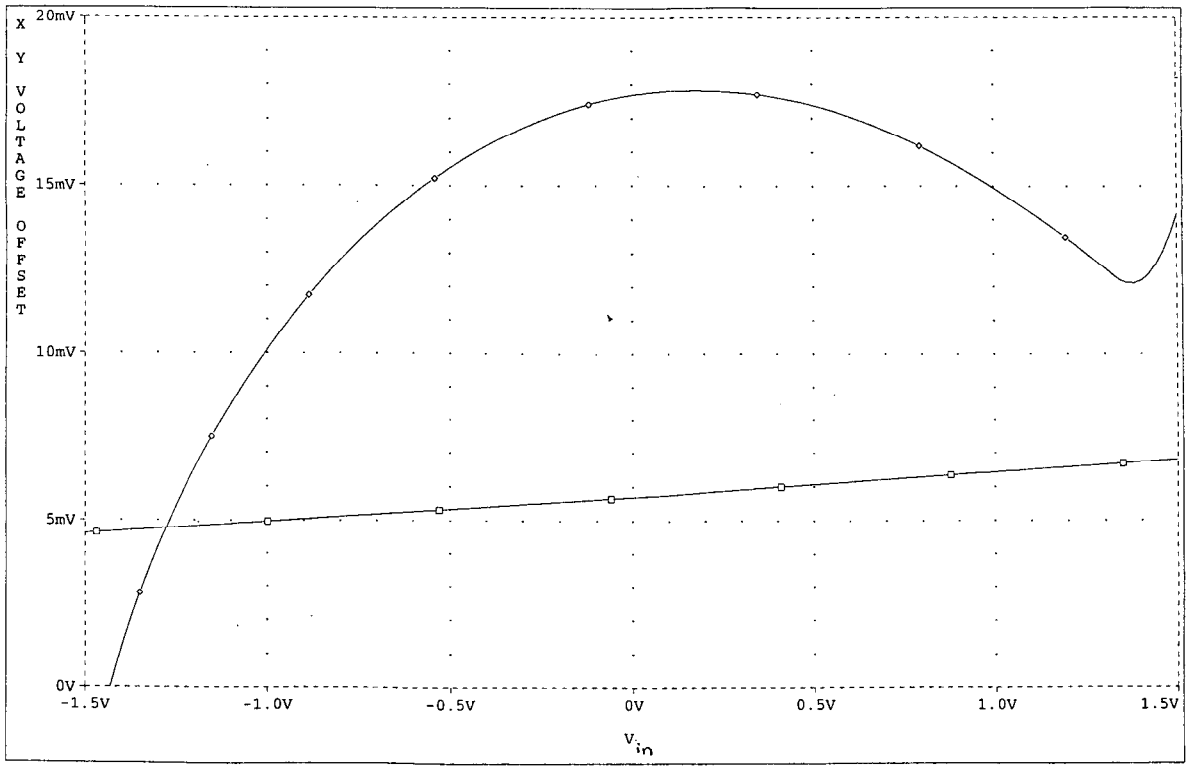


(b)

Fig. 5. (a) The Z terminal voltage when the CCII is used as a unity gain amplifier. (b) The current from the X terminal when the CCII is used to realize a unity gain amplifier.



(c)

Fig. 5. *(Continued.)* (c) The voltage offset between the X and Y terminals with and without the compensating circuit.

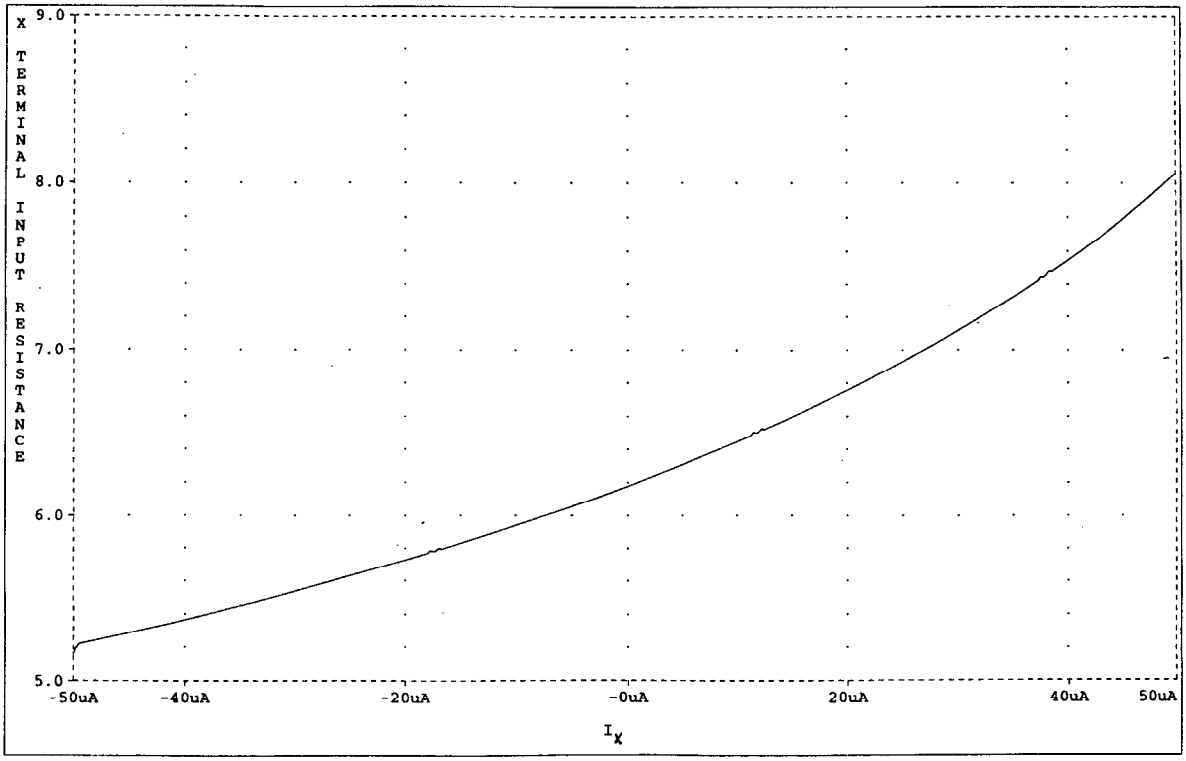
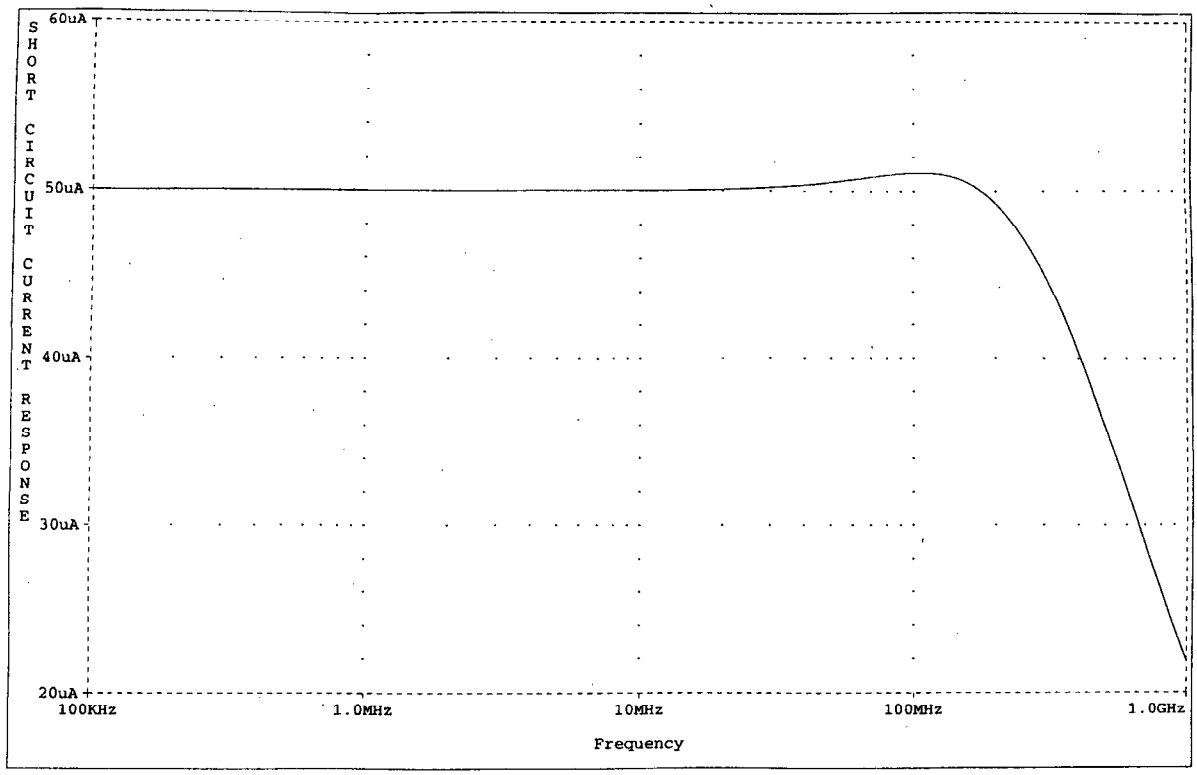
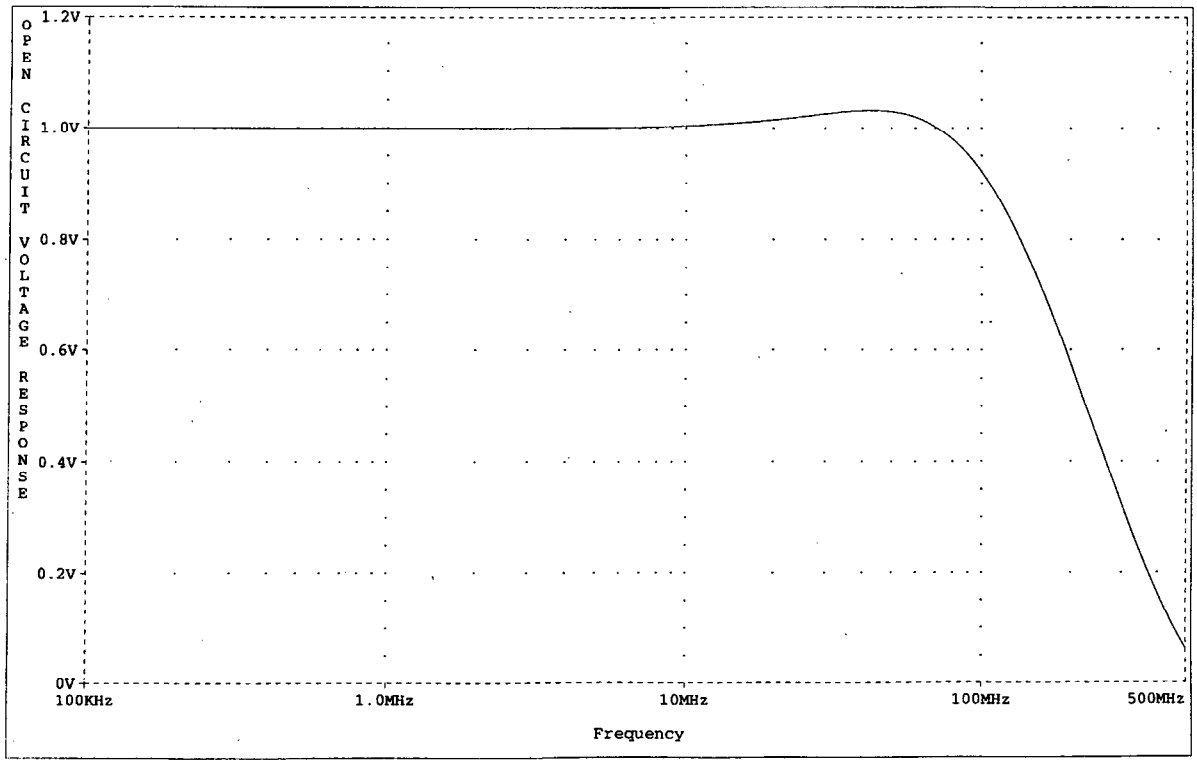


Fig. 6. The X terminal input resistance versus I_X.

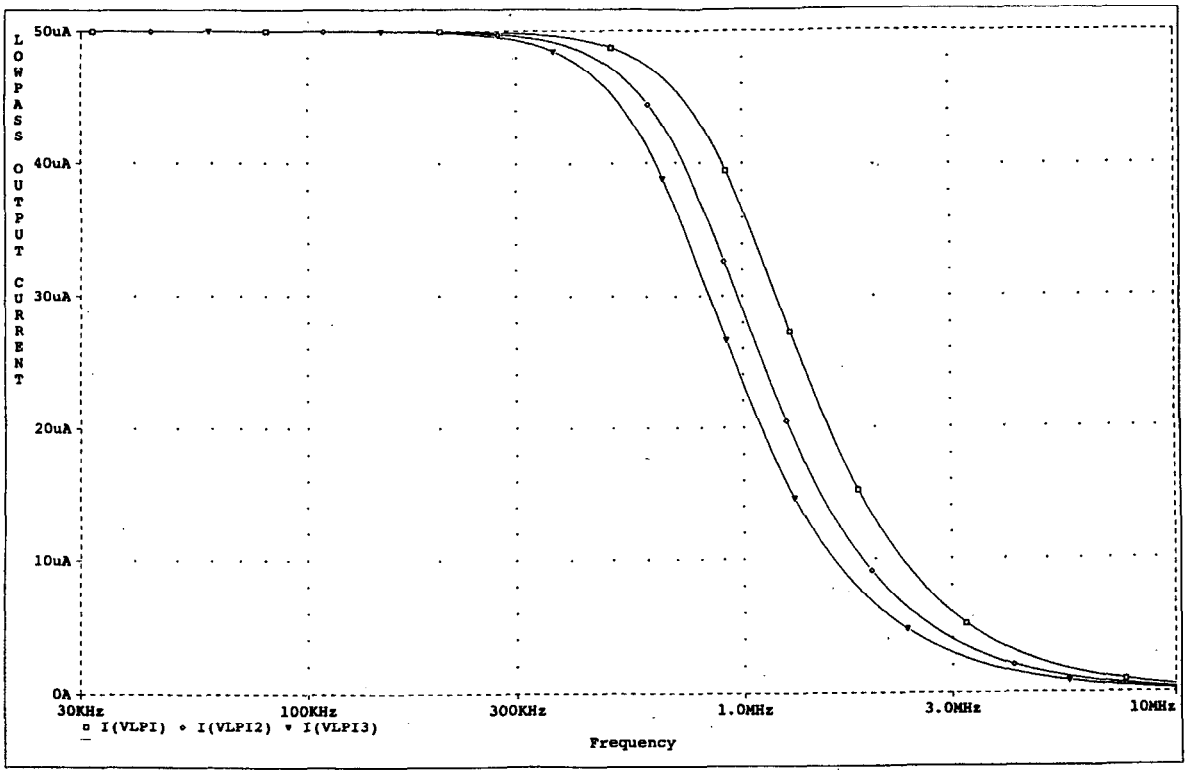


(a)

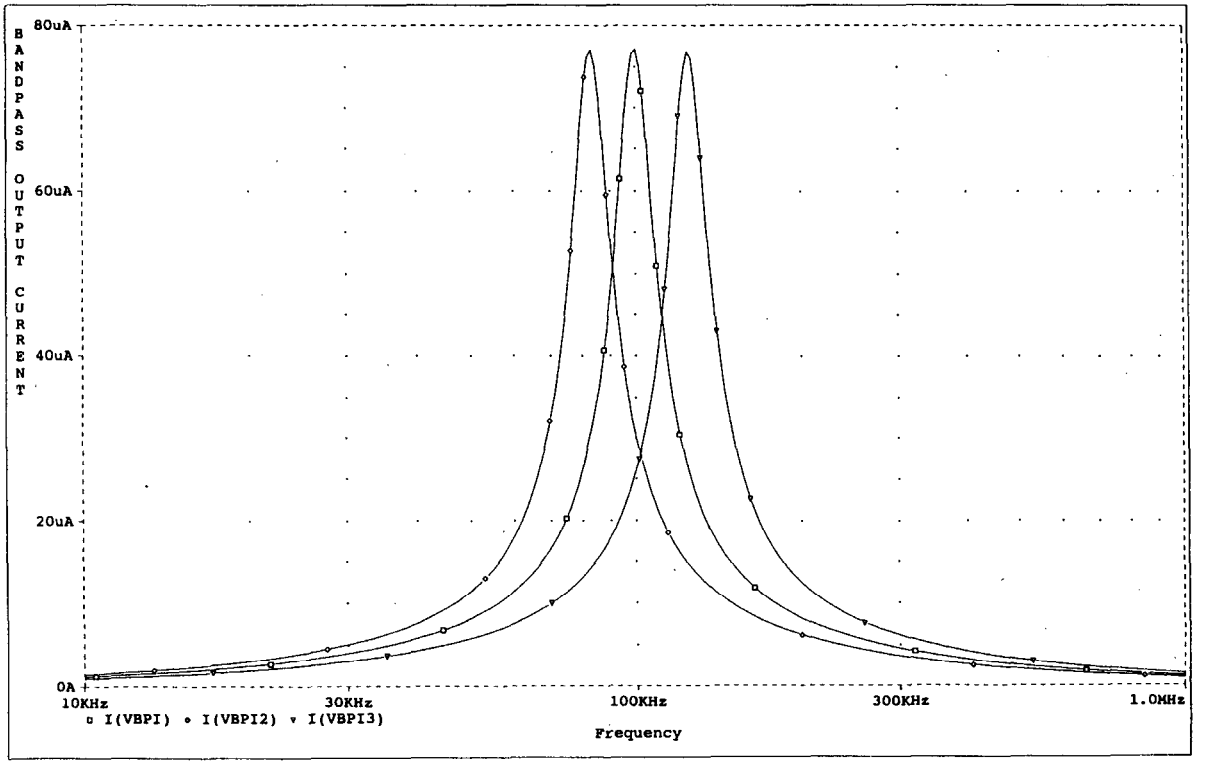


(b)

Fig. 7. (a) The short circuit output current from the Z terminal versus frequency. (b) The open circuit X terminal voltage versus frequency.



(a)



(b)

Fig. 8. (a) The electronically tuned low-pass response of the current mode filter. (b) The electronically tuned band-pass response of the current mode filter.

IV. A New Electronically Tunable Filter Realization Suitable for VLSI

A number of low-pass–band-pass current mode filters employing the CCII have been suggested [5], [8] however most of these realizations employ floating capacitors and resistors which require a large area to be implemented by MOS transistors. However the suggested structure for the second-order tunable filter shown in Fig. 3(a) employs only grounded resistors which are much easier to implement. A number of realizations of the tunable grounded resistors exist [9], [10].The transconducter [6] shown in Fig. 3(b) has been used in realizing the resistors in the filter circuit. The resistor is obtained by shorting the input and output terminals of the voltage tuned transconducter. The resistor value is given by

$$R = \frac{1}{2K_{eq}(V_c - V_{Tn} - |V_{Tp}|)}. \tag{16}$$

The low-pass and band-pass current transfer functions are given by

$$\frac{I_{LP}}{I_i} = \frac{\dfrac{1}{C_1C_2R_1R_2}}{s^2 + \dfrac{S}{C_1R} + \dfrac{1}{C_1C_2R_1R_2}} \tag{17}$$

$$\frac{I_{BP}}{I_i} = \frac{\dfrac{S}{C_1R_2}}{s^2 + \dfrac{S}{C_1R} + \dfrac{1}{C_1C_2R_1R_2}}. \tag{18}$$

The ω_o and Q are given by

$$\omega_o = \frac{1}{\sqrt{C_1C_2R_1R_2}}, \quad Q = R\sqrt{\frac{C_1}{C_2R_1R_2}} \tag{19}$$

and the center frequency gain is given by

$$T(j\omega_o) = \frac{R}{R_2}. \tag{20}$$

V. Realization of the Voltage Conveyor

The MOS circuit realizing the CCII can be easily modified to realize a voltage conveyor as well. The voltage conveyor has a describing matrix of the form

$$\begin{bmatrix} I_y \\ V_x \\ V_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ I_z \end{bmatrix}. \tag{21}$$

The difference between the current and voltage conveyors is that the latter conveys the voltage on the X terminal to the Z terminal instead of conveying the current. The voltage conveyor circuit is shown in Fig. 4, where the transistor topology which is used to realize the X terminal is repeated to realize the Z terminal, hence the voltage on the Y terminal is conveyed to both the X and the Z terminals.

VI. Simulation Results

SPICE simulations for both the CCII circuit as well as the proposed filter have been carried out. These simulations take into account second-order effects like the channel length modulation and the mobility degradation. SPICE parameters used are given in Table I. The transistors aspect ratios are given in Table II and the supply voltages are adjusted to $V_{DD} = 5$ V and $V_{SS} = -5$ V.

Fig. 5(a) and (b) shows the voltage at the Z terminal and the current at the X terminal when the CCII is used as a voltage amplifier with a unity gain. The voltage offset between the X and the Y terminals due to second-order effects with and without the compensation circuit are given in Fig. 5(c), the control voltage used is $V_c = 2.75$ V. The compensated circuit offset voltage is seen to be nearly constant.

The input resistance from the X terminal is 50 Ω for the uncompensated CCII, and less than 10 Ω when the compensation circuit is used. Fig. 6 gives the variation of this input resistance with the current withdrawn from the X terminal. The output resistance from the Z terminal is larger than 500 KΩ. The THD was less than 0.06% at 100 KHZ and 3 V peak to peak sinusoidal input.

Fig. 8(a) shows the low-pass current response of the filter given in Fig. 3(a) where the input current is 100 μ A (peak to peak) and electronic scanning is used to change the cutoff frequency by tuning the three equal resistors R, R_1 and R_2 from 2 KΩ to 3 KΩ. The capacitor values are $C_1 = 0.05$ nf and $C_2 = 0.1$ nf, in order to realize a Butterworth response.

The short circuit frequency response between the Z and X terminal currents and the open circuit frequency response between the Y and X terminal voltages are shown in Fig. 7(a) and (b) respectively.

Fig. 8(b) shows the bandpass current response when an input current of 40 μA (peak to peak) is used, the capacitor values are $C_1 = 1$ nf and $C_2 = 0.4$ nf. The grounded resistors are adjusted such that $R_1 = R_2 = R/4 = r$. The center frequency is then scanned by electronically tunning the value of r from 2 KΩ to 3 KΩ.

VII. Conclusion

A novel CMOS realization of the second generation current conveyor is given the circuit is then modified to compensate the voltage offset resulting from second- order effects and to reduce the input resistance of the X terminal. A new electronically tunable current mode low-pass–band-pass filter application utilizing the CCII circuit is given. The filter employs only grounded resistors and capacitors hence can be integrated on one chip. Simulation results confirm the excellent performance of both the CCII and the current mode filter.

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