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PARASITIC-CAPACITANCE-INSENSITIVE VOLTAGE-MODE MOSFET-C FILTERS USING DIFFERENTIAL CURRENT VOLTAGE CONVEYOR*

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Abstract. A new CMOS realization of the differential current voltage conveyor (DCVC) is introduced. The properties of the DCVC are shown to be suitable for very large-scale integration applications employing metal oxide semiconductor transistors operating in an ohmic region. A novel voltage-mode integrator is introduced. Detailed analysis of the parasitic capacitances is included. Voltage-mode continuous-time filters that benefit from the current processing capabilities at the input terminals of the DCVC are presented. Self-compensation of the proposed circuits is also presented. The effectiveness of the proposed circuits is demonstrated through HSPICE simulations based on the AMI 1.2μm N-well level 3 parameters.
Key words: Active Filters, MOSFET-C, Tow Thomas biquad, universal filter.

1. Introduction

Recently current-mode analog integrated circuits in CMOS technology have received much interest. Current-mode techniques can achieve considerable improvement in amplifier speed, accuracy, and bandwidth [11]. Traditionally, most analog signal processing operations have been accomplished employing the voltage as the signal variable. To maintain compatibility with existing voltage processing circuits, it is necessary to convert the input and output signals of a current-mode signal processor to voltage using transconductors. However, this has the disadvantage of increasing both the chip area and power dissipation.

This paper explores implementing fully integrated MOSFET-C voltage-mode

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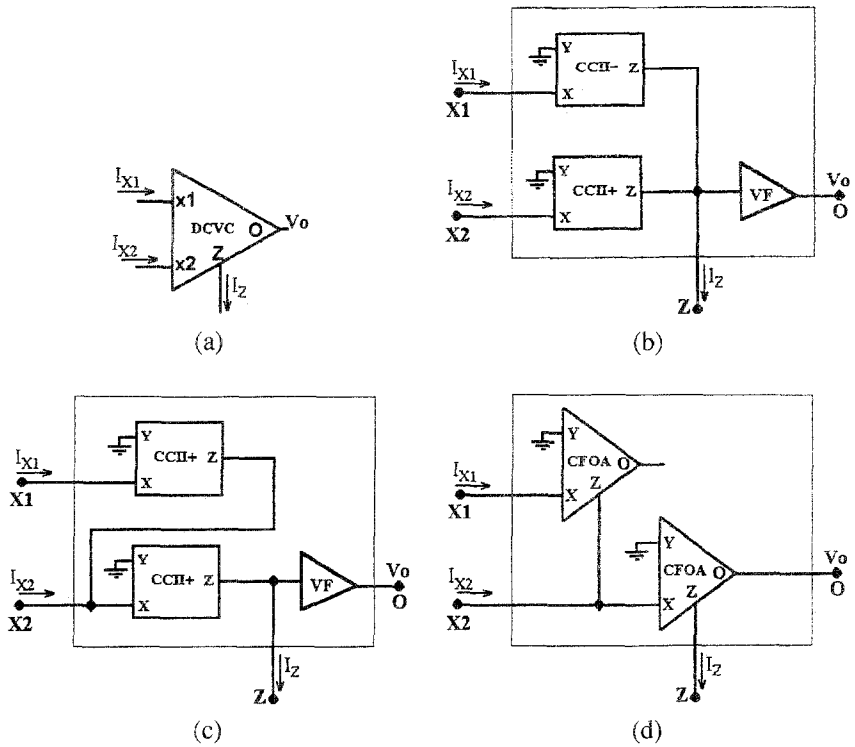

Figure 1. (a) DCVC symbol; (b) DCVC implementation using CCII+, CCII−, and Voltage Follower (VF); (c) DCVC implementation using CCII+ and VF; (d) DCVC implementation using CFOAs.

continuous-time filters using the differential current voltage conveyor (DCVC), keeping compatibility with existing signal processing circuits and taking advantage of the DCVC current-mode characteristics [1], [9], [10]. Also because the DCVC is not slew limited in the same fashion as operational amplifiers, it can provide amplification of high-frequency signals with the ease of using standard operational amplifiers in addition to a constant bandwidth virtually independent of the gain, as shown in Section 4.

The DCVC is a new, versatile, four-terminal analog building block represented symbolically as shown in Figure 1a. It is characterized by the following set of equations:

$$V_{X1} = V_{X2} = 0 \tag{1}$$

$$I_Z = I_{X1} - I_{X2} \tag{2}$$

$$V_O = V_Z. \tag{3}$$

2. The proposed DCVC

Few recent CMOS realizations have been suggested to implement the DCVC [9], [10]. The DCVC can be implemented using existing analog building blocks. It can be implemented using one CCII+, one CCII−, and a voltage follower, as shown in Figure 1b, or two CCII+ and a voltage follower, as shown in Figure 1c, or two current feedback op-amps (CFOAs), as shown in Figure 1d. A CMOS realization based on a differential current conveyor (DCC) [7] followed by a voltage buffer, shown symbolically in Figure 2a, is presented in Figure 2b. The performance of the proposed circuit was verified by HSPICE simulations, with supply voltages of ±2.5 V. Through the action of current mirrors formed from transistors M1, M2, M3, and M4, and assuming all transistors working in the saturation region,

$$I_6 = I_7 = I_5. \tag{4}$$

Thus

$$V_{gs6} = V_{gs7} = V_{gs5}, \tag{5}$$

and because

$$V_{g6} = V_{g7} = V_{g5}, \tag{6}$$

then substituting from equation (6) into equation (5),

$$V_{X1} = V_{X2} = V_{s5} = 0. \tag{7}$$

Also,

$$I_Z = I_{11} - I_{15}, \tag{8}$$

and because

$$I_{11} = I_{10}; \qquad I_{15} = I_9 = I_8; \qquad I_{12} = I_{13} \tag{9}$$

$$I_8 = I_{12} - I_6 - I_{X1} \tag{10}$$

$$I_{10} = I_{13} - I_7 - I_{X2}, \tag{11}$$

then substituting from equations (9), (10), and (11) into equation (8),

$$I_Z = I_{X1} - I_{X2}. \tag{12}$$

Through the action of the current mirror formed from transistors M20 and M21,

$$I_{18} = I_{19}. \tag{13}$$

Thus

$$V_{s18} = V_{s19}, \tag{14}$$

and because

$$I_{16} = I_{17}, \tag{15}$$

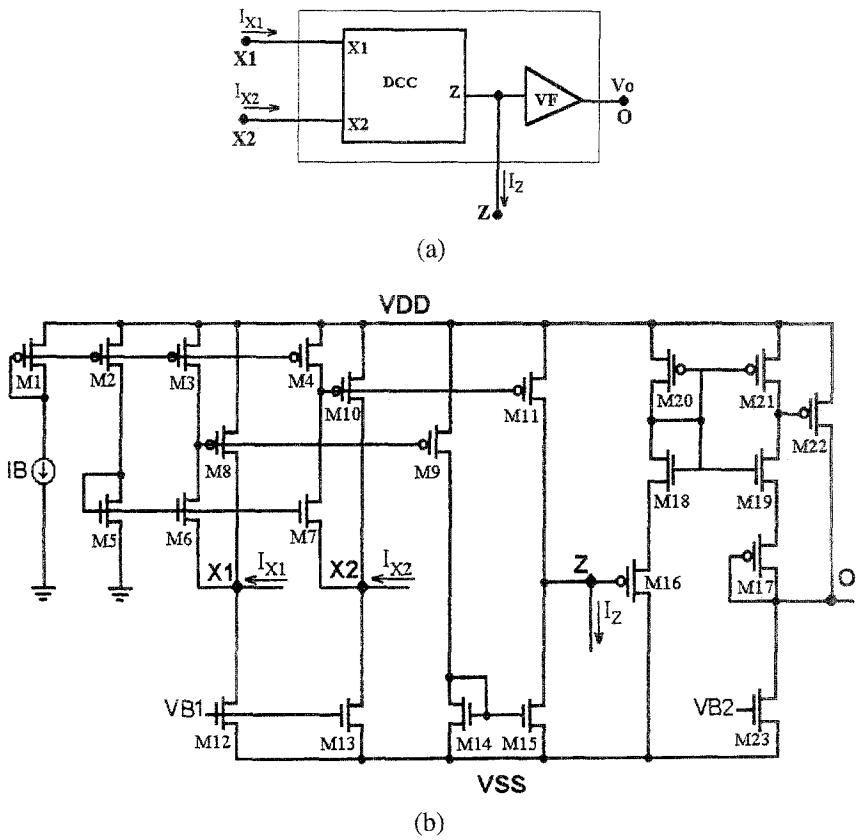

Figure 2. (a) DCVC implementation using DCC and VF; (b) Proposed CMOS realization of DCVC.

then

$$V_{sg16} = V_{sg17}. \tag{16}$$

Substituting from equation (14) into equation (16),

$$V_O = V_Z. \tag{17}$$

The previous analysis did not include the effect of the channel length modulation. Such an effect can be reduced by properly sizing the transistors and produces a second-order effect. On the other hand, it can be shown that mismatches in the threshold voltage due to the body effect in the input stage do not have any effect on the offset voltage as shown in the Appendix.

The main advantage of the DCVC is its ability to implement different analog circuits without the need of resistors, because it can be used to cancel both the even and odd nonlinear terms associated with MOS transistors operating in the

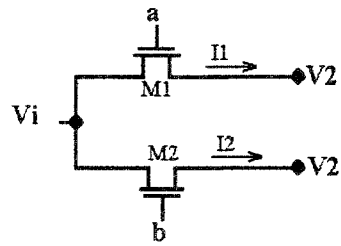

Figure 3. Nonlinearity cancelation in MOS transistors.

ohmic region [5]. The two NMOS transistors M1 and M2, shown in Figure 3, are assumed to be matched and operating in the ohmic region. The current in that region is given by

$$I = K_n(V_G - V_T)(V_D - V_S) + a_1(V_D^2 - V_S^2) + a_2(V_D^3 - V_S^3) + \cdots \quad (18)$$

Because the transistors M1 and M2 have equal drain and equal source voltages, both the even and odd nonlinearities are canceled by subtraction,

$$I_1 - I_2 = G(V_i - V_2), \quad (19)$$

where

$$G_i = \mu_n C_{ox} \frac{W}{L}(V_a - V_b). \quad (20)$$

Several methods have been developed to subtract the current of MOS transistors operating in the ohmic region. In the following sections, the input terminals of the DCVC are used to achieve the subtraction operation, producing circuits working in voltage mode that benefit from the current processing capabilities at the input terminals. In addition, positive and negative values of the conductance G can be achieved through appropriate choice of the gate control voltages V_a and V_b.

3. DCVC-based integrator

A new generalized voltage-mode integrator with all parasitic capacitances is shown in Figure 4. The proposed integrator employs a single grounded capacitor and can be tuned to achieve both ideal and lossy integration. For ideal operation, the transfer function is given by

$$\frac{V_o}{V_i} = \frac{G_1}{G_2} \frac{1}{(\frac{s}{\omega_o} + 1)}, \quad (21)$$

where

$$\omega_o = \frac{G_2}{C}. \quad (22)$$

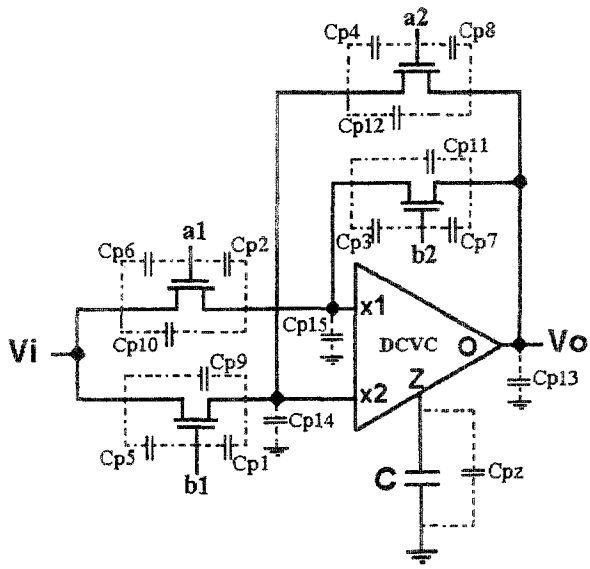

Figure 4. DCVC integrator with all-parasitic capacitances.

Thus ideal integration can be achieved by setting $G_2 = 0$, and by equating the gate control voltages V_{a2} and V_{b2}. Practically, this is equivalent to removing the two NMOS transistors in the feedback paths. Also, positive and negative integration can be achieved through appropriate choice of the gate control voltages V_{a1} and V_{b1}. Analysis of the effect of the parasitic capacitances is based on the method introduced in [3]. Because the voltage sources V_{a1}, V_{a2}, V_{b1}, and V_{b2} are dc sources, the effect of the capacitances C_{p1}, C_{p2}, C_{p3}, C_{p4}, C_{p5}, C_{p6}, C_{p7}, and C_{p8} will be negligible. The capacitances C_{p9}, C_{p10}, C_{p11}, and C_{p12} are drain-to-source capacitances of two matched NMOS transistors and are connected between equal potential nodes; thus, they cancel out. Also, because of the virtual grounded input terminals $X1$ and $X2$ and the low impedance output O of the DCVC, capacitances C_{p13}, C_{p14}, and C_{p15} have little effect. Thus response limitations incurred by capacitive time constants are eliminated because the low input impedance input terminals lead to circuits that are insensitive to stray capacitances [3], [4]. However, the DCVC suffers from a parasitic capacitance C_{pZ} at the Z terminal. Taking into consideration the effect of the parasitic capacitance C_{pZ}, equation (22) reduces to

$$\omega_o = \frac{G_2}{C(1 + \frac{C_{pZ}}{C})}. \tag{23}$$

Thus the integrating capacitor C is chosen much larger than C_{pZ} to eliminate its effect. It is also possible to compensate the effect of C_{pZ} by taking the design

value of C equal to its theoretical value minus C_{pZ}. Self-compensation can be achieved by using a capacitor $\acute{C}$, where

$$\acute{C} = C - C_{pZ}. \tag{24}$$

Thus the effect of C_{pZ} is absorbed in the integrating capacitance $\acute{C}$, and no additional elements for compensation are needed. Although the paracitic capacitance C_{pZ} is generally nonlinear, it can be linearized around the operating point. The variations in its value should be minimal because the input signals to be filtered are normally very small in magnitude so that filter structures can achieve high linearity. For practical purposes, this should be sufficient. For example, the implementation of the DCVC presented in Figure 1d will suffer from the paracitic capacitance at the Z terminal of the second CFOA, which is characterized to be 5.5 pF through measurements for the commercially available CFOA chip AD844 [6], [8]. Such a value is assumed to be constant during operation, and all passive compensation methods use such a nominal value. Nevertheless, more elaborate techniques using active compensation should be investigated to achieve full cancelation at any operating point.

4. DCVC-based amplifier

Amplifiers are one of the most commonly used analog building blocks in modern analog VLSI signal and information processing. Linear passive resistors consume a large chip area and suffer from the spread in their absolute values caused by random process variations and temprature. Thus the capability to electronically tune the resistance value is considered a big advantage. A direct application of the DCVC to implement a voltage-controlled voltage source (VCVC) is shown in Figure 5, where the output voltage is given by

$$\frac{V_o}{V_i} = \frac{G_1}{G_2} \frac{1}{(\frac{C_{pZ}}{G_2} s + 1)}. \tag{25}$$

Thus a single DCVC is capable of providing equal gain for both the inverting and noninverting inputs. It is also clear that a constant bandwidth virtually independent of the gain can be achieved by keeping the conductance G_2 constant while controlling the gain through the conductance G_1, as shown in Figure 6. Both features cannot be achieved using operational amplifiers. Assuming that the parasitic capacitance C_{pZ} magnitude is approximately constant, its effect can be completely canceled by connecting a capacitor of magnitude C_{pZ} between the output terminal O and the input terminal $X1$.

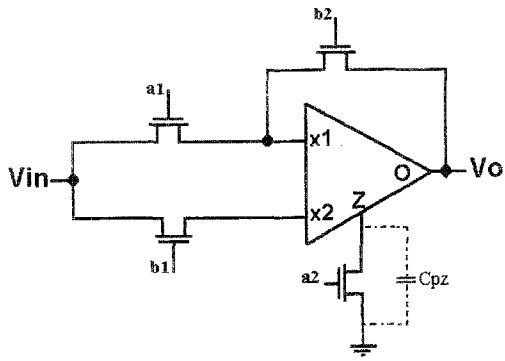

Figure 5. DCVC voltage-controlled voltage source with parasitic capacitance.

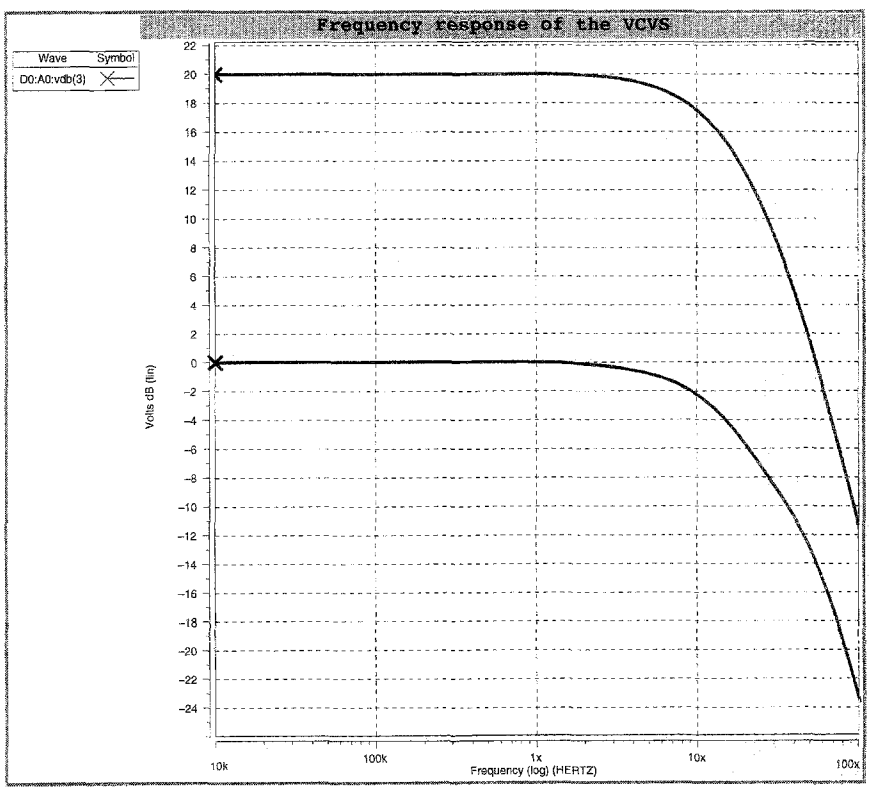

Figure 6. DCVC amplifier response with gain, $K = 1$ and 10.

5. Active filters using the DCVC

Continuous-time filters using operational amplifiers, transconductors, and switched capacitors are now widely accepted in industry where they are used in

applications involving direct signal processing, especially for medium dynamic range applications [11]. Usually two inverting integrators are cascaded, and a third inverter allows closing the overall loop with the proper phase. This idea is behind many of the biquad filter structures available. The active elements count in these structures could be reduced if a true noninverting integrator could be built with a single active element. Unfortunately, this cannot be done with single-input operational amplifiers but can be easily done using the DCVC. In addition, the availability of two virtual ground terminals at the input of the DCVC allows for summing currents leading to circuits with fewer active elements. The realization of the Tow Thomas (TT) biquad and a universal filter are introduced in the following sections.

5.1. The Tow Thomas biquad

Because the TT biquad depends on current summing by introducing a virtual ground at the input terminal of the conventional operational amplifier and on the availability of performing only inverting integration, three operational amplifiers are needed. On the other hand, because the DCVC does not suffer from these problems, the TT biquad can be implemented as shown in Figure 7 using only two DCVCs. Unlike the classical TT biquad implemented using three operational amplifiers, all possible polarities of the bandpass and lowpass outputs are summarized in Table 1. The transfer functions of the bandpass and lowpass outputs are given by

$$\frac{V_1}{V_i} = \frac{\frac{G_3 s}{C_1}}{D(s)} \tag{26}$$

$$\frac{V_2}{V_i} = \frac{\frac{G_3 G_2}{C_1 C_2}}{D(s)}, \tag{27}$$

where $D(s)$ is given by

$$D(s) = s^2 + \frac{G_4}{C_1} s + \frac{G_1 G_2}{C_1 C_2}. \tag{28}$$

Thus ω_o and Q are given by

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \tag{29}$$

$$Q = \frac{1}{G_4} \sqrt{\frac{C_2 G_1 G_2}{C_1}}. \tag{30}$$

For a lowpass response with a specified dc gain $|T(0)|$

$$G_3 = |T(0)| G_1. \tag{31}$$

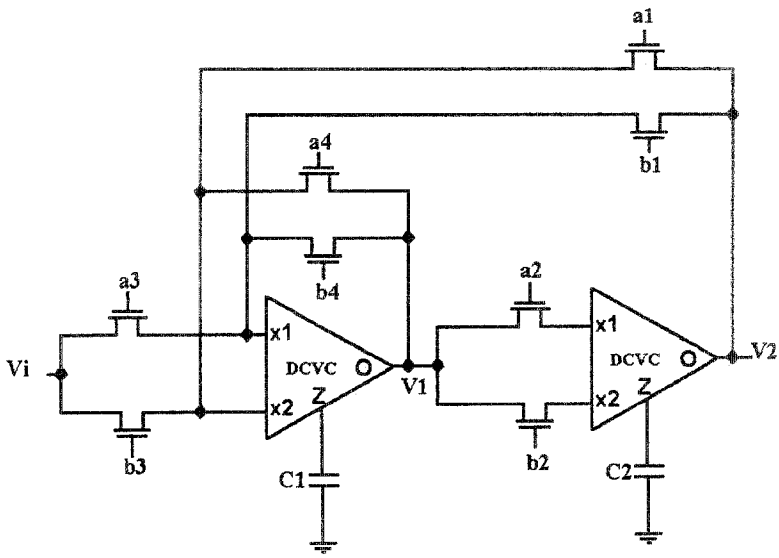

Figure 7. Tow Thomas biquad using DCVC.

Table 1. The four alternative response polarities of the TT biquad

G_i Polarity				Filter Response Polarity	
G_1	G_2	G_3	G_4	Bandpass	Lowpass
+	+	+	+	+	+
+	+	−	+	−	−
−	−	+	+	+	−
−	−	−	+	−	+

For a bandpass response with a specified center frequency gain $|T(j\omega_o)|$,

$$G_3 = |T(j\omega_o)|G_4. \tag{32}$$

It is clear from equation (28) that the quality factor Q can be independently controlled without affecting ω_o by varying G_4. Also, the conductance G_3 controls the filter gain without affecting either ω_o or Q. The TT biquad filter is self-compensated by absorbing the effect of the stray capacitance C_{pZ} presented in both C_1 and C_2, and no additional elements for compensation are needed. The TT circuit presented is very interesting because it can be easily converted into the quadrature oscillator presented in [10] by simply grounding the input source. Figure 8 represents the ideal, uncompensated, and compensated lowpass responses of the TT biquad designed to give a Butterworth response, where $C_1 = C_2 = 15$ pF, $G_1 = G_2 = G_3 = 35.5$ μA/V, and $G_4 = 50.2$ μA/V.

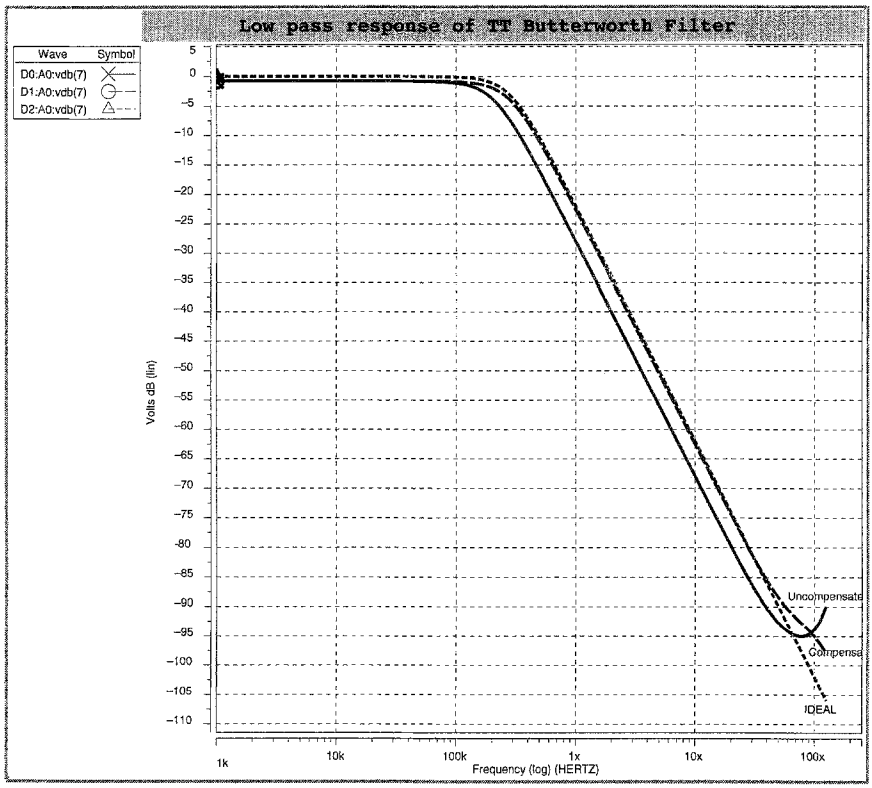

Figure 8. Ideal, uncompensated, and compensated Butterworth lowpass responses of TT biquad.

5.2. *Universal filter*

Universal filters constitute a fundamental second-order building block in many analog signal processing applications. Second-order universal filters are designed to provide lowpass, bandpass, highpass, allpass, and notch responses. A novel voltage-mode universal filter that uses a minimum number of active elements is presented in Figure 9. The transfer function is given by

$$\frac{V_o}{V_i} = \frac{\frac{C_3}{C_2}S^2 + \frac{G_4}{C_2}s + \frac{G_2G_3}{C_1C_2}}{s^2 + \frac{G_5}{C_2}s + \frac{G_1G_2}{C_1C_2}}, \tag{33}$$

where ω_o and Q are given by

$$\omega_o = \sqrt{\frac{G_1G_2}{C_1C_2}} \tag{34}$$

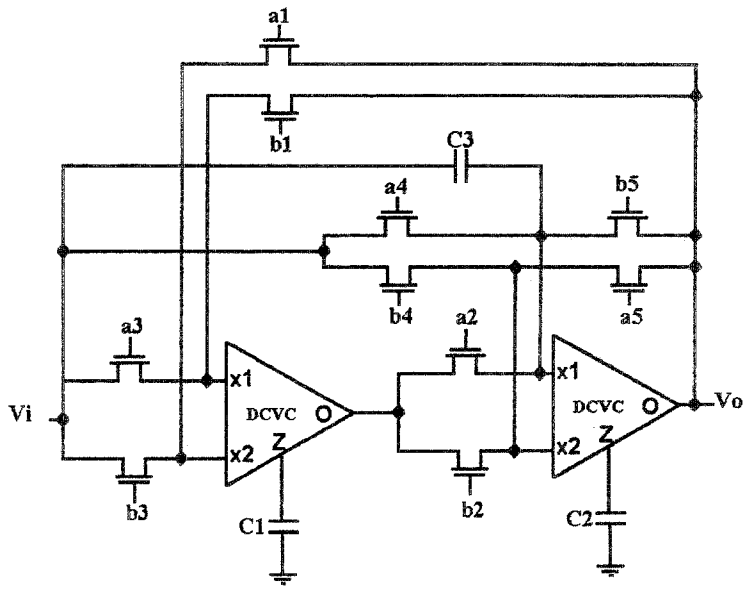

Figure 9. Universal filter using DCVC.

Table 2. Realizability conditions for the universal filter

Filter Response	Realizability Conditions
Highpass	$G_3 = G_4 = 0$
Bandpass	$G_3 = 0, C_3 = 0$
Lowpass	$G_4 = 0, C_3 = 0$
Allpass	$G_3 = G_1, G_4 = -G_5, C_3 = C_2$
Notch	$G_3 = G_1, G_4 = 0, C_3 = C_2$

$$Q = \frac{1}{G_5}\sqrt{\frac{C_2 G_1 G_2}{C_1}}. \tag{35}$$

It is clear that the quality factor Q can be independently controlled by varying G_5 without affecting ω_o. All possible outputs are summarized in Table 2. The proposed configuration is attractive in realizing higher-order transfer functions. Second-order sections based on the proposed universal filter can be cascaded to achieve an nth order using only n DCVCs. Again the proposed universal filter is self-compensated because the effect of the stray capacitance C_{pZ} can be absorbed in both C_1 and C_2. Figure 10 represents the magnitude and phase responses of a notch filter, where $C_1 = C_2 = C_3 = 10$ pF, $G_1 = G_2 = 47.4$ μA/V, and $G_3 = 67$ μA/V.

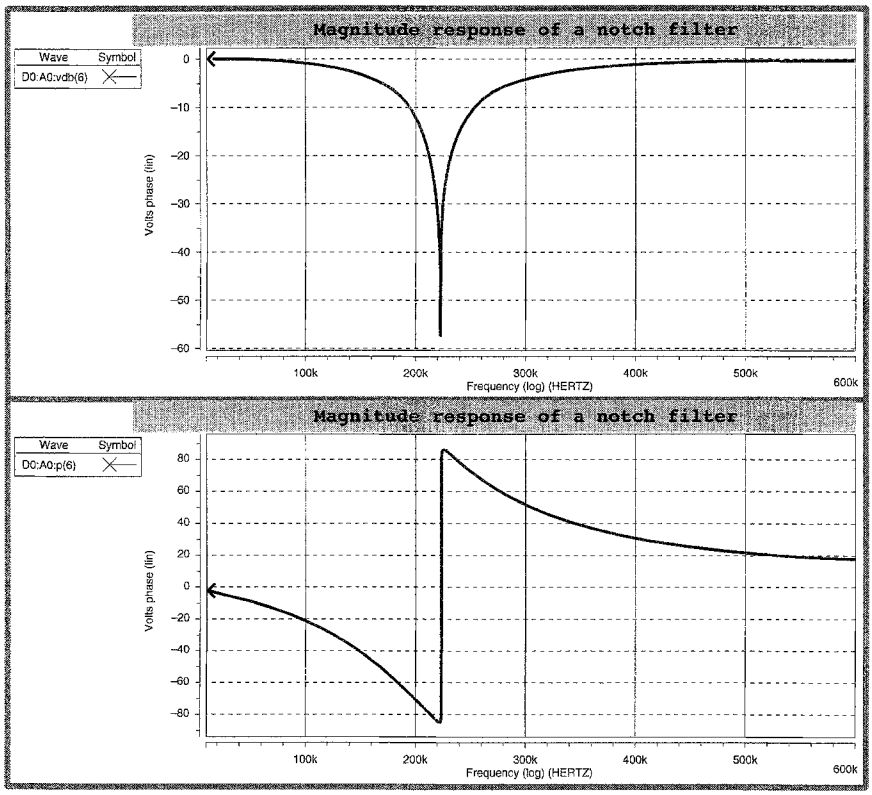

Figure 10. Magnitude and phase responses of a Notch filter.

6. Nonideal analysis

The nonidealities related to the voltage and current following operations of DCVC can be modeled by the following equations:

$$V_O = \beta(s)V_Z \tag{36}$$

$$I_Z = \alpha(s)(I_{X1} - I_{X2}), \tag{37}$$

where $\beta(s)$ and $\alpha(s)$ are the active nonidealities of the DCVC. They are approximated by the following single-pole transfer functions:

$$\beta(s) = \frac{\beta_o}{(1 + \frac{s}{p_v})} \tag{38}$$

$$\alpha(s) = \frac{\alpha_o}{(1 + \frac{s}{p_i})}. \tag{39}$$

Here, p_v and p_i are 3-dB cutoff frequencies of the voltage and current gains,

respectively. β_o and α_o represent the dc inaccuracies of these gains, and they can be expressed as $\beta_o = 1 - \epsilon_v$ and $\alpha_o = 1 - \epsilon_i$ with $|\epsilon_v| \ll 1$ and $|\epsilon_i| \ll 1$, where ϵ_v and ϵ_i denote the voltage and current tracking errors, respectively. Then the charactaristic equation reduces to

$$D(s) = s^2 + \frac{\omega_o}{Q\sqrt{\frac{\alpha_2(s)\beta_2(s)}{\alpha_1(s)\beta_1(s)}}}s + \omega_o^2\alpha_1(s)\alpha_2(s)\beta_1(s)\beta_2(s). \tag{40}$$

If we assume infinite values for p_i and p_v (i.e., they are frequency independent), then the actual natural frequency ω_{oa} and actual quality factor Q_a are given by

$$\omega_{oa} = \omega_o\sqrt{\alpha_1\alpha_2\beta_1\beta_2} \tag{41}$$

$$Q_a = Q\sqrt{\frac{\alpha_2\beta_2}{\alpha_1\beta_1}}. \tag{42}$$

The gain sensitivities of both the natural frequency and quality factor can be given by

$$S_{\alpha_1}^{\omega_{oa}} = S_{\alpha_2}^{\omega_{oa}} = S_{\beta_1}^{\omega_{oa}} = S_{\beta_2}^{\omega_{oa}} = \tfrac{1}{2} \tag{43}$$

$$S_{\alpha_2}^{Q_a} = S_{\beta_2}^{Q_a} = -S_{\alpha_1}^{Q_a} = -S_{\beta_1}^{Q_a} = \tfrac{1}{2}. \tag{44}$$

Let us now assume finite values for p_i and p_v and neglect all the other nonidealities. Assuming these nonidealities are the same for both DCVC, we make the following approximation:

$$\frac{1}{(1+\frac{s}{p_v})^2(1+\frac{s}{p_i})^2} \approx \frac{1}{(1+\frac{s}{p_{eq}})}, \tag{45}$$

where

$$p_{eq} = \frac{2}{p_v} + \frac{2}{p_i}. \tag{46}$$

Using Budak-Petrela's method [2], the following deviations can be deduced for the natural frequency and quality factor:

$$\frac{\Delta\omega_o}{\omega_o} \approx 0 \tag{47}$$

$$\frac{\Delta Q}{Q} \approx \frac{2Q^2}{\sqrt{4Q^2-1}}.\frac{\omega_o}{p_{eq}}. \tag{48}$$

Thus, the pole-Q increases for high-Q filters with high natural frequencies. Noted that this Q-enhancement effect, which may be expected, might cause instability problems for high-Q filters with high natural frequencies and limit the operational frequency range of the filter. Also note that, as in all the good active filters, the relative deviation of the natural freqency is zero.

7. Conclusions

A new realization of the differential current voltage conveyor (DCVC) is presented. The DCVC provides a constant bandwidth virtually independent of the gain. The main advantage of the DCVC is its ability to implement different analog circuits without the need of resistors, because it can be used to cancel both the even and odd nonlinear terms associated with MOS transistors operating in the ohmic region. Most of the parasitic capacitances are eleminated due to the virual grounds at the input terminals. The proposed applications employing this concept are MOS-C integrators, continuous-time filters, and oscillators. HSPICE simulations that confirm the theoretical analysis are included.

Appendix

Assuming that all transistors in Figure 2 are operating in the saturation region, the current of the NMOS transistors ignoring channel length modulation is given by

$$I_D = \frac{K_n}{2}(V_{gs} - V_T)^2, \tag{49}$$

where

$$V_T = V_{To} + \gamma(\sqrt{V_{sb} + 2\phi_f} - \sqrt{2\phi_f}). \tag{50}$$

Thus the expressions for the current in M5 and M6 are given by

$$I_5 = \frac{K_n}{2}(V_g - V_{s5} - V_{T5})^2 \tag{51}$$

$$I_6 = \frac{K_n}{2}(V_g - V_{s6} - V_{T6})^2. \tag{52}$$

Because $I_6 = I_5$ by the current mirroring action, the offset voltage is given by

$$\triangle V = V_{s6} - V_{s5}. \tag{53}$$

From the preceding equations, the offset voltage $\triangle V$ is obtained as

$$\triangle V = \gamma(\sqrt{V_{s5} - VSS + 2\phi_f} - \sqrt{V_{s6} - VSS + 2\phi_f + \triangle V}). \tag{54}$$

Thus the obvious solution is

$$\triangle V = 0. \tag{55}$$

Thus

$$V_{s6} = V_{s5} = 0 \tag{56}$$

and

$$V_{X1} = V_{s6} = 0. \tag{57}$$

Similary, the offset voltage at the other terminal $X2$ is also zero. Hence the circuit operation is independent of the threshold voltage variation due to the body effect.

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