Analytical synthesis of elliptic voltage-mode even/odd-nth-order filter structures using DDCCs, FDCCIIIs, and grounded capacitors and resistors

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Abstract: Despite the recent publication of the analytical synthesis of voltage-mode even/odd-nth-order differential difference current conveyor (DDCC) and fully differential current conveyor II (FDCCII)-grounded resistor and capacitor universal Butterworth/Chebyshev filter structures, an elliptic voltage-mode even/odd-nth-order DDCC and FDCCII-based filter structure is yet to be presented in the literature. Under the restriction of a finite order, the elliptic filter is better at meeting the stringent cut-off ratio of a very narrow transition band as compared to other kinds of filters, thus making the synthesis of such an elliptic filter to be extremely useful. In this study, one even-nth-order and two odd-nth-order elliptic filter structures are analytically synthesised using DDCCs and FDCCIIIs. The feasibility of such structures is validated through H-spice simulations on the proposed elliptic third-order low-pass and elliptic fourth-order low-pass, high-pass, band-pass, and band-reject filters.

1 Introduction

Active filters are broadly applied in the field of communication and signal processing, to almost all sophisticated electronic systems, such as radio, television, telephone, radar, space satellites, biomedical equipment, and so on. Active filters have proven to provide lowered disturbances, lower carbon dioxide emissions through improved energy efficiency, lower current consumption and increased production stability to name a few.

Over the last decade or so, numerous current conveyor-based second and higher-order filters have been presented [1–59]. Several nth-order filter syntheses through signal-flow graph approach have been reported [15–22]. A third-order all-pass (AP) filter [19, 21] was realised employing four second-generation current conveyors, three floating/grounded capacitors, and eight to nine floating/grounded resistors. The same third-order AP filter was realised in [22] with the aim of having all capacitors grounded, but still used five current feedback amplifiers, each of which is equivalent to a plus-type second-generation current conveyor followed by a voltage buffer, and ten floating/grounded resistors in addition to three grounded capacitors. It is apparent that too many active and passive components are utilised and need to be reduced. A new active element, extra-X second-generation current conveyor has been recently reported, and filters and other applications have emerged with simpler compact circuits using this device [23–25].

Just joining two current signals, current-mode (CM) addition and subtraction can be easily carried out. On the contrary, voltage-mode (VM) addition and subtraction need a hardware adder and subtractor, respectively, for realisation. Two recently reported active components, differential difference current conveyors (DDCCs) [26] and fully differential current conveyors (FDCCIIIs) [27] enjoy intrinsic voltage addition and subtraction produced from their input–output characteristics leading to more attractive synthesis of VM filters [8, 12–14, 16–24, 30–35, 41–46, 51–54, 59–65].

Several DDCC or/and FDCCII-based filters have been presented in the literature [14, 28–59]. A single FDCCII-based universal (i.e. low-pass (LP), high-pass (HP), band-pass (BP), band-reject (BR), and AP) biquad filter [14] with three inputs and a single output was reported using two grounded/floating capacitors and three grounded/floating resistors. Since the number of transistors in a DDCC is around half of that in an FDCCII, another universal biquad filter was reported [32] using two DDCCs instead of a single FDCCII in addition to the same number of passive elements as in [14]. To have all the passive components grounded, one more DDCC was added to realise a universal second-order filter [33, 34]. Recently, the three DDCCs have been replaced by two FDCCIIIs for the synthesis of a universal biquad filter [35]. The first DDCC-based nth-order universal filter structure [58] has been reported employing $n + 1$ DDCCs (including one super-large DDCC with $n + 2$ output terminals), $n$ grounded capacitors, and $n + 2$ grounded resistors. The super-large DDCC suffers from $n + 1$ (too many) stages of current mirrors which produce gradual incremental output errors and power dissipation. Therefore, an nth-order universal filter structure, employing one FDCCII (instead of the aforementioned super-large DDCC), $n − 1$ DDCCs, $n$ grounded capacitors and $n$ grounded resistors (the minimum number of passive components), was reported in [59]. The intrinsic addition and subtraction ability of DDCCs and FDCCIIIs were fully applied to the strategy of synthesis to generate the even/odd-nth-order VM universal filter structure. Based on the differences between the input voltage and (i) an nth-order HP signal, (ii) a conventional nth-order BR or notch signal, and (iii) an nth-order AP signal, a very systematic approach was presented to derive an nth-order universal filter structure, which can realise VM even/odd order LP, HP, BP, AP, and traditional notch filter transfer functions. An odd/ even nth-order notch transfer function was defined and realised using DDCC and FDCCIIIs.

The aforementioned filters are Butterworth/Chebyshev type filters. Nevertheless, it is well known that the narrowest transition band is a particularly strong point of elliptic approximations. It would take a maximally flat (Butterworth) function of order 25 and a Chebyshev filter of order eight to achieve the same narrow transition band of an elliptic fourth-order filter (see the Appendix). Hence, it is worth investigating and synthesising an elliptic VM even/odd-nth-order filter structure using DDCCs and FDCCIIIs.

In recent years, analytical synthesis methods have effectively demonstrated the realisation of even/odd-nth-order VM/CM filters.
and oscillators [31, 59–68]. In the synthesis process, a complicated nth-order transfer function is decomposed by a series of iterative algebraic operations, which meet the conditions of synthesis with respect to the input–output characteristics of the active components used, until a set of simple equations are generated, and then synthesised using simple integrators and a constraint circuitry, if necessary. Hence, the new analytical synthesis methods may be called ‘expansion in a continuous fraction using sub-circuits [69]’ and are different from one another due to the usage of different sub-circuits and the realisation of distinct transfer functions. Note that these new analytical synthesis methods can be applied to the synthesis of linear systems with stable transfer functions. In the present study, three new analytical synthesis methods are introduced for realising one elliptic even-nth-order and two elliptic odd-nth-order filter structures using DDCCs and FDCCIIs with all the capacitors and resistors grounded.

## 2 Analytical synthesis methods

### 2.1 Analytical synthesis method (ASM) for even-order elliptic filter

In this section, we will first analytically synthesise an elliptic even-nth-order filter structure with the following transfer function:

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{a_n s^n + b_{n-1} s^{n-1} + \cdots + a_1 s + b_0}{a_n s^n + a_{n-1} s^{n-1} + \cdots + a_1 s + a_0}.
\]

(1)

where \( n \) is an even integer. DDCCs with input–output characteristics given by

\[
I_{Y_1} = I_{Y_2} = I_{Y_3} = 0,
\]

(2)

\[
V_{X_\pm} = V_{Y_1} - V_{Y_2} + V_{Y_3},
\]

(3)

\[
I_{Z_\pm} = \pm I_{X_\pm},
\]

(4)

and FDCCIIs with input–output characteristics given by

\[
I_{Y_1} = I_{Y_2} = I_{Y_3} = I_{Y_4} = 0,
\]

(5)

\[
V_{X_+} = V_{Y_1} - V_{Y_2} + V_{Y_3},
\]

(6)

\[
V_{X_-} = V_{Y_4} - V_{Y_1} + V_{Y_2},
\]

(7)

and \( I_{Z_\pm} = I_{X_\pm} \) will be used as active elements in the synthesis process.

Since DDCCs and FDCCIIs enjoy the superiority of intrinsic VM addition and subtraction, the transfer function (1) may be replaced by the following: (see (8)).

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = 1 - \frac{a_n s^n + b_{n-1} s^{n-1} + \cdots + a_1 s + b_0}{a_n s^n + a_{n-1} s^{n-1} + \cdots + a_1 s + a_0}.
\]

(8)

Fig. 1 DDCC and FDCCI-based even-nth-order elliptic filter structure

Fig. 2 Amplitude frequency response of the voltage gain \( V_{X_\pm}(V_{Y_1} - V_{Y_2} + V_{Y_3}) \) of the DDCC+ [27]

Fig. 3 Amplitude frequency response of the current gain \( I_{Z_\pm}/I_{X_\pm} \) of the DDCC+ [27]
Note that (3) is simpler and easier than (1) from the point of view of the numerator order and relatively easier to synthesise than (1).

Cross multiplying (3), dividing by $s^{n-1}$, and re-arranging yields

$$V_{\text{out}}(a_0 s + a_{n-1}) = V_{\text{in}}(a_{n-1} + \frac{b_1}{s} + \frac{a_{n-2}}{s^2} + \cdots + \frac{a_1}{s^{n-1}} + \frac{b_0}{s^n}) - V_{\text{out}}(a_{n-1} + \frac{a_0}{s} + \frac{a_{n-2}}{s^2} + \cdots + \frac{a_1}{s^{n-1}} + \frac{b_0}{s^n}).$$

(11)

Taking out the last two $s^{-(n-1)}$ terms from (5) yields

$$\frac{b_0}{s^n} V_{\text{in}} - \frac{a_n}{s^{n-1}} V_{\text{out}} = a_0 \frac{1}{s^{n-1}}(V_{\text{in}} - V_{\text{out}}) + \frac{b_0}{s^n} a_{n-1} V_{\text{in}}.$$  

(12)

Adding the other two $s^{-(n-2)}$ terms of (5) to (6) yields

$$\frac{a_n}{s^{n-2}} V_{\text{in}} - a_0 \frac{V_{\text{in}} - V_{\text{out}}}{s^{n-1}} + \frac{a_n}{s^{n-1}}(V_{\text{in}} - V_{\text{out}}) + \frac{b_0}{s^n} V_{\text{in}} = a_0 \frac{1}{s^{n-1}}(V_{\text{in}} - V_{\text{out}}) + \frac{a_0}{s^{n-1}}(V_{\text{in}} - V_{\text{out}}) + b_0 = \frac{a_0}{s^{n-1}}(V_{\text{in}} - V_{\text{out}}) + \frac{a_0}{s^{n-1}}(V_{\text{in}} - V_{\text{out}}) + \frac{b_0}{s^n} V_{\text{in}}.$$  

(13)

where $b_0 = b_1 = a_0$.

Note that, in (7), there are two $V_{\text{in}} - V_{\text{out}}$ terms and one extra term ($\frac{b_0}{s^n} V_{\text{in}}$) in bigger brackets. Moreover, adding the other two $s^{-(n-3)}$ terms of (5) to (7) yields (see (14)), where $b_0 = b_1 = a_0$.

Note that, in (8), there are three $V_{\text{in}} - V_{\text{out}}$ terms and two extra terms ($\frac{b_0}{s^n} V_{\text{in}}$ and ($\frac{b_0}{s^n} s^{-1}$)) in $V_{\text{in}}$. By iteratively applying combinations of (6) to (8), (5) may be decomposed as below after dividing by $a_{n-1}$

$$V_{\text{out}}\left(\frac{a_n}{a_{n-1}} s + 1\right) = V_{\text{in}}(1) + \left(\frac{a_n}{a_{n-1}} s + \frac{a_{n-1}}{s^{n-1}}\right)(V_{\text{in}} - V_{\text{out}}) + \frac{a_{n-1}}{a_{n-2}}(V_{\text{in}} - V_{\text{out}}) + \cdots + \frac{a_n}{a_{n-3}}(V_{\text{in}} - V_{\text{out}}) + \frac{a_n}{a_{n-2}}(V_{\text{in}} - V_{\text{out}}) + \frac{b_0}{a_{n-1}} V_{\text{in}}$$

(14)

where $b_0 = b_1 = a_0$ for $i = 0, 2, 4, \ldots, n - 4, n - 2$.

Changing the plus sign after $V_{\text{in}}(1)$ in (9) to a minus sign, (9) becomes (see (16)), where $b_i = -b_i$ for $i = 0, 2, 4, \ldots, n - 4, n - 2$.

Therefore, we obtain the following $n$ simple equations decomposed from (10) by letting the new node voltages, $V_i$, where $i = 1, 2, \ldots, n - 1$

$$V_i = \frac{a_i}{a_{n-1}}(-V_{\text{in}} + V_{\text{out}}) + \frac{b_i}{a_{n-1}} V_{\text{in}}.$$  

(17)

$$V_i = \frac{a_i}{a_{n-1}}(-V_{\text{in}} + V_{\text{out}} + V_{\text{in}}).$$  

(18)

$$V_i = \frac{a_i}{a_{n-1}}((-V_{\text{in}} + V_{\text{out}}) + V_{\text{in}}) + \frac{b_i}{a_{n-1}} V_{\text{in}}.$$  

(19)

$$V_i = \frac{a_i}{a_{n-1}}((-V_{\text{in}} + V_{\text{out}}) + V_{\text{in}}).$$  

(20)

$$V_{n-i} = \frac{a_{n-i}}{a_{n-i}}((-V_{\text{in}} + V_{\text{out}}) + V_{n-i}).$$  

(21)

$$V_{n-i} = \frac{a_{n-i}}{a_{n-i}}((-V_{\text{in}} + V_{\text{out}}) + V_{n-i}).$$  

(22)

$$V_{n-i} = \frac{a_{n-i}}{a_{n-i}}((-V_{\text{in}} + V_{\text{out}}) + V_{n-i}).$$  

(23)

As a consequence, (10) can be simplified as

$$V_{\text{out}} = -\frac{a_{n-1}}{a_{n-1}}(-V_{\text{in}} + V_{\text{out}} + V_{n-i}).$$  

(24)

Observing (11) to (18), we see that there are two types of equations. Equations (12), (14), (16), and (18) belong to the first type, while (11), (13), (15) and (17) belong to the second type. We first consider the realisation of the first type of equations. Equation (18) for $V_{\text{out}}$ can be realised using one DDCC<sup>−</sup>, one grounded resistor and one grounded capacitor, as shown by the bottom-most sub-circuit of Fig. 1, by letting

$$V_{X_+} = V_{Y_1} - V_{Y_2} + V_{Y_3} = V_{\text{out}} - V_{\text{in}} + V_{n-i}.$$  

(25)

Similarly, (16) for $V_{n-i}$ can be realised using one DDCC<sup>+</sup>, one grounded resistor, and one grounded capacitor, as shown by the bottom circuit from the bottom in Fig. 1, by letting

$$V_{X_+} = V_{Y_1} - V_{Y_2} + V_{Y_3} = V_{\text{out}} - V_{\text{in}} + V_{n-i}.$$  

(26)

Similarly, equations for $V_{n-i}, \ldots, V_{n-i} \ldots, V_{n-i}$ can be realised using one DDCC<sup>+</sup>, one grounded resistor, and one grounded capacitor.
However, the sub-circuit for $V_z$ that uses DDCC+ is replaced by an FDCCII, in view of the fact that we have to realise $V_{out} = V_{in} - V_{out}$. For this purpose, $V_z$ is realised using an FDCCII, as shown by the second sub-circuit from the top in Fig. 1, by letting

$$V_{X_z} = V_{Y_1} - V_{Y_2} + V_{Y_3} = V_{out} - V_{in} + V_i$$

and

$$V_{X_z} = V_{Y_1} - V_{Y_2} + V_{Y_3} = V_{out} - V_{in} = V_{out}$$

(27)

We now consider the realisation of the second type of equations. Equation (17) for $V_{out}$ can be realised using one FDCCII, two grounded resistors and one grounded capacitor, as shown by the second sub-circuit from the bottom in Fig. 1, by letting

$$V_{X_z} = V_{Y_1} - V_{Y_2} + V_{Y_3} = V_{out} - V_{in} + V_{out}$$

and

$$V_{X_z} = V_{Y_1} - V_{Y_2} + V_{Y_3} = V_{out} - V_{in} = V_{out}$$

(29)

so that

$$I_{Z_z} + s^{-1} I_{X_z} = I_{X_z} + s^{-1} I_{X_z} = \left(\frac{a_{n-1}}{a_n}\right)(V_{out} - V_{in} + V_{out}) + \left(\frac{b_{n-1}}{a_n}\right)\frac{V_{in}}{s}$$

(31)

In a similar manner, equations for $V_{out}, V_{out}, \ldots$ can be realised using one FDCCII, two grounded resistors and one grounded capacitor. Equation (11) for $V_z$ can be realised, as shown by the top sub-circuit of Fig. 1 using one FDCCII, two grounded resistors and one grounded capacitor, by letting $V_{Y_1} = 0, V_{Y_2} = V_{in}$ and $V_{Y_3} = 0$. Finally, the superposition of all these sub-circuits realises the FDCCII/DFCICII-based even-nth-order elliptic filter, as shown in Fig. 1. Note that (1) is decomposed into $n$ simple equations, each of which is realised using a DDCC or an FDCCII. Accordingly, the proposed elliptic even-nth-order filter structure employs $(n/2) + 1$ FDCCIs, $(n/2 - 1)$ DDCCs, $(3n/2) + 1$ grounded resistors, and $n$ grounded capacitors.

If we denote the grounded capacitors counting from the top of Fig. 1, where $n = 4$, by $C_1, C_2, C_3$, and $C_4$, and the grounded conductances counting from the top and from left to right by $G_1, G_2, G_3, G_4$, and $G_5$, then the corresponding transfer function is (see (32)), which is the standard transfer function of an elliptic VM fourth-order filter. We now consider the non-ideality of the two active elements, FDCCII and DDCC, which involves the voltage and current transfer gains, denoted by $\alpha$ and $\beta$, respectively. A non-ideal DDCC can be represented by [26]

$$V_{X_z} \equiv a_i(V_{Y_1} - V_{Y_2} + V_{Y_3})$$

and

$$I_{Z_z} \equiv b_i I_{X_z}$$

(33)

(34)

Also, a non-ideal FDCCII may be represented by

$$V_{X_z} \equiv a_i(V_{Y_1} - V_{Y_2} + V_{Y_3})$$

$$V_{X_z} \equiv a_i(V_{Y_1} - V_{Y_2} + V_{Y_3})$$

$I_{Z_z} = b_i I_{X_z}$, and $I_{Z_z} = b_i I_{X_z}$.

Thus, (19) becomes (see (35)). Observing (20), it is evident that if each conductance $G$ is replaced by a conductance which is the original conductance $G$ divided by its corresponding $\alpha$ and $\beta$ shown in (20), then the non-ideal effects will be compensated as stated in the recent report [59], leading to more accurate output signals.

For further investigation, note that the voltage transfer function of the $X^+$ terminal voltage, $V_{X_z}$, with respect to the linear combination, $V_{Y_1} - V_{Y_2} + V_{Y_3}$, of three input voltages, is

$$\frac{V_{X_z}}{V_{Y_1} - V_{Y_2} + V_{Y_3}} = \frac{a_{n-1}}{1 + s/a_{n-1}}$$

(36)

and the current transfer function of the $Z^+$ output current, $I_{Z_z}$, with respect to the $X^+$ input current, $I_{X_z}$, is

$$\frac{I_{Z_z}}{I_{X_z}} = \frac{b_i}{1 + s/a_{n-1}}$$

(37)

for the FDCCII [27] and these are shown in Figs. 4 and 5 of [27], from which it can be seen that the bandwidths for both the voltage and current gains are 10 MHz, the dominant frequency limiting factor. The amplitude-frequency responses of

$$\frac{V_{X_z}}{V_{Y_1} - V_{Y_2} + V_{Y_3}}$$

and $I_{Z_z}/I_{X_z}$, for a DDCC+ (using the implementation of [26] with supply voltage $\pm 1.65 V$ and bias current 158.4 $\mu A$) having a $k_1$ at $X^+$ and $Z^+$ terminals are shown in Figs. 2 and 3 (using Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 $\mu m$ process and level-49 parameters), respectively. It can be seen that both upper 3 dB frequencies are located at 10 MHz. Therefore, substituting (21), (22), and the other corresponding transfer functions of an FDCCII and a DDCC into (20), the maximum operating frequency of the synthesised DDCC and the FDCCII-based circuit is 10 MHz.

### 2.2 Analytical synthesis methods for odd-Order elliptic filter

In this section, we propose two analytical synthesis methods for realising a VM elliptic odd-nth-order filter with the following transfer function:

$$\frac{V_{out}}{V_{in}} = \frac{b_{n-1}s^{n-1} + b_{n-2}s^{n-3} + \cdots + b_3s^2 + b_2}{a_n s^n + a_{n-1}s^{n-1} + \cdots + a_3s^3 + a_2s^2 + a_1s + a_0}$$

(39)

where $n$ is an odd integer, also using DDCCs and FDCCIs.

#### 2.2.1 Analytical synthesis method (ASM) 1::

Cross multiplying and dividing (23) by $s^{-1}$ yield

$$\frac{V_{out}}{V_{in}} \left(a_0 + \frac{a_{n-1}}{s} + \frac{a_{n-2}}{s^2} + \cdots + \frac{a_3}{s^3} + \frac{a_2}{s^2} + \frac{a_1}{s} + a_0 \right) = \frac{b_{n-1}s^{n-1} + b_{n-2}s^{n-3} + \cdots + b_3s^2 + b_2}{s^{n-1} + \frac{a_0}{s^{n-1}}}$$

(40)

Re-arranging (24), we get

$$\frac{V_{out}}{V_{in}} = \frac{a_0 \left(V_{Y_1} - V_{Y_2} + V_{Y_3}\right)}{s^n C_1 + s^3 C_2 + \cdots + s^0 C_n + \left(V_{Y_1} - V_{Y_2} + V_{Y_3}\right)}$$

(32)

$$\frac{V_{out}}{V_{in}} = \frac{a_0 \left(V_{Y_1} - V_{Y_2} + V_{Y_3}\right)}{s^n C_1 + s^3 C_2 + \cdots + s^0 C_n + \left(V_{Y_1} - V_{Y_2} + V_{Y_3}\right)}$$

$$\frac{V_{out}}{V_{in}} = \frac{a_0 \left(V_{Y_1} - V_{Y_2} + V_{Y_3}\right)}{s^n C_1 + s^3 C_2 + \cdots + s^0 C_n + \left(V_{Y_1} - V_{Y_2} + V_{Y_3}\right)}$$

(35)
\[ V_{\text{out}}(a_{n} + a_{-1}) = V_{\text{in}}(b_{n} - 1) + \left( V_{\text{in}} \frac{b_{n} - 1}{s^2} - V_{\text{out}} \frac{a_{n} - 1}{s^2} + a_{n} \right) \]
\[ \quad + \cdots + \left( V_{\text{in}} \frac{b_{n} - 1}{s^{n-2}} - V_{\text{out}} \frac{a_{n} - 1}{s^{n-2}} + a_{n} \right) \]
\[ + \left( V_{\text{in}} \frac{a_{n}}{s^{n-1}} - V_{\text{out}} \frac{a_{n}}{s^{n-1}} + a_{n} \right). \] (41)

The last three terms of (25) may be combined as
\[ V_{\text{in}} \frac{a_{n}}{s^{n-1}} - V_{\text{out}} \frac{a_{n}}{s^{n-1}} = a_{n} \left( V_{\text{in}} - V_{\text{out}} \right). \] (42)

Adding the last two \( s^{-n-3} \) terms of (25) to (26) and recombing yield
\[ \left( V_{\text{in}} \frac{b_{n} - 1}{s^{n-1}} - V_{\text{out}} \frac{a_{n}}{s^{n-1}} \right) \]
\[ + \left( V_{\text{in}} \frac{a_{n}}{s^{n-1}} - V_{\text{out}} \frac{a_{n}}{s^{n-1}} + a_{n} \right) = a_{n} \left( V_{\text{in}} - V_{\text{out}} \right). \] (43)

Adding the last one \( s^{-n-4} \) term of (25) to (27) and rearranging yield (see (44)), where \( b_{i} = b_{i} - a_{i} \).

By iteratively applying the combinations from (26) to (28), (25) becomes (see (45)), where \( b_{i} = b_{i} - a_{i} \) for \( i = 2, 4, \ldots, n - 5, n - 3 \).

Changing the plus sign after \( V_{\text{in}}(1) \) in (29) to a minus sign, (29) becomes (see (46)), where \( b_{i} = b_{i} - a_{i} \) for \( i = 2, 4, \ldots, n - 3 \).

Therefore, we obtain the following \( n \) simple equations decomposed from (30) by denoting the new node voltages, \( V_{n} \), where \( i = 1, 2, \ldots, \), and \( n - 1 \)

\[ V_{1} = a_{n} \frac{a_{n}}{s^{n}} (V_{\text{in}} + V_{\text{out}}). \] (47)

\[ V_{2} = a_{n} \frac{a_{n}}{s^{n}} (V_{\text{out}} + V_{1}). \] (48)

\[ V_{3} = a_{n} \frac{a_{n}}{s^{n}} ((V_{\text{in}} + V_{\text{out}}) + V_{2}) + b_{n} \frac{b_{n}}{s^{n}} V_{n}. \] (49)

\[ V_{4} = a_{n} \frac{a_{n}}{s^{n}} (V_{\text{out}} + V_{3}). \] (50)

\[ \left( V_{\text{in}} \frac{b_{n} - 1}{s^{n-1}} - V_{\text{out}} \frac{a_{n}}{s^{n-1}} \right) + \left( V_{\text{in}} \frac{a_{n}}{s^{n-1}} - V_{\text{out}} \frac{a_{n}}{s^{n-1}} + a_{n} \right) = a_{n} \left( V_{\text{in}} - V_{\text{out}} \right). \]

\[ \left( V_{\text{out}} \frac{a_{n}}{s^{n-1}} - V_{\text{out}} \frac{a_{n}}{s^{n-1}} + a_{n} \right) + \left( V_{\text{out}} \frac{a_{n}}{s^{n-1}} - V_{\text{out}} \frac{a_{n}}{s^{n-1}} + a_{n} \right) = a_{n} \left( V_{\text{in}} - V_{\text{out}} \right). \]

As a consequence, (29) can be simplified as
\[ V_{\text{out}} \left( b_{n} - 1, b_{n} - 1, b_{n} - 1 \right) \quad \text{or} \quad V_{\text{out}} (1) \]

\[ \left( V_{\text{in}} - V_{\text{out}} \right) \left( b_{n} - 1, b_{n} - 1, b_{n} - 1 \right). \] (51)

Observing the above equations, (31), (38), it is apparent that there are four types of equations. Equations (32), (34), (35), and (37) belong to the first type, (33) and (36) to the second type, (38) to the third type, and (31) to the fourth type. Each of (32), (34), (35), and (37) is realised using only one DDCC+ (with \( V_{X} = V_{X} + V_{Y} + V_{Z} \) and \( V_{X} = V_{X} - V_{Y} - V_{Z} \) in \( i = 1, 3, n - 4, \) and \( n - 2 \), respectively, one grounded resistor and one grounded capacitor); see e.g. the second DDCC sub-circuit from the top and the second DDCC sub-circuit from the bottom for the realisations of (32) and (37), respectively, in Fig. 4. The second type is realised by using two grounded resistors, one grounded capacitor and an FDCCII by letting

\[ V_{X} = V_{Y} - V_{Z} + V_{Y} = V_{1} - V_{\text{in}} + V_{\text{out}} \]

and

\[ V_{X} = V_{Y} - V_{Z} + V_{Y} = V_{1} - V_{\text{in}} + V_{\text{in}}. \]

\[ i_{X} + i_{Z} = i_{Y} + i_{Y} = V_{X} - V_{X} + V_{X} + V_{X} \] (57)

The third sub-circuit from the top in Fig. 4 shows the realisation of (33), while the third sub-circuit from the bottom shows the realisation of (36). The third type realising (38) uses one DDCC with \( V_{X} = V_{Y} - V_{Z} + V_{Y} = V_{\text{in}} - V_{-1} + 0 \), two grounded
resistors and one grounded capacitor, while the fourth type of sub-circuit uses one DDCC with
\[ V_{X+} = V_{X-} + \frac{a_{n-1}}{s} V_{in} + 0. \] (58)

one grounded resistor, and one grounded capacitor. These are shown in the bottom-most and top-most sub-circuits, respectively, in Fig. 4. The superposition of all of the sub-circuits realised from (31) to (38) constructs the elliptic DDCC and DDCCI-based odd-order filter structure I, as shown in Fig. 4. Note that we decomposed (23) into n simple equations, and each one realised using a DDCC or an FDCCI. Accordingly, the proposed elliptic VM odd-order filter structure employs \((n – 3)/2\) DDCCs, \((n + 3)/2\) DDCCs, \((3n – 1)/2\) grounded resistors, and n grounded capacitors.

If we denote the grounded capacitors counting from the top of Fig. 4, when \(n = 5\), by \(C_1, C_2, C_3, C_4\), and \(C_5\), and the grounded conductances counting from the top and from left to right by \(G_1, G_2, G_3, G_4, G_5\), and \(G_0\), then the elliptic fifth-order filtering transfer function is (see (59)) . Note that the coefficient of the second-order term of the numerator may be 'smaller' or 'larger' than that of the denominator in an elliptic five-order filter transfer function. Hence, different from ASM 1, the method used for realising transfer function (23), wherein the coefficient of the second-order term of the numerator is 'larger' than that of the corresponding term in the denominator in an elliptic fifth-order filter transfer function is shown below.

Cross multiplying and dividing (23) by \(s^{n-1}\) yield
\[ V_{out}\left(\frac{a_n s + a_{n-1}}{s} + \frac{a_{n-1}}{s^2} + \frac{a_{n-2}}{s^3} + \cdots + \frac{a_2}{s^{n-3}} + \frac{a_1}{s^{n-2}} + \frac{a_0}{s^{n-1}}\right) \]
\[ = V_{in}\left(\frac{b_n}{s} + \frac{b_{n-1}}{s^2} + \cdots + \frac{b_2}{s^{n-3}} + \frac{b_1}{s^{n-2}} + \frac{b_0}{s^{n-1}}\right). \] (62)

Re-arranging (42) yields
\[ V_{out}(a_n s + a_{n-1}) = V_{in}(b_n) + V_{out}\left(\frac{a_{n-1}}{s} - \frac{a_{n-2}}{s^2} + \frac{a_{n-3}}{s^3} + \cdots + \frac{a_2}{s^{n-3}} + \frac{a_1}{s^{n-2}} + \frac{a_0}{s^{n-1}}\right) \]
\[ + \cdots + V_{out}\left(\frac{a_2}{s^{n-3}} + \frac{a_1}{s^{n-2}} + \frac{a_0}{s^{n-1}}\right). \] (63)

Following the same steps as in ASM1, the above equation may be written as
\[ V_{out}\left(\frac{a_n}{b_{n-1}} s + \frac{a_{n-1}}{b_{n-1}}\right) = V_{in}(1) - \left(\frac{a_{n-1}}{b_{n-1}} V_{in} - \frac{a_{n-1}}{b_{n-1}} (V_{in} - V_{out})\right) \]
\[ - \cdots - \left(\frac{a_2}{b_2} (V_{out} - \frac{a_2}{b_2} (V_{out} - V_{out})) + \frac{b_2}{b_2} V_{out})\right) \]
\[ + \cdots + \frac{b_{n-1}}{a_{n-1}} V_{in})\right) + \frac{b_{n-1}}{a_{n-1}} V_{in}). \] (64)

where \(b_{i} = b - a\) for \(i = 2, 4, \ldots, n - 3\).

Therefore, we obtain the following simple equations decomposed from (43) by letting the new node voltages, \(V_i\), where \(i = 1, 2, \ldots, n-1\)
\[ V_i = \frac{a_i}{b_i} (V_{in} - V_{out}). \] (65)

\[ \frac{V_{out}}{V_{in}} = \frac{s^2 C_1 C_2 C_3 G_1 + s^2 C_1 C_2 C_3 G_2 + \cdots + s^2 C_1 C_2 C_3 G_5}{s^2 C_1 C_2 C_3 G_1 + s^2 C_1 C_2 C_3 G_2 + \cdots + s^2 C_1 C_2 C_3 G_5 + s C_1 C_2 C_3 G_1 + s C_1 C_2 C_3 G_2 + \cdots + s C_1 C_2 C_3 G_5}. \] (59)

and (see (61)) respectively. The conductance compensation scheme mentioned in Section 2.1 can also be applied to all of the conductances except \(G_i\) for producing more precise output signals.

### 2.2.2 Analytical synthesis method (ASM) 2

Note that the elliptic fifth-order filter transfer function, (23) when \(n = 5\), has different sets of coefficients based upon distinct \(f_a/f_p\), which may be 1.05, 1.075, 1.1, 1.15, 1.20, 1.25, and 1.30, respectively. Therefore, the coefficient of the second-order term of the numerator may be 'smaller' or 'larger' than that of the denominator in an elliptic fifth-order filter transfer function. Hence, different from ASM 1, the method used for realising transfer function (23), wherein the coefficient of the second-order term of the numerator is 'larger' than that of the corresponding term in the denominator in an elliptic fifth-order filter transfer function is shown below.
\[ V_2 = \frac{a_{1,0}}{a_{0,0}} (V_{out} - V_i). \]  
(66)

\[ V_1 = \frac{a_{1,0}}{a_{0,0}} ((V_{in} - V_{out}) - V_i) + \frac{b_{1,0}}{a_{0,0}} V_{in}. \]  
(67)

\[ V_4 = \frac{d_{1,0}}{d_{0,0}} (V_{out} - V_i). \]  
(68)

\[ V_{n+2} = \frac{a_{n+2,0}}{a_{n+2,0}} ((V_{in} - V_{out}) - V_{n+2}) + \frac{b_{n+2,0}}{a_{n+2,0}} V_{in}. \]  
(69)

\[ V_{n+1} = \frac{a_{n+1,0}}{a_{n+1,0}} (V_{out} - V_{n+1}). \]  
(70)

As a consequence, (44) can be simplified as

\[ V_{out} \left( \frac{a_{n-1,0}}{b_{n-1,0}} + \frac{a_{n,0}}{b_{n,0}} \right) = (V_{in} - V_{n,0})(1) \quad \text{or,} \]

\[ V_{out} \left( \frac{a_{n,0}}{a_{n-1,0}} \right) = (V_{in} - V_{n,0}) \left( \frac{b_{n,0}}{b_{n-1,0}} \right). \]  
(71)

Observing the above simple equations (45) to (52), it is apparent that there are four types of equations. Equations (46), (48), (49), and (51) belong to the first type, which can be realised using one grounded resistor, one grounded capacitor and one DDCC+ with \( V_{x+} = V_{Y+} = V_{Z+} \) (from Fig. 5). The superposition of all of the sub-circuits realised from (45) to (52) constructs the proposed elliptic DDCC and FDCCII-based odd-nth-order filter structure II, as shown in Fig. 5. Note that we decomposed (23) into \( n \) simple equations, and realised each of them using a DDCC or an FDCCII. Accordingly, the proposed elliptic odd-nth-order filter structure employs \( n + 3 \) 2 FDCCIIIs, \( n + 3 \) 2 DDCCs, \( n + 1 \) grounded resistors, and \( n \) grounded capacitors.

If we denote the grounded capacitors counting from the top of Fig. 5, when \( n = 5 \), by \( C_1, C_2, C_3, C_4, \) and \( C_5 \), and the grounded conductances counting from the top and from left to right by \( G_1, G_2, G_3, G_4, G_5, \) and \( G_6 \), then the elliptic fifth-order filter transfer function is (see (74))

\[ V_{out} = \frac{s^5 C_5 C_4 C_3 C_2 C_1 G_6 + s^4 C_5 C_4 C_3 G_5 G_6 + G_5 G_4 G_3 G_2 G_1}{s^5 C_5 C_4 C_3 C_2 C_1 + s^4 C_5 C_4 C_3 G_5 + s^3 C_5 C_4 G_3 G_2 G_1 + s^2 C_5 G_4 G_3 G_2 + s G_5 G_4 G_3 + G_5 G_4 G_3 + G_5 G_4 G_3 + G_5 G_4 G_3 + G_5 G_4 G_3}. \]  
(74)

\[ s^5 C_5 C_4 C_3 G_6 + s^4 C_5 C_4 C_3 G_5 + s^3 C_5 C_4 G_3 G_2 + s^2 C_5 G_4 G_3 + s G_5 G_4 + G_5 G_4 + G_5 G_4 + G_5 G_4 + G_5 G_4. \]  
(75)

and (see (76)) respectively. The conductance compensation scheme mentioned in Section 2.1 can also be applied to all of the conductances except \( G_6 \) for eliminating the non-ideal effects and producing more precise output signals.

3 Simulation results

Simulation 1: The elliptic fourth-order LP and HP filters derived from Fig. 1 (when \( n = 4 \)) are considered to demonstrate the filter feasibility with the H-Spice with the TSMC 0.35 \( \mu \text{m} \) process. The complementary metal oxide semiconductor implementations of the DDCC and the FDCCII are as shown in [26,27], respectively, and \( \pm 1.65 \text{V} \) supply voltages are employed. The component values are given by: (i) \( R_1 = 18.1 \text{k} \Omega, R_2 = 4.68 \text{k} \Omega, R_3 = 14.7 \text{k} \Omega, R_4 = 10 \text{k} \Omega \) (at the X-terminal of the second FDCCII), \( R_5 = 38.6 \text{k} \Omega, R_6 = 3.88 \text{k} \Omega, R_7 = 7.32 \text{k} \Omega, \) and \( C_1 = C_3 = 100 \text{pF}, C_2 = C_4 = 200 \text{pF}, \) and (ii) \( R_1 = 15.2 \text{k} \Omega, R_2 = 306 \text{k} \Omega, R_3 = 13.5 \text{k} \Omega, R_4 = 10 \text{k} \Omega, R_5 = 8.7 \text{k} \Omega, R_6 = 36.3 \text{k} \Omega, R_7 = 4.38 \text{k} \Omega, \) and \( C_1 = C_3 = 100 \text{pF}, C_2 = C_4 = 200 \text{pF}, \) for realising the following fourth-order LP and HP elliptic filter transfer functions:

\[ V_{out} = \frac{s^3 C_5 C_4 C_3 C_2 C_1 G_6 + s^2 C_5 C_4 C_3 G_5 G_6 + G_5 G_4 G_3 G_2 G_1}{s^3 C_5 C_4 C_3 C_2 C_1 + s^2 C_5 C_4 C_3 G_5 + s^1 C_5 C_4 G_3 G_2 + s C_5 G_4 G_3 + C_5 G_4 + C_5 G_4 + C_5 G_4 + C_5 G_4}. \]  
(74)

\[ s^5 C_5 C_4 C_3 G_6 + s^4 C_5 C_4 C_3 G_5 + s^3 C_5 C_4 G_3 G_2 + s^2 C_5 G_4 G_3 + s C G_5 + G_5 + G_5 + G_5 + G_5. \]  
(75)
\[ V_{\text{out}} = \frac{s^4 + 4.46600s^2 + 3.82123}{s^4 + 1.08782s^2 + 2.07169s^2 + 1.12434s + 0.98747} \]  

(77)

with the theoretical output parameters: \( f_p = 100 \text{ kHz}, f_s = 105 \text{ kHz}, A_1 = 3.87, A_2 = 1, \) and peak = 4.0726, and

\[ V_{\text{out}} = \frac{s^4 + 0.79663s^2 + 0.10218}{s^4 + 1.81846s^2 + 3.32744s^2 + 1.96523s + 2.05945} \]  

(78)

with the theoretical output parameters: \( f_p = 100 \text{ kHz}, f_s = 83.3 \text{ kHz}, A_1 = 1, A_2 = 0.0496, \) and peak = 1.11, respectively. The simulated amplitude-frequency response of the elliptic fourth-order LP filter is shown in Fig. 6. As can be seen, the output accuracy is quite good with deviations of 0.899\% for \( f_p = 100.90 \text{ kHz}, 0.491\% \) for \( f_s = 105.52 \text{ kHz}, 3.477\% \) for \( A_1 = 3.7355, 6.642\% \) for \( A_2 = 0.9336, \) and 0.391\% for peak = 4.0885, respectively. It is evident that both the elliptic fourth-order LP and HP filters are feasible operating very well at 100 kHz.
Simulation 2: Let us now consider the elliptic VM fourth-order BP and BR filters derived from Fig. 1. The component values are given by (i) $R_1 = 6.34\, \text{k}\Omega$, $R_1^* = 6.34\, \text{k}\Omega$, $R_2 = 39.5\, \text{k}\Omega$, $R_3 = 6.29\, \text{k}\Omega$, $R_3^* = 6.09\, \text{k}\Omega$, $R_4 = 20.8\, \text{k}\Omega$, and $C_1 = 24\, \text{pF}$, $C_2 = 850\, \text{pF}$, $C_3 = 12\, \text{pF}$, $C_4 = 800\, \text{pF}$, and (ii) $R_1 = 10.3\, \text{k}\Omega$, $R_1^* = 10.3\, \text{k}\Omega$, $R_2 = 51.8\, \text{k}\Omega$, $R_3 = 10.2\, \text{k}\Omega$, $R_3^* = 10.3\, \text{k}\Omega$, $R_4 = 30.8\, \text{k}\Omega$, and $C_1 = 16\, \text{pF}$, $C_2 = 600\, \text{pF}$, $C_3 = 8\, \text{pF}$, $C_4 = 500\, \text{pF}$, respectively, for realising the following elliptic VM fourth-order BP and BR filtering transfer functions:

$$V_{out} = \frac{s^4 + 2.00390s^2 + 1}{s^4 + 0.10340s^2 + 2.01925s + 0.10340 + 1}$$ (80)

with the theoretical output parameters: $f_c = 100\, \text{kHz}$, $f_{p1} = 93.56\, \text{kHz}$, $f_{p2} = 106.9\, \text{kHz}$, $f_{s1} = 89.91\, \text{kHz}$, $f_{s2} = 111.2\, \text{kHz}$, peak$_1 = 6.17$, and

$$V_{out} = \frac{s^4 + 2.08107s^2 + 1}{s^4 + 0.09559s^2 + 2.016425s + 0.09559 + 1}$$ (79)

with the theoretical output parameters: $f_c = 100\, \text{kHz}$, $f_{p1} = 93.56\, \text{kHz}$, $f_{p2} = 106.9\, \text{kHz}$, $f_{s1} = 95.92\, \text{kHz}$, and $f_{s2} = 104.3\, \text{kHz}$. The amplitude-frequency responses of the elliptic fourth-order BP and BR filters are shown in Figs. 8 and 9, respectively. As can be seen, the variation ranges of $f_c$, $f_{p1}$, $f_{p2}$, $f_{s1}$, $f_{s2}$, peak 1, and peak 2 for the BP filter are (i) from 99.515 to 99.793 kHz, (ii) from 91.205 to 92.813 kHz, (iii) from 105.368 to 107.725 kHz, (iv) from 87.258 to
88.689 kHz, (v) from 110.618 to 111.683 kHz, (vi) from 3.156 to 4.468 kHz, and (vii) from 3.267 to 4.439, respectively. The variation ranges of $f_c$, $f_{p1}$, $f_{p2}$, $f_{s1}$, $f_{s2}$, peak 1, and peak 2 for the BR filter are (i) from 99.213 to 99.968 kHz, (ii) from 78.756 to 87.126 kHz, (iii) from 115.258 to 138.121 kHz, (iv) from 85.895 to 89.802 kHz, (v) from 109.124 to 113.543 kHz, (vi) from 0.257 to 0.375 kHz, and (vii) from 0.265 to 0.332 kHz, respectively. Based upon the above H-Spice amplitude-frequency responses, the synthesised elliptic BP and BR filters are feasible at 100 kHz even though the errors of the parameters of the BR filter are much worse than those of the BP filter.

Simulation 3: The elliptic third-order LP filter shown in Fig. 4 (when $n=3$) is now considered to demonstrate the filter feasibility using H-Spice with TSMC 0.35 µm process. Component values are given by $C_1 = 24$ pF, $C_2 = 16$ pF, $C_3 = 24$ pF, and $R_1 = 12.7$ kΩ, $R_2 = 3.06$ kΩ, $R_3 = 18.8$ kΩ, $R_4 = 7.81$ kΩ, with the component spreads, 18.8/3.06 = 6 for the conductances, and 24/16 = 1.5 for the capacitances, for simulating the following elliptic third-order LP transfer function:

$$V_{out} = \frac{0.35225 s^2 + 0.598709}{s^3 + 0.84929s^2 + 1.14586s + 0.59870}$$

with $f_p = 1$ MHz, $f_s = 1.2$ MHz, $A_1 = 0.85$, $A_2 = 0.127519$, and peak 1. Note that the coefficient 0.35225 of the $s^2$ term in the numerator is smaller in magnitude than the coefficient 0.84929 of the $s^2$ term in the denominator. The simulated amplitude-frequency response of the elliptic third-order LP filter is shown in Fig. 10. As can be seen, the output accuracy is quite good with deviations of 0.887% for $f_p = 1.0089$ MHz, 1.248% for $f_s = 1.2150$ MHz, 3.714% for $A_1 = 0.8184$, 4.884% for $A_2 = 0.1337$, and 5.588% for peak $= 1$. 

Fig. 18 Input–output relationship of the fourth-order LP filter with dynamic range 1.25 V

Fig. 19 Input and output signals with THD = 1.0020% as $V_{in} = 0.136$ V

Fig. 20 Input and output signals with THD = 1.0063% as $V_{in} = 0.0602$ V

Fig. 21 Noise with the maximum value 0.0457 mV at 0.1 Hz

Fig. 22 Noise with the maximum value 0.2862 mV at 0.1 Hz (fourth-order LP filter)

Fig. 23 Frequency spectra of two tones for the intermodulation of the third-order LP filter


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interference, which can reduce audio clarity. Two-tone tests for intermodulation linearity simulations of the two elliptic third- and fourth-order LP filters are carried out, and the results shown in Figs. 23 and 24, respectively. As can be seen, the frequency spectrum of the intermodulation resulting from two linear tones is much clearer than that resulting from two nonlinear tones.

Finally, the power dissipations of the elliptic third- and fourth-order LP filters are 7.9200 and 23.6921 mW, respectively.

4 Conclusions

Although the superiority of intrinsic VM addition and subtraction of a DDCC and an FDCCII is very attractive for the synthesis of analogue VM circuits, no elliptic DDCC and FDCCII-based VM even or odd-nth-order filter structure has been presented in the VM literature. In the present study, three analytical synthesis methods, through suitable decomposition of a complicated elliptic nth-order transfer function by a series of iterative algebraic operations that meet the conditions of synthesis with respect to the input-and-output characteristics of the two active elements, DDCCs and FDCCIs, have been proposed to generate one elliptic even-nth-order and two elliptic odd-nth-order filter structures. H-Spice simulation results of the proposed elliptic third-order LP and elliptic fourth-order LP, HP, BP, and BR filters are included, verifying the theoretical results.

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6 References

7 Appendix

A maximally flat (Butterworth) LP filter transfer function of order 25 (see Fig. 25) has its poles located at 

\[ s = \frac{0.0813}{\pi} \left( 1 + \sqrt{\frac{1}{\pi^2} - 1} \right) \]

for various values of \( \pi \). For example, for \( \pi = 2 \), the pole location is 

\[ s = 0.0813 \left( 1 + \sqrt{3} \right) \approx 0.2412 \]

7.1 Butterworth LP filter transfer function of order 25

\[ H(s) = \frac{1}{1 + s^2} \]

\[ H(s) = \frac{1}{1 + s^2} \]

Fig. 25 Comparison of the amplitude-frequency responses of a Butterworth LP filter of order 25, a Chebyshev one of order 8, and an elliptic one of order 4

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numerator, and two second-order factors, \((s^2 + 0.491207s + 0.454281)\) and \((s^2 + 0.051378s + 0.977203)\), in the denominator.

The above three, Butterworth, Chebyshev, and elliptic LP transfer functions of orders 25, 8, and 4, respectively, are simulated using Matlab and then the amplitude-frequency responses obtained, as shown in Fig. 11. As can be seen, the three responses coincide at one point, which is located at the absolute magnitude of 0.7 and angular frequency of 1 rad/s; when \(A_2 = 0.0813\), the ratios of \(f_c/f_p\) are 1.11 for the Butterworth, 1.08 for the Chebyshev, and 1.05 for the elliptic filter, corresponding to very narrow 0.11, 0.08, and 0.05 rad/s transition bands. Thus, we see that in order to achieve nearly the same narrow transition band of an elliptic LP filter of order 4, we need a maximally flat (Butterworth) function of order 25 and an equi-ripple (Chebyshev) function of order 8.