Ahmed A. Morgan, Ph. D.

Lecturer
Computer Engineering Department
Faculty of Engineering, Cairo University

Research Interest

- **Computer Architecture**
- **VLSI Design**
- **Multi-core Systems**
- **Networks-on-Chip**
- **High-Performance Computing and Parallel Architectures**

Education

2007 – 2011 Dept. of Electrical and Computer Engineering, University of Victoria Victoria, Canada
Ph.D. in Electrical and Computer Engineering
Dissertation Title: Networks-on-Chip: Modeling, System-level Abstraction, and Application-specific Architecture Customization

2001 – 2005 Faculty of Engineering at Shoubra, Benha University Cairo, Egypt
M.Sc. in Electronic Engineering
Dissertation Title: FPGA Implementation of a Fully Pipelined ARM Processor

2001 – 2002 Information Technology Institute & Mentor Graphics Corporation Cairo, Egypt
Diploma in Electronic Design Automation & VLSI Design
Grade: Excellent

1995 – 2000 Faculty of Engineering at Shoubra, Benha University Cairo, Egypt
B.Sc. in Electronics and Telecommunications Engineering
Grade*:* Excellent with Honor degree (86.2%)

Work Experience

2011 – Faculty of Engineering, Cairo University Cairo, Egypt
Assistant Professor at the department of Computer Engineering. Teaching and developing computer engineering courses, developing lab manuals, supervising graduate and undergraduate students, and participating in the exam works

Courses Taught: Computer Architecture (1 and 2), High Performance Computing and Parallel Programming, Advanced Computer Architecture, GPGPU, Design for Testability (DFT), Computer Network Modeling, and Cloud Computing

2011 – Faculty of Engineering, Misr International University (MIU) Cairo, Egypt
Part-Time Lecturer at the department of Electronics and Communication Engineering. Teaching and developing computer engineering courses, developing lab manuals, supervising undergraduate students, and participating in the exam works

Courses Taught: Microprocessor and Programming, Computer Organization, and Logic Circuit Design

2007 – 2011 Faculty of Engineering, University of Victoria Victoria, Canada
Teaching and Research Assistant at the Department of Electrical and Computer Engineering. Assisting in teaching electrical and computer engineering courses, helping in creating course materials, developing lab manuals, preparing laboratory experiments and participating in the exam works

Courses Taught: Engineering Design and Communication (1 and 2), Fundamentals of Electrical Engineering, Digital Design, Introduction to Computer Architecture, Engineering Economics, Microprocessor Systems, Computer Systems and Architectures

2002 – 2006 Faculty of Engineering at Shoubra, Benha University Cairo, Egypt
Teaching and Research Assistant at the Department of Electronics, Communications and Computer Engineering. Assisting in teaching electrical and computer engineering courses, developing course materials, preparing laboratory experiments and participating in the exam works

Courses Taught: Fundamentals of Electronic Engineering, Electronics (1 and 2), Electronic Circuits, Measuring Instruments, Logic Design, Electromagnetic Fields, Antennas and Wave Propagation

Publications

A. Book Chapters

1. A. A. Morgan, H. Elmiligi, M. W. El-Kharashi, and F. Gebali, "Bio-inspired NoC architecture optimization," in Autonomic Networking-on-Chip: Bio-inspired Specification, Development, and Verification, P. Cong-Vinh, Ed. CRC Press, 2012.

B. Journals

1. A. A. Morgan, H. Elmiligi, M. W. El-Kharashi, and F. Gebali," Networks-on-Chip Architecture Customization using Network Partitioning: A System-Level Performance Evaluation," International Journal of Computing and Digital Systems, vol. 4, no. 1, pp. 19-31, Jan. 2015.
2. A. A. Morgan, H. Elmiligi, M. W. El-Kharashi, and F. Gebali," Unified multi-objective mapping and architecture customisation of networks-on-chip," IET Computers & Digital Techniques, vol. 7, no. 6, pp. 282-293, Nov. 2013.
3. H. Elmiligi, A. A. Morgan, M. W. El-Kharashi, and F. Gebali,"Improving networks-on-chip performability: A topology-based approach," International Journal of Circuit Theory and Applications, vol. 39, no. 6, pp. 557-572, Jun. 2011.
4. H. Elmiligi, A. A. Morgan, M. W. El-Kharashi, and F. Gebali, "Power optimization for application-specific networks-on-chips: A topology-based approach," Journal of Microprocessors and Microsystems, vol. 33, no. 5–6, pp. 343–355, Aug. 2009.

C. Conferences

1. A. A. Morgan, H. Elmiligi, M. W. El-Kharashi, and F. Gebali, "Multi-objective optimization of NoC standard architectures using genetic algorithms," in Proceedings of the tenth IEEE International Symposium on Signal Processing and Information Technology (ISSPIT'10), Luxor, Egypt, Dec. 15–18, 2010, pp. 85–90.
2. A. A. Morgan, H. Elmiligi, M. W. El-Kharashi, and F. Gebali, "Multi-objective optimization for networks-on-chip architectures using genetic algorithms," in Proceedings of the 2010 IEEE International Symposium on Circuits and Systems (ISCAS'10), Paris, France, May 30–June 2, 2010, pp. 3725–3728.
3. H. Elmiligi, A. A. Morgan, M.W. El-Kharashi, and F. Gebali, "Networks-on-chip topology optimization subject to power, delay, and reliability constraints," in Proceedings of the 2010 IEEE International Symposium on Circuits and Systems (ISCAS'10), Paris, France, May 30-June 2, 2010, pp. 2354–2357.
4. A. A. Morgan, H. Elmiligi, M. W. El-Kharashi, and F. Gebali, "Area and delay optimization for networks-on-chip architectures using genetic algorithms," in Proceedings of the fourth International Design and Test Workshop (IDT'09), Riyadh, Saudi Arabia, Nov. 15–17, 2009, pp. 1–6.
5. H. Elmiligi, A. A. Morgan, M. W. El-Kharashi, and F. Gebali, "A delay-aware topology-based design for networks-on-chip applications," in Proceedings of the fourth International Design and Test Workshop (IDT'09), Riyadh, Saudi Arabia, Nov. 15–17, 2009, pp. 1–5.
6. A. A. Morgan, H. Elmiligi, M. W. El-Kharashi, and F. Gebali, "Area-aware topology generation for application-specific networks-on-chip using network partitioning," in Proceedings of the 2009 IEEE Pacific

Rim Conference on Communications, Computers and Signal Processing (PACRIM'09), Victoria, BC, Canada, Aug. 23–26, 2009, pp. 979–984.

7. H. Elmiligi, A. A. Morgan, M. W. El-Kharashi, and F. Gebali, "A reliability-aware design methodology for networks-on-chip applications," in Proceedings of the fourth IEEE International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS'09), Cairo, Egypt, Apr. 6–9, 2009, pp. 107–112.
8. A. A. Morgan, H. Elmiligi, M. W. El-Kharashi, and F. Gebali, "Networks-on-chip topology generation techniques: Area and delay evaluation," in Proceedings of the third IEEE International Design and Test Workshop (IDT'08), Monastir, Tunisia, Dec. 20–22, 2008, pp. 33–38.
9. A. A. Morgan, H. Elmiligi, M. W. El-Kharashi, and F. Gebali, "Application-specific networks-on-chip topology customization using network partitioning," in Proceedings of the First International Forum on Next-Generation Multicore/Manycore Technologies (IFMT'08), Cairo, Egypt, Nov. 24–25, 2008, pp. 1–6.
10. H. Elmiligi, A. A. Morgan, M. W. El-Kharashi, and F. Gebali, "Power-aware topology optimization for networks-on-chips," in Proceedings of the 2008 IEEE International Symposium on Circuits and Systems (ISCAS'08), Seattle, WA, USA, May 18–21, 2008, pp. 360–363.
11. H. Elmiligi, A. A. Morgan, M. W. El-Kharashi, and F. Gebali, "A topology-based design methodology for networks-on-chip applications," in Proceedings of the second International Design and Test Workshop (IDT'07), Cairo, Egypt, Dec. 16–18, 2007, pp. 61–65.
12. H. Elmiligi, A. A. Morgan, M. W. El-Kharashi, and F. Gebali, "Performance analysis of networks-on-chip routers," in Proceedings of the second International Design and Test Workshop (IDT'07), Cairo, Egypt, Dec. 16–18, 2007, pp. 232–263.
13. A. A. Morgan, Mahmoud E. Allam, May A. Salama, and Hala A. K. Mansour, "Implementation of an ARM Compatible Processor Core for SOC Designs," in Proceedings of the third IEEE/ITI International Conference on Information and Communication Technology (ICICT'05), Cairo, Egypt, Dec. 5–6, 2005, pp. 851-859.