Computer Engineering Department
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Problem #1:

Write a VHDL code for an 8 bit priority encoder. The output of the priority encoder is the number of the highest active bit. The priority encoder also has a VALID output signal which is asserted whenever at least one of its inputs is one. Compile and simulate your code.

Problem #2:

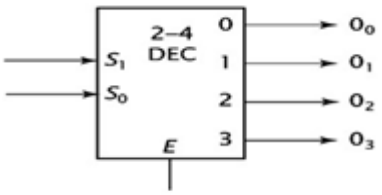
It is required to design a ***majority Logic*** circuit whose output is equal to 1 if the majority of the inputs are 1's. The output is 0 otherwise. The circuit has 3 inputs and it produces logic one if more than one of its inputs are logic one.

a- Draw the schematic diagram of the previous circuit using **only NAND gates**

b- Write a VHDL code for the previous circuit using structural approach (*you have to define NAND gate in VHDL first*)

Problem #3:

Given the following 2 to 4 decoder with enable



S_1	S_0	E	O_0	O_1	O_2	O_3
X	X	0	0	0	0	0
0	0	1	1	0	0	0
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	1

Write a VHDL code for a 3 to 8 decoder using 2 to 4 decoders (*you need to write VHDL code for 2to4 decoder first*), compile and simulate your code

Problem #4:

Write a VHDL code for a D-latch, compile and simulate your code

Problem #5:

Design a 4-to-1 Multiplexer using 2-input AND gates, Inverters and Tri-state buffers only. Write a VHDL code for this design, compile and simulate it.