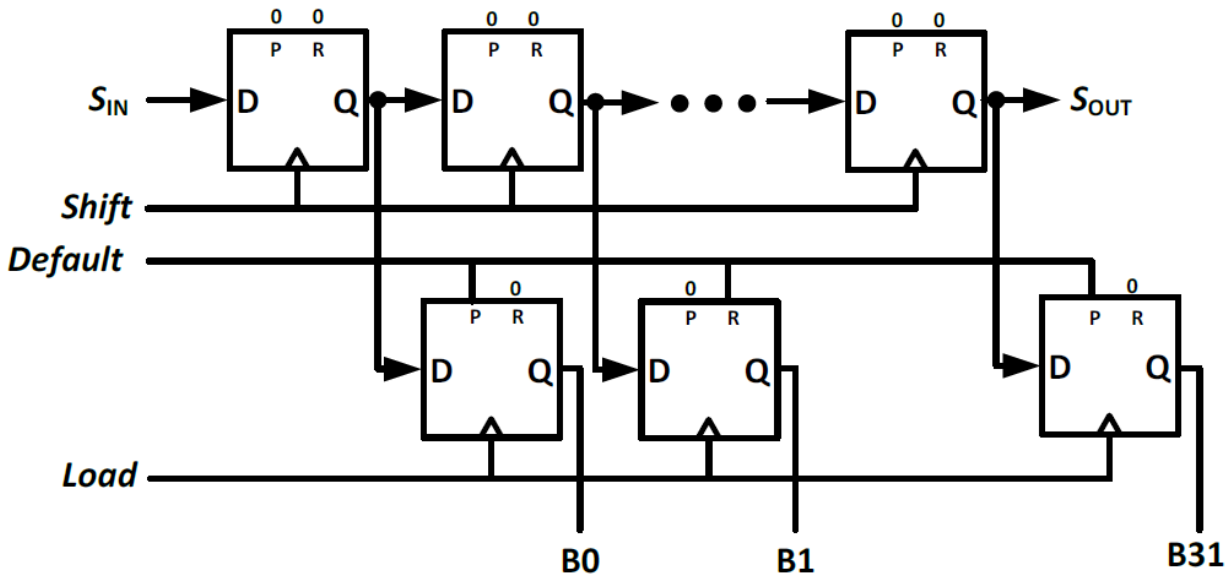
Due date March 29th, 2018



Design and layout a serial Interface Bus (SIB) with the above architecture. The Data (S_{IN}) is shifted right using a "$Shift$" signal and after loading all top registers a "$Load$" signal loads all the 32 bits in parallel manner to set all bits B0 to B31

The requirements of the project are:

1) Design a FF with the following capabilities:
   - Positive Edge CLK
   - Asynchronous Preset and Reset signals.
2) Create a testbench to test the FF
3) Layout the cell for a minimum area, use proper V_{DD}, GND, D, Q , P and R connections to ease top level connections. Make it DRC and LVS clean.
4) Extract the FF and simulate the extracted version.
5) Create top Level schematic of the Serial Interface Bus
6) Simulate the top level by loading a stream of bits and loading it. Test the "$Default$" signal as well.
7) Create a Layout of the top level.
8) Minimize the area.