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Process variability-induced NoC link failure: A probabilistic model

Eman Kamel Gawish [a], M. Watheq El-Kharashi [b,*], M.F. Abu-Elyazeed [a]

[a] Department of Electronics and Electrical Communications Engineering, Cairo University, Giza 12613, Egypt
[b] Department of Computer and Systems Engineering, Ain Shams University, Cairo 11517, Egypt

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ABSTRACT

As technology scales down, the amount of process variations increases causing Networks-on-Chip (NoC) links, designed to be identical, to have current and delay variations. Thus, some links may fail to meet design timing or power constraints. Using current and delay variations with design constraints, we estimate link failure probability across NoC links. Modeling results show that the average NoC link failure probability across a 4×4 mesh reaches 3.3% for voltage mode (VM) links and 3.7% for current mode (CM) links at 32 nm. The average NoC link failure probability also increases as the supply voltage decreases or the operating frequency increases. As NoC mesh size scales from 4×4 to 8×8, the link failure probability doubles to 8% for VM links at 22 nm. Topology evaluation shows that for small NoC size, the grid topology outperforms the tree one with lower amount of variation. On the other hand, for relatively large NoC sizes, the hierarchical tree and ring topologies outperform the grid topology with lower amount of variations across the links.

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1. Introduction

The inability to precisely control the manufacturing process might result in unpredictable behavior of both device and wire (voltage and current), which in turn causes performance and power variations as well as an error-prone operation. These issues have higher effects on modern fabrication technologies with feature sizes smaller than 65 nm. The reasons for the higher effects can be summarized in the following [1]:

1. The feature size is approaching the fundamental dimensions, such as the size of atoms and the wave-length of the light, which are used for patterning lithography masks.
2. The process-resulting variations are becoming comparable to the full length or width of the device.

Process variations mainly result from front-end and back-end fabrication processes. The front-end fabrication processes are those involved in the fabrication of devices, whereas back-end processes are those involved in the fabrication of interconnects. Both the front-end and the back-end fabrication processes can have either random or systematic variability effects. Systematic variations effects have spatial correlation, mainly depending on the position on the die, and usually arise from lithography, chemical mechanical polishing (CMP), or etching fabrication steps. These effects cause systematic variations in gate length, threshold voltage, or line width roughness (LWR). Random variability effects do not have any spatial correlation and are random in nature, like random dopant fluctuation (RDF), oxide thickness fluctuation (OTF), or line edge roughness (LER) [1].

Networks-on-Chips (NoCs) appear as a good alternative to global on-chip interconnect because of their optimized electrical properties [2,3]. NoCs provide better performance in terms of power, delay, higher bandwidth, and scalability compared to buses and global interconnects. An efficient NoC design addresses the issues of performance [4–6], silicon area consumption [7], power/energy efficiency [8,9], reliability [6,10,11], and variability [12]. These issues are the fundamental design drivers for efficient NoC implementations [3].

An NoC is built from basic components as switches, links, and network interfaces. Switches and end nodes are connected by links, thus forming the topology and final network structure. In the NoC scenario, link design becomes more critical than switch design. NoC severe timing and power consumption constraints have made link design a priority. Contrary to the off-chip domain, wiring delay becomes not only appreciable but significant in the flit critical path. Also link power consumption can still be more than 70% of the total network energy consumption [13]. That is why we focus on process-induced variations across NoC links.

As technology scales down, identical NoC links encompass current and delay variations due to different variability sources in the front-end and the back-end fabrication processes. The increase in variations makes worst-case design too pessimistic and very complex. There are many corners due to random and systematic variations effects that may seldom occur and require high margins to be covered [1].

* Corresponding author.
E-mail address: watheq.elkharashi@eng.asu.edu.eg (M.W. El-Kharashi).

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The delay-insensitive current mode (CM) interconnect is a good approach to deal with delay variability. In delay-insensitive CM interconnect, a handshake protocol is used for signaling and transfer of data between the sender and the receiver. While this solves the problem of delay variations, process variations in CM interconnect result in current variations that affect the signal integrity in the current received [14].

Electronic design automation (EDA) tools are moving from pure static analysis to statistical static analysis [1]. Thus, we propose a variability-tolerant NoC link design methodologies for both voltage mode (VM) and CM interconnects [15–17]. In these methodologies, we model variability to calculate a statistical guard/margin for current or delay that tolerates random and systematic variability with a defined power cost.

In this paper, we model link failure probability for VM links and present link failure probability comparison for CM and VM NoC links. We also show model accuracy and computation time using our statistical design approach. Finally, we compare the amount of current and delay variations across the NoC links at different technology nodes for grid, ring, and star topologies.

The main contributions of this work are as follows:

1. The link failure probability resulting from process variability is modeled and a comparison between CM and VM links is conducted.
2. A comparison of link failure probability of a 4×4 mesh versus an 8×8 mesh at different technology nodes is conducted.
3. A study of the effects of supply voltage and frequency scaling on failure probability across NoC links is presented.
4. A hot-spot like floor-plan generator for different NoC topologies is developed and variability-aware topology evaluation is performed.

This paper is organized as follows. Section 2 provides the literature review. Section 3 introduces the interconnect model for link design and process variations. Section 4 shows our statistical delay variations model. Section 5 shows the proposed current variations model. Section 6 shows NoC link failure model. Section 7 introduces NoC topology evaluation at different mesh sizes. Section 8 provides conclusion and future work.

2. Related work

There have been several work in the literature addressing the variability effects on logic and interconnects. Yu et al. modeled the interconnect capacitance random variations resulting from LER, using a statistical MATLAB model, which proved to be an order of magnitude faster than Monte-Carlo simulation with error less than 10% at 45 nm technology [18]. Their results show that the interconnect capacitance deviation increases as technology scales down.

Twaddle et al. presented analysis of LER-resulting variations on delay of short interconnect as technology scales down. Their results indicate that variability effects on delay are increasing and need to be included in statistical models of standard cells [19]. In this paper we also include LER effects in our MATLAB model of process variations.

Mehrotra et al. addressed the effects of systematic process variations on interconnects and modeled their effects on delay, noise, and cross-talk [20,21].

Sarangi et al. modeled the effects of random and systematic process on the probability of error for a microprocessor, mainly measuring variability in logic and SRAM components [22]. Their model provided the failure rates of micro architectural blocks as a function of frequency and the amount of variations. While Sarangi et al. considered only systematic and random variations resulting from front-end fabrication processes to get the normalized gate delay, we consider systematic and random variations resulting from both the front-end and the back-end fabrication processes to get the total interconnect delay variations [15].

Nicopoulos et al. presented the first comprehensive evaluation of NoC susceptibility to process variation effects and proposed an array of architectural improvements in the form of a new router design to increase resiliency to these effects [3]. By process variation exploration, they identified the contribution of each major router stage to the overall critical path delay. The contribution to delay was used to guide the proposed modifications to improve process variation resilience without adversely affecting performance.

Konstantinos et al. proposed a circuit-level fault modeling tool that captured runtime process-induced random delay variations and their corresponding system level faults pointing to router components that need resilient design [23]. In this paper, we model link failure probability due to random and systematic process variations.

Nurmi et al. proposed an algorithm to optimize NoC link design for minimum delay [24]. They used a buffer insertion technique that selected the optimum number of repeaters and their gains to minimize the delay.

Hern et al. addressed the systematic and random effects of the front-end processes on the delay in NoC links [25]. They showed that process variations in NoC links cause links to have different delays. Our work in [15] uses link delay variations to calculate the optimum number of repeaters that tolerates process variations effects.

Nigussie et al. addressed effects of process and environmental variations on the signal integrity of CM interconnect. Additionally, calibration and driver/receiver circuit reconfiguration techniques were proposed to encompass different sources of variations [14]. Our work in [17] proposed statistical current margin that tolerates process variations.

Rivaz et al. addressed effective NoC design by selecting appropriate link length and driver size and relaxing the interconnect density to reduce delay and cross-talk. Their simulation results show how the delay scales with link length and driver size [26]. Our work in [16] shows how delay variations scale with interconnect geometry, like link length, width, height, and spacing.

Gilabert et al. addressed the issue of evaluating different NoC topologies, like grid and tree. They compared the NoC performance (delay and area) of different topologies with different NoC sizes [27].

Fallin et al. proposed a simple hierarchical ring topology that enables better scalability, while maintaining the simplicity of existing ring-based designs [28].

Elmiligi et al. performed topology evaluation for nine commonly used network architectures from performability perspective. Their methodology considered (network topology, target application traffic distribution, mapping of processing elements, noise power, and voltage swing) [10]. In this paper, we perform NoC topology evaluation from the process variations perspective.

Sharifi et al. proposed a variation-aware source routing algorithm for a heterogeneous NoC, where each router has a different operating latency, as a result of random process variations [29]. Their routing scheme computes the best path for each communication between a sender and a receiver, based on the inherent speed of the routers (dictated by process variations) and the current traffic pattern. Sharifi et al. considered delay variations of the router, but as technology scales down, interconnect delay has proven to dominate gate delay.

Ebrahim et al. proposed fault-tolerant routing, tolerating the fault probability resulting from random variations only [30]. The model proposed in this paper considers both systematic and random variations.

3. Interconnect model

This section describes the interconnect model adapted from link design and process variations perspectives. In order to study process variations effects on interconnect, we focus on device and interconnect parameters that can be affected randomly or systematically by process variations, as shown in Fig. 1. Variations in threshold voltage V_{th}, gate length L_g, and gate oxide thickness T_{ox}, resulting from front-end processes, may lead to current/delay variations in the driver of CM/VM interconnect.

The fluctuations in the back-end processes cause variations in geometry and material properties of the wire structure. Studies show that among the back-end fabrication process steps, erosion, and dishing during the CMP process have strong impact on wire parasitics [31]. This is due to the systematic pattern or spatial effects (metal density, width, and space) [14]. Variations in the interconnects resistance and capacitance cause the signal received to be delayed or attenuated [32]. Finally, variations in V_{th}, L_g, and T_{ox} of the receiver will affect the receiver resistive and capacitive loads, which in turn affect the signal received.

It can be noted in Fig. 1 that environmental variations in the supply voltage *GND*, *VDD*, and temperature of the driver and receiver $Temp_{Tx}$, $Temp_{Rx}$, respectively of the interconnect will also cause variations in current I_{win}, I_{rec}, and delay. These environmental variations are out of scope of this work.

3.1. Link layout model

Each interconnect is modeled as a signal-carrying conductor plane and a ground plane, separated by a dielectric and having interconnect capacitance C_{int} that is composed of interlayer capacitance C_p, coupling capacitance C_c, and fringing capacitance C_f, as shown in Fig. 2. We used the interconnect model of a distributed RC network. Assuming the NoC link is short compared to global interconnect, the inductive effects of the NoC link are neglected. The total capacitance and resistance per unit length for a wire line is modeled by [20,21]

$$C_{int} = \varepsilon\left(1.15\left(\frac{W}{H}\right) + 2.8\left(\frac{T}{H}\right)^{0.222} + 2\left(0.03\left(\frac{W}{H}\right) + 0.83\left(\frac{T}{H}\right) - 0.07\left(\frac{T}{H}\right)^{0.222}\right)\left(\frac{S}{H}\right)^{-1.34}\right) \quad (1)$$

$$R_{int} = \frac{\rho}{TW} \quad (2)$$

where C_{int} is the total interconnect capacitance per unit length, ε is the silicon-di-oxide permittivity, W is the metal width, T is the metal thickness, S is the spacing between adjacent metal lines, H is the metal line height above ground plane, R_{int} is the total interconnect resistance per unit length, and ρ is the resistivity of the metal.

It can be noted from the interconnect model in (1) and (2) that the geometry of interconnect determines the total interconnect capacitance and resistance. Hence, variations in interconnect geometry resulting from CMOS fabrication process variability will cause variations in the interconnect capacitance and resistance, which, in turn, will cause variations in the interconnect current/delay as well [33].

3.2. Process variation model

CMOS fabrication process variability causes variations in the interconnect geometry. These variations could be related to the position on the die (systematic or spatial variations) or could be random variations.

3.2.1. Systematic (spatial) process variations

Systematic variability effects have some spatial correlation, which means the variability at a point (x,y) is related to variability at neighbor points with a correlation field given by [25]

$$\rho(r) = \begin{cases} 1 - \frac{3r}{2X_L} + 0.5\left(\frac{r}{X_L}\right)^3, & r \le X_L \\ 0 & \text{otherwise} \end{cases} \quad (3)$$

We use the spherical correlation model with isotropic distribution assumption. Eq. (3) shows the correlation function for this model, where $r = \|l\| - \|l'\|$ is the distance between two given locations, $\|l\|$ and $\|l'\|$, and X_L is a characteristic correlation length depending on the photo lithographic process [25]. We assume that the chip size is small compared to the exposure field, hence setting X_L to 1.

Using this spherical correlation model with the geoR statistical package [34] of R [35], we generate within-die systematic variation maps for gate length, threshold voltage, line width, and line height for different technologies [15]. Fig. 3 shows a variations map generated for the gate length L_g at 45 nm with a 0.12 standard deviation in the value of gate length. From Fig. 3, the values of L_g

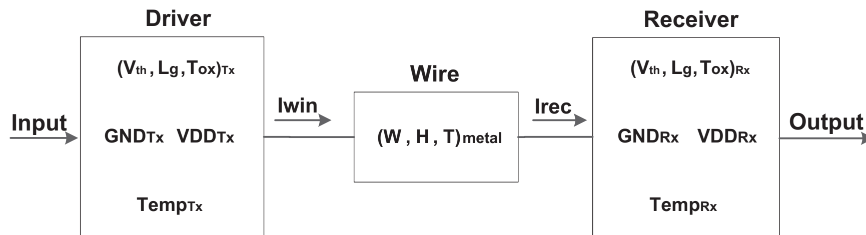

Fig. 1. Parameters affected by process variations in interconnect [25].

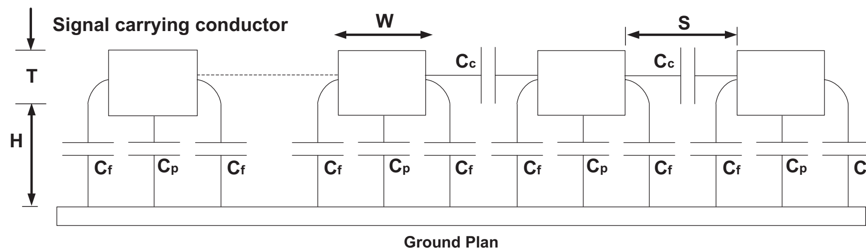

Fig. 2. Interconnect line model for NoC links [20,21].

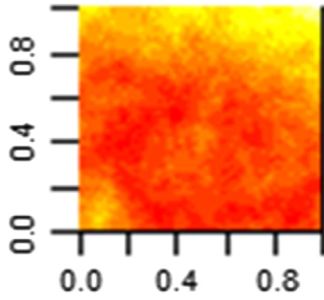

Fig. 3. Systematic variations map for L_g with a 0.12 standard deviation.

depend on the mean value, its deviation, and the position on the die. The color brightness reflects the value of L_g, hence points with near brightness are highly correlated and points with far brightness are loosely correlated.

The variation calculations depend on the mean and standard deviation values for L_g, V_{th}, T_{ox}, LWR, etc., reported in ITRS reports [36]. Systematic variations in device and interconnect geometries will cause systematic deviation components of delay and current, as shown in Fig. 1 and detailed in our previous work [15–17].

3.2.2. Random process variations

We also compute random effects in threshold voltage, gate length, OTF, and LER [15]. These random variation effects are modeled using Hessian function of the numDeriv package [37] of R [35]. Hessian function takes an equation that is a function of normally distributed variables with defined means and standard deviations and generates the mean and standard deviation for the output of the equation. We used Hessian function with delay and current equations in Sections 4 and 5 with means and random deviations of V_{th}, L_g, T_{ox}, and LER as reported in ITRS reports [36] to generate random deviations in delay and current.

We used the Nangate open cell library [38] to extract technology parameters at 45 nm, and performed scaling by the factor $1/s$ to extract technology and layout parameters at other technology nodes [25]. The scaling factor s is the ratio between the scaled technology node and the 45 nm node size in [38]. The values of interconnect and device parameters we used are shown in Table 1.

Table 1
Data used for the technologies considered in this paper.

Technology	65 nm	45 nm	32 nm	22 nm	16 nm
Link length L_{int} **(mm)**	1.00	0.83	0.59	0.41	0.31
Core area (mm^2)	0.69	0.48	0.24	0.11	0.06
Supply voltage V_{DD} **(Volt)**	1.10	1.00	0.90	0.80	0.70
Threshold voltage V_{th} **(Volt)**	0.20	0.18	0.16	0.15	0.13
Gate length L_g **(nm)**	72.00	50.00	35.50	24.40	17.70
Line width W (μm)	0.200	0.140	0.099	0.068	0.049
Line spacing S **(nm)**	202.00	140.00	99.60	68.40	49.70
Line thickness T **(nm)**	404.00	280.00	199.00	136.90	99.60
Line height H **(nm)**	418.00	290.00	206.20	141.80	103.10

4. Statistical delay variations model

This section describes how we used the link design and process model to statistically calculate delay variations across NoC links. The systematic (spatial) and random variations resulting from fabrication process variability are molded to calculate geometry variations at each interconnect link of NoC. It is then used with the interconnect model described in Section 3 and the delay model described below to calculate the delay variations across the NoC links designed to be identical.

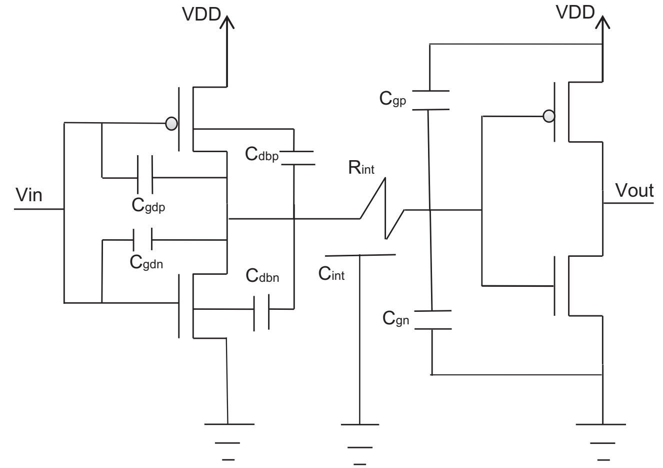

Fig. 4. VM link architecture [20,21].

VM link architecture is shown in Fig. 4. Each NoC link consists of sections of repeaters, each repeater consists of NMOS and PMOS transistors, with gate and drain capacitances Cgn, Cgp, Cdn, and Cdp, respectively. For simplicity, we neglect the gate to drain capacitance Cgdn and Cgdp, when we calculate the overall load capacitance of a repeater since they are order of magnitude smaller than the gate capacitance [20,21].

The interconnect delay variations are modeled by the total interconnect resistance and capacitance as described by [20,21]

$$T_d = 0.4R_{int}C_{int}L_{int}^2 + 0.7(R_{tr}C_{int}L_{int} + R_{tr}C_L + R_{int}L_{int}C_L) \quad (4)$$

$$R_{tr} = \frac{L_g}{W_g}(\mu_n C_{ox}(V_{gs} - V_{th}))^{-1} \quad (5)$$

$$C_{ox} = \frac{\varepsilon}{T_{ox}} \quad (6)$$

$$C_L = Cgn + Cgp + Cdn + Cdp \quad (7)$$

where T_d is the wire delay, L_{int} is the interconnect link length, C_L is the device load capacitance that consists of the input capacitance of the output buffer, which includes the gate and drain capacitances of the NMOS and PMOS transistors Cgn, Cgp, Cdn, and Cdp [20,21], as shown in Fig. 4, R_{tr} is the transistor on-resistance modeled by (5), L_g is the transistor gate length, W_g is the NMOS transistor gate width, μ_n is the electron mobility of NMOS transistor, C_{ox} is the NMOS gate capacitance per unit area, V_{GS} is the gate to source voltage, V_{th} is the NMOS gate threshold voltage, and T_{ox} is the gate oxide thickness.

The generated variations maps for L_g, V_{th}, W, and H are used with the link delay variations model and superimposed on the NoC floor-plan to get the delay attached to each link in the NoC. The results of applying this to the 45 nm technology case are shown in Fig. 5. It can be noted that the NoC links have different delays due to systematic variability effects. Link delay ranges from 2.76 ns to 3.17 ns with an around mean delay of 2.92 ns. The systematic delay deviation is estimated for this sample die. This is repeated for 100 dies and the values of the systematic delay deviations are averaged to get σT_{dsys}, which is as 5.1% for this case study. Estimation for systematic delay variations across a 4×4 grid NoC is done for the 65 nm, 45 nm, and 32 nm technologies. This is illustrated in the fourth column of Table 2. We also computed random effects in threshold voltage, gate length, OTF, and LER for 65 nm, 45 nm, and 32 nm technologies, respectively. These random variations effects are modeled using Hessian function of the numDeriv package [37] of R [35], as described in Section 3.

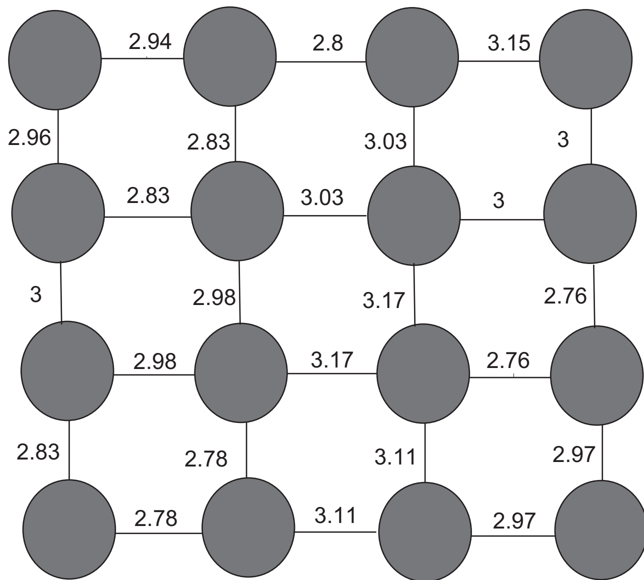

Fig. 5. A 4×4 NoC sample at 45 nm with delay on each link in ns.

Table 2
Link delay random and systematic standard deviations.

Technology	σT_{drand}%		σT_{dsys}%		σT_{dtotal}%
	Proposed	Hern et al. [25]	Proposed	Hern et al. [25]	Proposed
65 nm	3.5	NA	4.6	NA	5.8
45 nm	3.7	2.00	5.1	4.31	6.3
32 nm	4.3	4.23	6.0	4.34	7.4

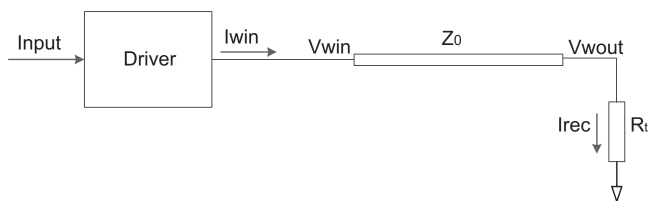

Fig. 6. CM link architecture [14].

By generating random delay deviations for samples of 100 dies and averaging the results, the NoC links have random delay deviation σT_{drand}. The estimation of these random delays is shown in the second column of Table 2.

While Sarangi et al. consider only systematic and random variations resulting from front-end fabrication processes to get the normalized gate delay [22], we consider systematic and random variations resulting from both the front-end and the back-end fabrication processes to get the total interconnect delay variations. The total delay variations can be expressed by

$$\sigma T_{dtotal} = \sqrt{\sigma^2 T_{drand} + \sigma^2 T_{dsys}} \tag{8}$$

Table 2 also shows σT_{dtotal} for different technologies. It can be noted that both random and systematic delay variations increase as technology scales down.

A comparison between our model and recent work in the literature is shown in Table 2. It can be seen that our values are close to those in [25]. The difference in the shown values can be explained by the additional variation effects we consider in our model. While Hern et al. focus only on front-end variability in the buffer transistors [25], we additionally consider variation effects on the interconnect geometry resulting from the back-end variability.

5. Statistical current variations model

The simple model for CM link architecture to be used for analyzing process variations effects is shown in Fig. 6. The model abstracts the interconnect into driver, wire, and receiver.

The driver output current I_{win} goes through lossy transmission line wire represented by characteristic impedance Z_0, near and far voltages V_{win} and V_{wout}, to reach a receiver with a lower current value I_{rec} terminated on a resistive load R_t [14]

$$V_{wout} = V_{win} - I_{win} Z_0 \tag{9}$$

$$I_{rec} = \frac{V_{wout}}{R_t} \tag{10}$$

$$I_{win} = \frac{W_g}{2L_g} \mu_n C_{ox} (V_{gs} - V_{th})^2 \tag{11}$$

$$Z_0 = \sqrt{\frac{R_{int}}{\omega C_{int}}} \tag{12}$$

$$R_t = (1-\gamma) R_{tr} \tag{13}$$

where ω is the angular frequency in GHz and γ is the receiver matching parameter.

In order to reduce power dissipation, the termination resistance is matched to the transmission line characteristic impedance. Hence, R_t is given by

$$R_t = Z_0 \tag{14}$$

and the total current variations is defined by

$$\sigma I_{total} = \sqrt{\sigma^2 I_{rand} + \sigma^2 I_{sys}} \tag{15}$$

The results of current variations obtained by our variability model for a 4×4 mesh at 65 nm are comparable to the values of CM interconnect type LEDRCm (level encoded dual-rail current mode interconnect) in [14], as detailed in our previous work in [17].

6. NoC link failure probability

By link failure probability, we mean the probability of the link to fail to meet the design constraints resulting in failure or error at the receiver. For VM interconnect the failure probability is the probability the link fails to meet the delay constraints due to process variability, whereas for CM interconnects the failure probability is the probability the link fails to meet the current constraints due to process variability.

6.1. VM link failure probability

For synchronous VM links, the failure probability is described by

$$P_{e(link)} = P(T_{link} > T_{nominal}) \tag{16}$$

where $P_{e(link)}$ is the link failure probability, T_{link} is the link delay and $T_{nominal}$ is the link nominal delay that meets the delay constraints.

In case of using the statistical link design in [15], there is still a link failure probability defined as the probability the link delay fails to meet the delay constraints, in spite of using the statistical

delay guard. That is

$$P_{e(link)} = P(T_{link} > (T_{nominal} + \sigma T_{dtotal})) \quad (17)$$

where σT_{dtotal} is the total delay deviation due to process variability, which is used as statistical delay guard/margin in variability tolerant NoC link designs [15].

6.2. CM link failure probability

For asynchronous CM links, handshake protocols are used. Thus, current variations affecting signal integrity are the critical factor impacting link failure, where link failure probability is defined by

$$P_{e(link)} = P(I_{link} < I_{nominal}) \quad (18)$$

where $P_{e(link)}$ is the link failure probability, I_{link} is the link receiver current, and $I_{nominal}$ is the link nominal received current that meets the current constraints. In case of using the statistical link design in [17]

$$P_{e(link)} = P((I_{link} + \sigma I_{statistical}) < I_{nominal}) \quad (19)$$

where $\sigma I_{statistical}$ is the total current deviation set as a statistical guard.

6.3. NoC average link failure probability

We define the NoC average link failure probability $P_{e(NoC)}$ as the sum of link failure probabilities across the NoC links divided by the number of links (n_{links})

$$P_{e(NoC)} = \frac{\sum P_{e(link)}}{n_{links}} \quad (20)$$

The following case study describes how the proposed model in [15] is developed to estimate the failure probability for each link across an NoC.

A number of samples ($n_{samples} = 1000$) of NoCs are generated, where each sample represents a different die with different variability-induced random and spatial variations. The statistical failure probability of each link in NoC is evaluated. A case study for 4×4 mesh at 65 nm is shown in Fig. 7. The link failure probability is calculated by summing the number of times an NoC link in a floor-plan fails to meet the delay constraints due to the systematic (spatial) process variations at its position on the die, within $n_{samples}$, and dividing by the number of samples $n_{samples}$. The calculations are done by MATLAB [39]. The link failure probabilities across the NoC for the case study in Fig. 7 range from 1.6% to 3.4%. Summing the individual link failure probabilities and dividing by the number of links in NoC, the average NoC link failure probability is 2.37% for this case study.

Comparisons of NoC average link failure probabilities due to process variability at different technology nodes for CM versus VM links of 4×4 mesh are shown in Table 3. It is clear that $P_{e(NoC)}\%$ increases as technology scales down. It can also be noted that, for the same mesh size and some technology, VM links achieve lower failure rate than CM links. CM links are more affected by front-end variations than VM ones. For VM links, we consider front-end process-induced variations in transistor resistance. Whereas, for CM links, we consider front-end process-induced variations in transistor resistance of the receiver and the current of the driver.

As shown in Table 4, as mesh size scales from 4×4 to 8×8, the NoC average link failure probability increases from 3.8% to 7.93% at 22 nm. This agrees with the fact that as the mesh size increases, the amount of spatial variations across NoC links increases. We

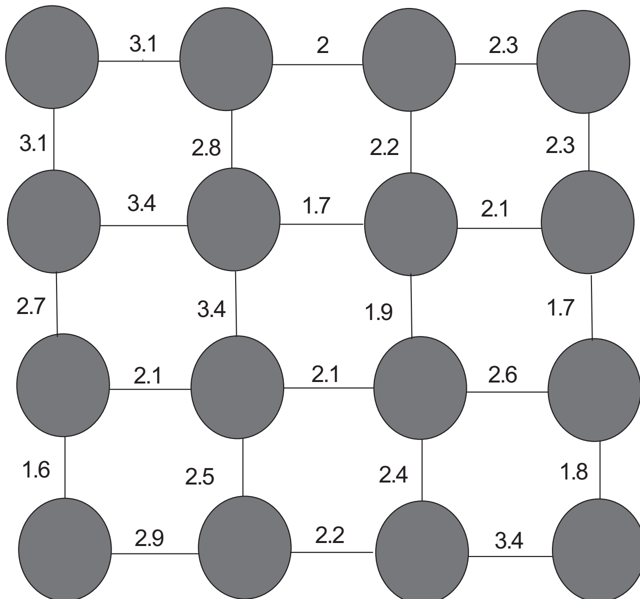

Fig. 7. NoC link failure probability percentage across a 4×4 mesh at 65 nm.

Table 3
A comparison of NoC link failure probabilities of CM versus VM.

Technology node	$P_{e(NoC)}\%$	
	CM	**VM**
65 nm	3.31	2.45
45 nm	3.55	2.78
32 nm	3.69	3.31

Table 4
NoC average failure probabilities for a 4×4 mesh versus a 8×8 mesh for VM links.

Technology node	$P_{e(NoC)}\%$	
	4 × 4 mesh	**8 × 8 mesh**
65 nm	2.45	4.92
45 nm	2.78	5.21
32 nm	3.31	6.49
22 nm	3.80	7.93

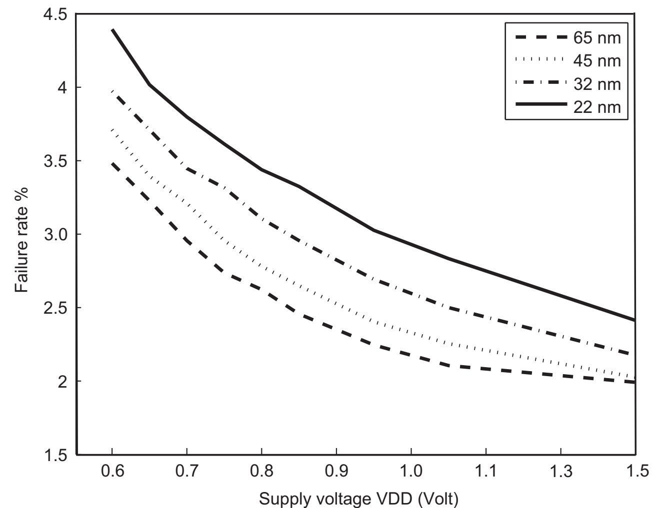

Fig. 8. Average NoC link failure versus supply voltage.

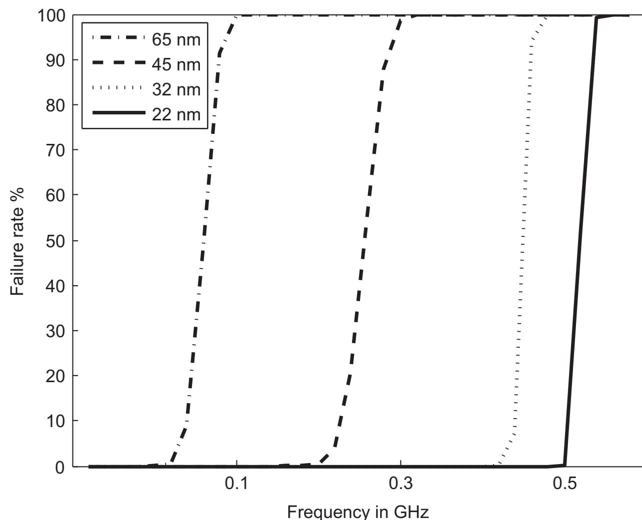

Fig. 9. Average NoC link failure probability versus clock frequency.

Table 5
Computation time for modeling link variations and calculating NoC link failure probabilities.

NoC topology	CPU time (min)
Grid 4 × 4	15
Grid 8 × 8	170

note that the amount of random variations does not scale with mesh size scaling [17].

The average link failure probability for VM links is estimated as the supply voltage VDD scales from 1.5 V to 0.6 V, as shown in Fig. 8. We can note here that, as technology scales down from 65 nm to 22 nm, the link failure probability increases. It can also be seen that, as the supply voltage decreases, the variations in threshold voltage, for example, are more pronounced, hence more links fail to meet the design timing constraints and the average NoC link failure probability increases. This agrees with the results in [22], where the error rate resulting from process variations in logic increases as the supply voltage decreases.

The effect of increasing the link frequency on NoC average link failure probability for VM links is shown in Fig. 9. The link failure probability increases steeply as we increase the frequency, as more and more links fail to meet timing constraints. This also agrees with the results presented in [22], where the error rate increases as the operating frequency increases.

The computation time for modeling link variations and calculating NoC link failure probabilities is shown in Table 5. It is shown that as the mesh size scales from 4 × 4 to 8 × 8, the CPU time needed increases from 15 to 170 min. This can be explained as mesh size increases, the number of links increases and hence more samples are needed to calculate systematic variations.

7. NoC topology evaluation

This section describes our floor-plan generator used to generate different NoC topologies and mesh sizes. It then shows the amount of current/delay variations across NoC links.

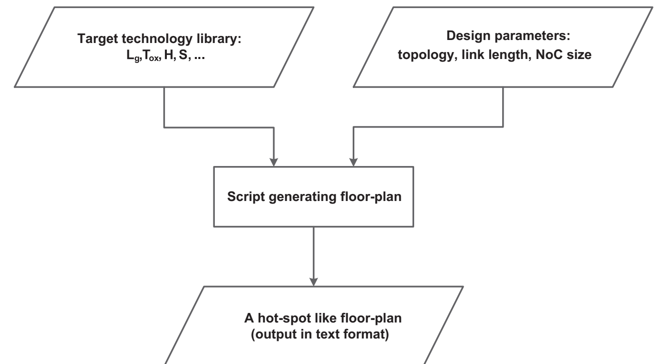

Fig. 10. A hot-spot like floor-plan generator.

7.1. A hot-spot like NoC floor-plan generator

We developed a hot-spot like NoC floor-plan generator, where floor-plans are generated for different topologies (grid, ring, torus, hierarchical ring, and hierarchical trees). The floor-plan tool locates each NoC link on the die with *x*, *y* coordinates for a two-dimensional floor-plan. The link location is used with the deployed systematic process variations model described in Section 3 to calculate the amount of induced systematic variations between the NoC links across the die. Using the location coordinates to locate the temperature variations across the die is out of the scope of this work.

The NoC floor-plan tool is implemented in MATLAB, as described in Fig. 10. Our floor-plan generator has two sets of inputs:

1. The target technology library, which contains the technological parameters, i.e., metal height, thickness, width, and spacing. For smaller technology nodes the dimensions are smaller, with higher correlations between the links according to (3) which increases the amount of variations, as described in Table 2.
2. The NoC design parameters, including target topology, NoC size, and link length.

The output of the generator is a hot-spot like floor-plan file in text format. Each NoC link is described by a name, width, height, left *x*, and bottom *y*, this format is similar to the format generated by hot-spot floor-plan tools used in literature [22].

7.2. Topology comparison

The most popular NoC topologies used in the literature are grid, rings, and torus. While grid does not scale well as NoC size increases, hybrid rings and hybrid trees have proven to provide better scalability and performance over grid as NoC size increases [26,27].

In this subsection, we perform topology evaluation with respect to the overall variations incurred in NoC links in different topologies, like grid, tree, ring, hierarchical ring (Hring), and hierarchical tree (Htree) for certain NoC sizes at 22 nm technology node. The comparisons are performed for 16-core and 32-core NoCs between the topologies: grid (shown in Fig. 5), ring, the Hring (shown in Fig. 11), and Htree (shown in Fig. 12). Fig. 11 and Fig. 12 show 3-layer Hring and Htree, where each layer of the hierarchy in each of the topologies has a different color.

Fig. 13 shows topology evaluation from a systematic variations perspective across all NoC links at 22 nm technology for VM interconnect links for NoCs of 64 and 16 cores. Results show that at small NoC sizes, grid outperforms tree with lower systematic variations across its links. This comes in accordance to results in [27]; the grid has better performance than the tree at relatively

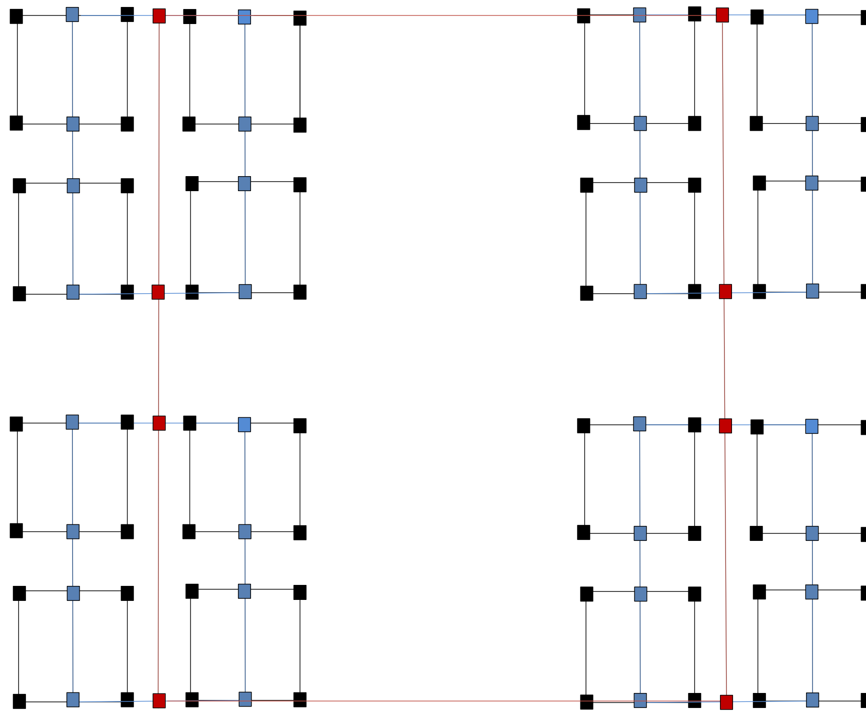

Fig. 11. A $4 \times 4 \times 4$ hybrid ring (Hring) NoC topology.

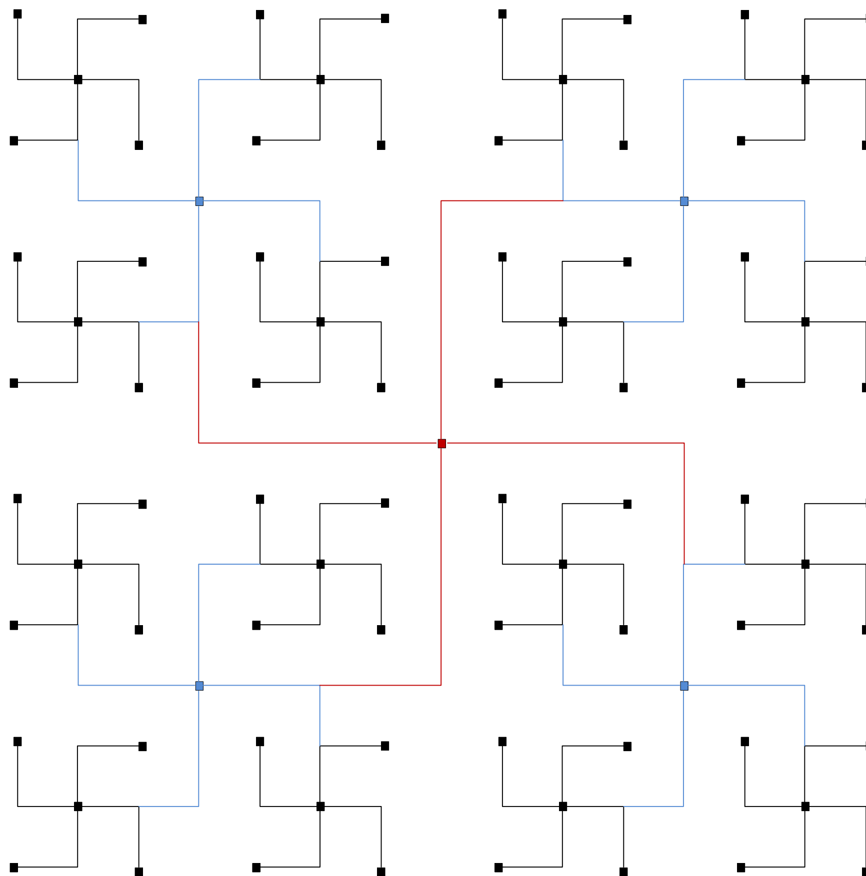

Fig. 12. A $4 \times 4 \times 4$ hierarchical tree (Htree) NoC topology.

small NoC sizes. Our evaluation also shows that the random component of the variations is not affected by the NoC topology. This can be explained as different topologies have different spatial properties depending on their positions on the die, hence have also different systematic components. On the other hand, random variations have no spatial properties and do not depend on the position on the die. Thus, random variations are independent of the NoC topology.

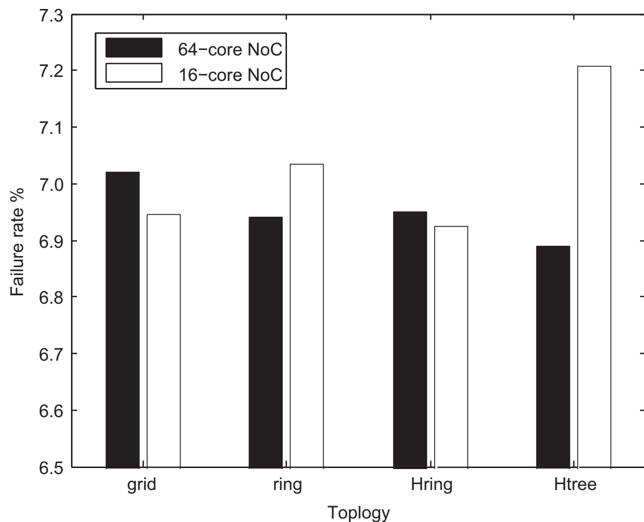

Fig. 13. NoC topology evaluation with VM links at 22 nm.

NoC topology evaluation is also conducted for VM links of a 64-core NoC at 22 nm technology node, as shown in Fig. 13. It can be seen that, from a process variability perspective, both the tree and the ring topologies outperform the grid topology at relatively large NoC sizes. This agrees with results reported in [28] and comes in accordance with grid poor scalability at large NoC sizes. It can also be noted that, as technology scales down, the amount of current/delay systematic variations also increases.

8. Conclusion and future work

This work models NoC link failure resulting from spatial (systematic) and random variations in interconnects due to CMOS fabrication front-end and back-end process variability. The NoC link geometry variations are used to calculate the interconnect delay/current variations in a statistical approach. In our previous work [15–17], we proposed a statistical NoC link design methodology for both CM and VM NoC links. We extended our previous work to calculate NoC link failure probability due to delay variations of VM or current variations of CM interconnect. Results show that link failure probability reaches 3.7% for 4×4 meshes. We studied the effect of increasing the supply voltage or clock frequency on the link failure probability by changing the supply voltage or clock frequency and running our link failure model at different technology nodes. Results show that the link failure probability increases as the supply voltages decreases or the clock frequency increases. We also performed topology evaluation from a process variability perspective. Results show that while the amount of random variations does not change with NoC topologies, the amount of systematic variations differs for different NoC topologies. It was also demonstrated that for relatively large NoC sizes, the tree topology outperforms grid from variations perspective. This comes in accordance with the results of performance-aware evaluation conducted recently in the literature [27].

Finally, although presented approaches target process variability random and systematic effects, they can be applied for design optimization for technologies from 65 nm down to 22 nm. Our model can be used to optimize the link design to tolerate process variability with known failure probability. We also provide the designer with the knowledge required to do variability-aware NoC mesh size scaling and topology selection.

As a future work, the NoC link failure probability can be used in modifying some routing protocols to rout flits to the links with lower link failure probability and measuring of the NoC overall failure rate under different traffic patterns and NoC architectures. This will help designers select the routing algorithms that are more tolerant for process variations for a certain NoC core size, injection rate, buffer size, clock frequency, traffic pattern, and technology node. Another possible future work is to input runtime temperature/supply-voltage variations to our link failure model. Changing the temperature/supply-voltage will change the amount of variations, and hence will change the link failure probability dynamically with runtime variations.

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