New Non-Destructive Read/Write Circuit for Memristor-Based Memories

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Abstract—The recently found Memristor is a potential candidate for the next-generation memory because of its nano-scale and non-volatile advantages. In this paper, a new Read/Write circuit design is proposed based on the Memristor as a memory element. The proposed circuit exhibits low power consumption, short delay time, and occupying less layout area. In addition, the proposed circuit has the advantage of non-destructive successive reading cycles capability.

Index Terms—Memristor, Read/Write circuit, Non-volatile memory, nano-computing storage

I. INTRODUCTION

Memristor has been recognized as the first practical implementation of the missing fourth circuit element predicted by L. Chua in 1971 [1]. In 2008, R. S. Williams introduced a two-terminal Titanium dioxide (TiO\textsubscript{2}) nano-scale device that follows the memristive characteristics defined by L. Chua in 1971 [2]. As a new nano-scale device, Memristor has attracted many researchers from the research community to develop Computer-Aided-Design (CAD) models for the Memristor device [3]–[5], proposed several promising applications such as a switch and as a memory cell [6]–[8], and to show the strength of using the Memristor in lieu of the conventional CMOS transistor [9].

It is stated by S. Williams that Memristors can potentially replace the CMOS transistors in future computers while occupying less chip area, consuming less power, and providing better performance [10].

As portrayed in Figure 1, L. Chua argued that there exists a missing link between \( \phi \) and \( q \), which is called Memristance [1] while other relation is linked using the basic circuit element (i.e., resistor (R), inductor (L), and capacitor(C)). By definition, a linear Memristor acts like a resistor. However, if the \( \phi-q \) relation is nonlinear, the device behaviour differs from that of a resistor.

Figures 2.a and 2.b show the physical structure of a Memristor device and its equivalent circuit model. The device is composed of a TiO\textsubscript{2} thin film of length \( D \), sandwiched between two metal contacts. There are two layers in the TiO\textsubscript{2} film. One layer is highly resistive TiO\textsubscript{2} (un-doped layer), and the other layer is filled with oxygen vacancies, which makes it highly conductive (doped layer). The state variable, \( w \), represents the width of the doped region.

When an external bias voltage, \( v \), is applied across the device, the electric field repels the positively charged oxygen vacancies in the doped layer into the undoped layer and the state length \( w \) is changed [2]. Hence, the device total resistivity changes. If the doped region extends to the full length \( D \) (i.e., \( w/D = 1.0 \)), the total resistivity of the device will be low and denoted by \( R_{on} \). On the other hand, when the un-doped region extends to the full length \( D \) (i.e., \( w/D = 0 \)), the total resistivity of the device will be high and denoted by \( R_{off} \).

According to [2], the Memristor exhibits memory effect as the device maintains its resistivity even if the bias voltage is removed. This unique characteristic makes the Memristor a very promising candidate to be used as a non-volatile memory element that will replace the traditional memories such as Dynamic Random Access Memories (DRAMs) and Static Random Access Memories (SRAMs). The mathematical model for Memristive device resistance, \( M \), is given by [7]:

\[
M(w) = R_{on} \times \frac{w}{D} + R_{off} \times (1 - \frac{w}{D}) \tag{1}
\]

where \( 0 \leq \frac{w}{D} \leq 1 \).

Figure 2.c displays the Memristor symbol. The orientation of the symbol follows the equivalent circuit in 2.b, where \( R_{on} \) is at the left and \( R_{off} \) is at the right.

Memristor-based memories exhibit higher storage density than hard drives with access times close to those of SRAM memories. It has been declared that Memristor devices can be scaled down beyond 10nm and can achieve data storage density close to 100 Gbits/cm, which is higher than current advanced flash memory technologies [11], [12]. Despite its advantage, reading stored data from the Memristor is a challenge. Due to the accumulative property of Memristors, repeated
reading cycles may disturb the stored data as in [6], [7] and hence a refreshment circuit is a must.

In this paper, a novel Read/Write circuit using the Memristor device as a memory element. The proposed circuit has the advantage of non-destructive reading process and eliminates the need of refreshment drivers as required by the previous Read/Write circuits such as [7]. Also, the proposed Read/Write circuit exhibits fast access time, low power consumption, and small layout area (i.e., higher storage density).

The rest of the paper is organized as follows. Section II introduces the new proposed Read/Write circuit. Section III highlights the simulation Finally some conclusions are drawn in Section IV.

II. PROPOSED READ/WRITE CIRCUIT

A new Read/Write circuit with non-destructive reading scheme is proposed in Figure 3. The proposed design deals with the Memristor as a single bit memory element, so only two logic levels (i.e., logic ‘1’ and logic ‘0’) are being stored. As normalized width ($w_n$), which equals to $w/D$, varies from zero to one, then, theoretically, $\{w_n = 0 \text{ to } 0.5\}$ defines logic ‘0’ and $\{w_n = 0.5 \text{ to } 1.0\}$ defines logic ‘1’. Due to circuit parameters non-ideality and leakage current, the output pattern should be defined such that some safety margin is allowed. Accordingly, logic ‘0’ is defined by $\{w_n = 0 \text{ to } 0.4\}$ and logic ‘1’ is defined by $\{w_n = 0.6 \text{ to } 1.0\}$, where the rest region $\{w_n = 0.4 \text{ to } 0.6\}$ is left as a safety margin [7]. Correspondingly, the best $w_n$ values for the high resistive state and low resistive state are one and zero, respectively.

![Fig. 3. Proposed Read/Write circuit for a Memristor-based memory.](image1)

As portrayed in Figure 3, the circuit is consisting of two memristors, two switches, and a diode. Hence, the circuit is mainly depending on the memristor to get the advantage of its small layout area and power consumption.

A. Writing Operation

The Write circuit is implemented as shown in Figure 4. In [2], it has been shown that the Memristor state depends on the applied voltage magnitude, polarity, and pulse duration as given by the following equation:

$$\frac{\partial w}{\partial t} = \mu_v \times \frac{R_{on}}{D} \times i(t)$$  \hspace{1cm} (2)

where, $\mu_v$ is the dopant mobility and $i(t)$ is the current flowing through the Memristor. Thus, there is a need to define these parameters to be able to fully switch the internal device state during the writing process. The nonlinear I-V characteristics of the Memristor device make the required pulse duration and voltage magnitude, that will change the device from the low resistive state to the high resistive state, different from the required values for the reverse process [2]. These writing voltage parameters can be adaptively selected according to the state needed to be written on the Memristor. Alternatively, the voltage magnitudes and pulse durations required for writing logic ‘0’ and for writing logic ‘1’ are calculated and the highest values are selected to perform both writing operations, which are denoted by $V_{wr}$ (i.e., $V_{in} = V_{wr}$ during the writing process) for the voltage magnitude and $T_{wr}$ for the pulse duration as portrayed in Figure 5.

![Fig. 4. The proposed Read/Write circuit during the writing operation.](image2)

![Fig. 5. Applying positive voltage to write logic ‘1’ (left) or negative voltage to write logic ‘0’ (right).](image3)
the applied voltage magnitude is decreased then the required pulse duration increases and vice versa). Hence, the value of $V_{wr}$ and $T_{wr}$ should be selected to have the lowest possible voltage magnitude with the highest response scheme. Also note that, the polarity of memristor M1 is chosen to take advantage of the non-linearity criteria of the memristor. As discussed before and presented in [13], the time needed to switch ON the device is larger than the switching OFF time. Accordingly, where memristor M1 is used with this polarity, the circuit will have more immunity to the leakage current.

B. Reading Operation

The key challenge in any Memristor-based non-volatile memory application is the Read circuit. This is because the applied Read voltage will disturb the stored data due to the accumulative property of Memristors. The proposed read circuit is shown in Figure 6.

For reading the stored data, a positive voltage, denoted by $V_{read}$ (i.e., $V_{in} = V_{read}$ during the reading process) is applied for $T_{read}$ pulse duration and two different scenarios are considered based on the stored data.

![Fig. 6. The proposed Read/Write circuit during the reading operation.](image)

1) **The stored data is logic '1':**

In this scenario, Memristor M1 in the ON state and the voltage drop on it is small and hence $V_T$ almost equal to $V_{read}$ which is designed larger than 0.7V to allow the current to flow through the diode and Memristor M2. In this circuit, Memristor M2 is used as a load resistor to get the advantage of the Memristor (i.e., small size, low power consumption, less heat, high resistivity in the OFF state, and compatibility with the circuit design) over the conventional resistor.

The output voltage drop on M2 (denoted by $V_o$) indicates which data is stored on the memory cell (i.e., if $V_o = V_L$, logic '0' is stored and if $V_o = V_H$, logic '1' is stored). As noticed in Figure 6, Memristor M2 is positioned to be always in the high resistive state. The output voltage, $V_o = V_H$, is given by:

$$V_o(= V_H) = V_T - n \times V_T \times \ln\left(\frac{I_d}{I_{sat}}\right)$$  \hspace{1cm} (3)

where, $V_o$ is the output voltage, $V_d$ is the diode voltage drop, $I_d$ is the diode ON current, $I_{sat}$ is the diode saturation current, $n$ is the diode ideality factor, and $V_T$ is the thermal voltage ($= k_B T / q \approx 26mV$ at room temperature). The value of $V_H$ should be designed as large as possible compared to $V_L$.

2) **The stored data is logic '0':**

In this scenario, Memristor M1 in the OFF state and the voltage drop on it is extremely large and hence $V_o$ is very small. $V_{read}$ is designed so that after the voltage drop on M1, $V_T$ is less than 0.7V and hence the diode switches OFF and acts as an open circuit where no current flows through M2.

The non-destructive feature of the proposed circuit does exist because the reading voltage will affect memristor M1 only during reading logic one, there will be no effect during reading logic zero because the diode will act as an open circuit and hence no current will flow through the memory element (M1). As the circuit use a positive voltage to write logic one then the reading voltage polarity and the writing voltage polarity is the same. The only main concern is to choose $V_{read}$ so that it turns ON the diode while reading logic one and OFF while reading logic zero. Also, the diode is used to make sure that the current flows through the load Memristor M2 in one direction to maintain its OFF state and also to provide immunity of the memory Read/Write circuit to leakage currents.

C. Memory array

Portrayed in Figure 7 the introduced memristor memory array with peripheral circuits which is similar to SRAMs [14], [15]. The array is normally folded into fewer rows of more columns because of the very skinny shape of the arrays make it hard to fit the chip into floor plan. Figure 7 represents a folding design. The pulse generator produces read or write pattern signals. When a read operation is performed, read enable signal will trigger the pulse generator to produce the read pattern. On the other hand, during the write operation, the pulse generator will produce the write-one pulse or write-zero pulse based on the incoming data stored in the input buffer (Data-in buffer). Also, the selector units turn the memristor cells to the ground for a write operation or to read circuitry for a read operation. R/W Enable signal managed the selector to switch depending on the needed operation (read or write operation).

For the writing operations, the pulse generator generates write pulses to the memory array based on the data value stored in the data-in buffer. At the same time, the selectors switch the appropriate column lines to the ground. The unselected lines will be floating, and thus there are no changing in the unselected cells.

For the reading operations, the pulse generator produces the read signals. Simultaneously, the selectors switch every selected column to a diode. The resulting voltage drop across the load memristor is captured by the data-out buffer.

The way to access the memristor memory cell is normally
similar to the well known SRAM. The data is written to the cells or read from it by the proposed write or read scheme. Thus, every memristor cell state will be at ideal logic one/zero position accordingly.

## III. SIMULATION RESULTS

The proposed Read/Write circuit behavior is verified by using Cadence Spectre simulation tools. The CMOS peripherals are implemented by TSMC 130nm CMOS technology. The Memristor model is the most important part of these simulations since numerous models for solid-state HP Memristor device had been developed and discussed in [3]–[5]. These models perform device analysis, Spice modeling, and verification results against the real device published data. Some of these models are utilizing a window function to fit the boundary condition or in other words to keep the changes of w within the device boundaries (i.e., from zero to D). Many of these models are implemented in a Verilog-A code as discussed in [5] and presented in [16]. In addition, a new computationally-efficient Memristor device model is proposed to fit all Memristive devices (i.e., TEAM model), which is basically adopted in all of the following simulation.

### A. Writing Operation Simulation Results

In this part, simulations performed based on the worst case change in the Memristor state (i.e., changing \( w_n \) from 0 to 1.0 or from 1.0 to 0). The main Memristor parameters (i.e., \( D, R_{on}, \text{ and } R_{off} \)) used in the simulation are the default ones mentioned in [16]. According to the used model and window function, the device needs 2.35V to be applied for 8nsec to fully change the internal state of the device. Figures 8.a and 8.b show the writing operation and the device response to the applied voltage.

It is clear from Figure 8 that during the writing operation, there is no voltage presented at \( V_{oc} \), which gives an immunity against accidental reading during the writing process. Also the internal state of the load Memristor M2 did not change and only the state of the memory cell (i.e., Memristor M1) was changed as desired.

It is also clear that, writing logic ‘1’ need more voltage than writing logic ‘0’. This is because of the memristor nonlinear I-V characteristics as mentioned in Section II.

### B. Reading Operation Simulation Results

The reading mechanism is conducted by applying a 1V voltage pulse for 3nsec to investigate the stored data on the memory cell. The results approved that the reading operation did not disturb the internal state of the Memristor device. Figures 9.a and 9.b show the output voltage for reading logic ‘1’ and logic ‘0’, respectively.
As shown in Figure 9, the reading mechanism neither change the internal state of Memristors M1 nor M2, and \( V_o \) varies from the high resistive state (i.e., \( V_o = V_H = 0.3V \)) to the low resistive state (i.e., \( V_o = V_L = 0.03V \)). Also it is showed that, the successive reading operations did not disturb the internal state of the memory cell. This is the main contribution of the proposed Read/Write circuit. As most circuits introduced in the literature such as [7], [8] need refreshment techniques to restore the original data after successive reading operations. Accordingly, the proposed Read/Write circuit provide non-destructive reading operations without the need for refreshing circuits because both the reading and writing voltages have the same polarity.

IV. Conclusion

In this paper, the design of new non-destructive Read/Write circuit for Memristor-based memory cell is proposed. The proposed circuit has the advantages of non-destructive successive reading cycles, low power consumption, and small layout area. All these advantages are verified by comprehensive simulations. The TEAM model had been used for the Memristor device simulations due to its accuracy and simplicity. It had been also demonstrated that the proposed circuit capable of maintaining the stored data for large number of successive reading cycles (limited by the leakage current).

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REFERENCES