A New Highly-Linear Highly-Sensitive Differential Voltage-to-Time Converter Circuit in CMOS 65nm Technology

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***Abstract*—Time-Based Analog-to-Digital Converter (ADC), at scaled CMOS technology, plays a major role in designing Software Defined Radio (SDR) receivers as it manifests higher speed and lower power than conventional ADCs. Time-Based ADC includes a Voltage-to-Time converter (VTC) which converts the input voltage into a pulse delay, and a Time-to-Digital Converter which converts the pulse delay into a digital word. In this paper, a novel design of a differential VTC circuit is proposed which reports wider dynamic range and higher sensitivity than previously published VTC circuits in TSMC 65nm CMOS technology, with a supply voltage of 1.2V. This new VTC circuit operates with no sample and hold circuit for analog input frequencies up to 2.5 GHz with a linearity error of 3%.**

I. INTRODUCTION

Nowadays, the effluence of scaling CMOS technology invades all industrial and scientific communities. This drift overcomes the main problem resulted from using conventional Analog-to-Digital Converters (ADCs) [1] in such applications. In fact, due to the capacity of demands, a single Integrated Circuit (IC) chip is intended to have several chains of transmitting and receiving blocks for different wireless standards which require from the ADC: a proper sampling frequency, and a proper dynamic range. As a result, the energy density of rechargeable power sources does not increase as fast as the power consumption of the electronics, so increasing the source power is not the aimed solution.

This induces applications such as Software Defined Radio (SDR) receivers to arise [1], [2]. The SDR IC configures and controls the chain that we want to use, otherwise all chains will be switched on. In SDR receiver, the received noisy RF analog signal is directly applied to a wide-band ADC, followed by the real time Digital Signal Processor (DSP). New ADCs can be reconfigured according to the SDR standard. This implies us to think about new techniques of ADCs design with much small area and low power consumption.

In deep sub-micron CMOS technology, technology scaling makes the ADC design much more complex, as it reduces the supply voltage which results in degrading the headroom level of the signal (signal swing) and the signal-to-noise ratio (SNR). Besides, it has a little effect on the threshold voltage resulting in design complexity (i.e. difficulty in cascading which is the fundamental concept of the op-amp design) [3]. With these causes, the conventional ADCs are not the promising solutions in lower technology nodes.

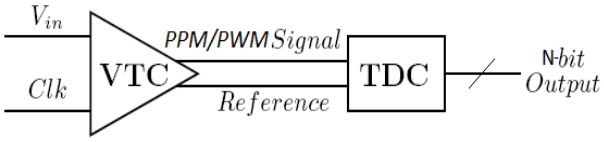

Fig. 1. Time-based ADC architecture.

In high frequencies, the time resolution of digital signals is much greater than the voltage resolution of the analog signals, so we do not need an op-amp or an explicit sample and hold circuit in the Time-Based ADC design. Consequently, We will increase the percentage of the digital part of the system using digital CMOS technology, in order to: solve analog problems, get the full use of the digital signal processing, reduce area and power consumption of the digital blocks, have faster ADCs with higher performance, and make the ADC move more and more to the signal input.

In Time-Based ADC, the analog signal amplitude is sampled and converted into a pulse in time-domain by modulating edges of the reference signal, then the time-domain pulse is quantized into a digital output. This operation is done using a Voltage-to-Time Converter (VTC) and a Time-to-Digital Converter (TDC), respectively as shown in Fig. 1. The VTC is also referred to as either a Pulse Position Modulator (PPM) or Pulse Width Modulator (PWM), depending on whether the delay is applied to one or both edges of the input clock pulses [4]. The TDC circuit consists of digital logic and counter circuits [5].

Several VTC circuits have been introduced in the literature [4], [6]–[8]. The basic core in these circuits is the current starved inverter, in which the applied analog input voltage (Vin) controls the fall time and makes the pulse width of the output inversely proportional to it. All previously published circuits are facing several limitations and design trade-offs between dynamic range and linearity. Also, they suffer from limited sensitivity which is defined as the slope of the pulse width versus Vin curve. In this paper, a new VTC circuit based on a differential current-starved architecture, is proposed.

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There are significant advantages to the differential design. First, the common-mode noise will be rejected. Second, the differential input offers a doubling of the signal amplitude resulting in a 3-dB improvement in the SNR. Third, the even-order harmonic distortion components caused by a single-ended VTC non-linearity will be suppressed. Finally, no reference voltages are required for the design. By gathering all advantages from the usage of lower technology nodes till this novel, we achieve magnificent results in linearity, dynamic range, and sensitivity at reasonable expense of extra area/ power overheads.

The rest of the paper is organized as follows. In Section II, the proposed design and analysis is discussed. Simulation results are illustrated in Section III. Finally, a conclusion is drawn in Section IV.

II. Proposed Design and Analysis

In this work, there are 3 new differential designs of current-starved VTC circuits. The first design intends to control the output falling edge of a PPM VTC. The second design intends to control the output rising edge of a PPM VTC. The final design is the proposed architecture, in which all edges are modulated resulting a PWM VTC. For a differential design, the applied input voltage for each VTC core equals +Vin/2 and -Vin/2. The mode of operation has been discussed in [7]. Fig. 2 shows the block diagram of a differential architecture that is used for all designs.

To get the delay equation of the 1st design, we should calculate at first the delay difference between the output falling edge and the clock rising edge for each core then we get the difference (fall delay) between them. The same procedure to get the rise delay for the 2nd design is done, but we will calculate the delay difference between the output rising edge and the clock falling edge for each design core. For the final design, the delay equation is the difference between each core pulse-width. This is because it is based on PWM.

Fig. 3(a) represents the first design core which is the same as the basic current starved VTC circuit with a quite modification which is revealed as Na1 transistor. This transistor is used to limit the flowing current in saturation mode, in case of lower values of Vin/2. Its width should be much less than Na2 transistor, so it will have a high resistance. This makes the current flow easily through Na2 which has a higher size. Same procedure is done for the core of the second design which is portrayed in Fig. 3(b) where the width of Pb2 is greater than Pb3.

The idea of the proposed differential VTC, as its core shown in Fig. 4, is to have a maximum dynamic range. This d-sign is based on the complementary behavior between the pull-down network and the pull-up network of a single VTC circuit. It has an inverted delayed clock using 11-cell buffer based inv-

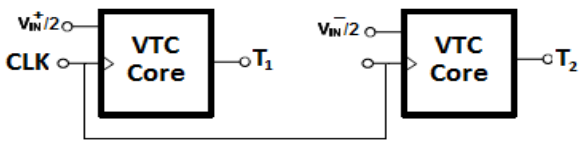

Fig. 2. The differential architecture of the 3 VTC designs.

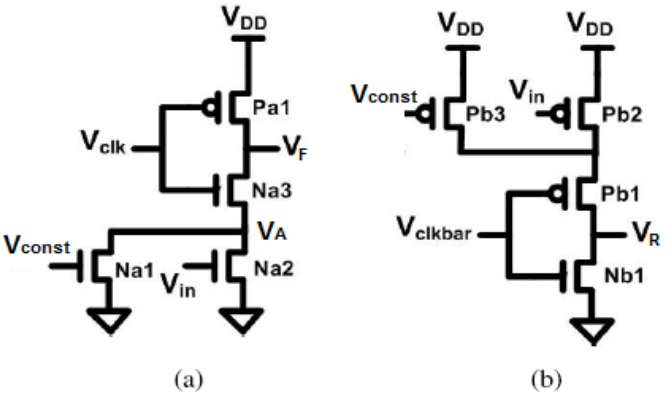

Fig. 3. Circuit schematic of Single-ended current-starved VTCs. (a) Rising circuit. (b) Falling circuit

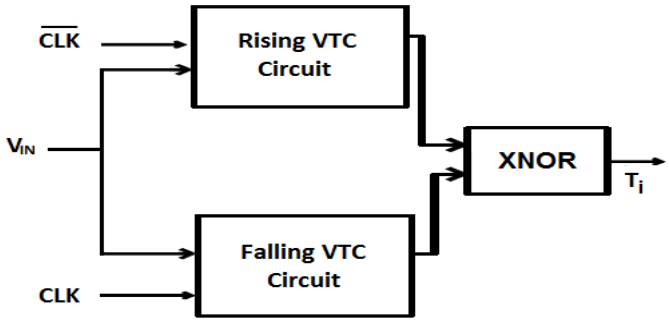

Fig. 4. The VTC core of the proposed architecture.

erter for the pull-up network. This delay helps in producing a high linear output as the output pulse equals $\Delta + T_r - T_f$, where Δ is the buffer delay, T_r is the rise delay of the 2nd design in which we minimize Pb2 width for a slow operation, and T_f is the fall delay of the 1st design in which we increase Na2 width for a high discharging rate of the load capacitor. The XNOR gate is responsible of getting the difference between T_r and T_f.

III. Simulation Results

All design simulations were carried out, by sweeping the input voltage, on Cadence Virtuoso using industrial hardware-calibrated TSMC 65nm CMOS technology and the results were tested using MATLAB. The supply voltage of the 3 designs is 1.2V, the applied DC input voltage is 600mV and the operating clock frequency is 250MHz.

A. Voltage Sensitivity and Linearity

To have a linearity error of 3%, we will sweep the input voltage, Vin, for the 3 designs and we will search for the linear range (dynamic range) in the delay-vs-Vin waveform that achieves this value. After estimating a linear line from the waveform, we will test the linearity on MATLAB. After some iterations, we will reach the 3% acceptable error. The linearity error check is based on curve fitting mechanism, in which we get the difference between the fundamental coefficients of the actual linear equation that produced from the schematic design on Cadence and the ideal first-order fundamental coefficients that fit the actual ones. In the linear range, we will choose any 2 points, and calculate the slope between the delay on y-axis and Vin on x-axis to calculate the circuit sensitivity.

TABLE I: Performance comparison between the proposed differential VTC circuits and single-ended approaches @ 3% error

Parameter	Falling circuit of this work	Rising circuit of this work	Proposed circuit of this work	Falling circuit of [7]	Rising circuit of [7]	Proposed circuit of [7]
VTC Area (μm^2)	0.8256	0.6336	2.7048	0.4128	0.3168	4.2872
DR (mV)	528	1136	1000	240	400	550
Sensitivity (ps/mV)	0.97	2.7	9.6	0.64	2.45	2.13
Power Dissipation F_s/@$F_{s,max}$ (μW)	19.41/259.1	15.7/37.2	159/358.2	9.65/-	9.138/-	61.86/-
$F_{s,max}$ (GHz)	4	0.7	2.5	1.6	0.285	0.7
DR @ $F_{s,max}$ (mV)	364	620	462	80	140	550
FOM F_s/@$F_{s,max}$ ($\times 10^{12}$)	3.59/2.05	20.5/7.23	1.57/1.49	1/-	0.14/-	3.4/-

For the differential falling-VTC, differential rising-VTC and the differential proposed architecture circuits: the linear range of Vin is from -264mV to 264mV and from -568mV to 568mV, and from -500mV to 500mV (i.e. the dynamic range is 528mV, 1136mV and 1000mV) respectively; the sensitivity is 0.97 ps/mV, 2.7ps/mV and 9.6ps/mV respectively. Area and the consumed power are: 0.8256μm^2 and 19.4μW for the 1st design, 10.6336μm^2 and 15.74μW for the 2nd design and 2.7048μm^2 and 159μW for the proposed one. Fig. 5(a), Fig. 5(b), Fig. 6(a), Fig. 6(b), Fig. 7(a) and Fig. 7(b) show the linear range with curve fitting and the linearity error check for each design at sampling frequency of 250MHz.

B. *Maximum Sampling Frequency*

Due to the fact that increasing the sampling frequency (F_s) distorts the signal linearity, we can increase the sampling frequency of each circuit. Hence, we will reduce the dynamic range to keep the 3% error existing. This procedure is permitted, as long as we have a higher dynamic ranges for the 3 designs than single-ended approaches. The 1st design, the 2nd design and the final one can operate in frequencies up to 4GHz, 700MHz and 2.5GHz respectively. They have a dynamic range of 364mV, 620mV and 462mV with a sensitivity of 0.5ps/mV, 1.7ps/mV and 3.2ps/mV respectively.

The maximum power consumed of the 3 designs is 259.1 μW, 37.21μW and 358.2μW. As the dominant power consumption in a CMOS circuit (it has a low static power consumption that is the result of leakage current) is dynamic power when switching at a high frequency, dynamic power contributes significantly to the overall power consumption. Fig. 5(c), Fig. 5(d), Fig. 6(c), Fig. 6(d), Fig. 7(c) and Fig. 7(d) show the linear range with curve fitting and the linearity error check for each design at its maximum sampling frequency.

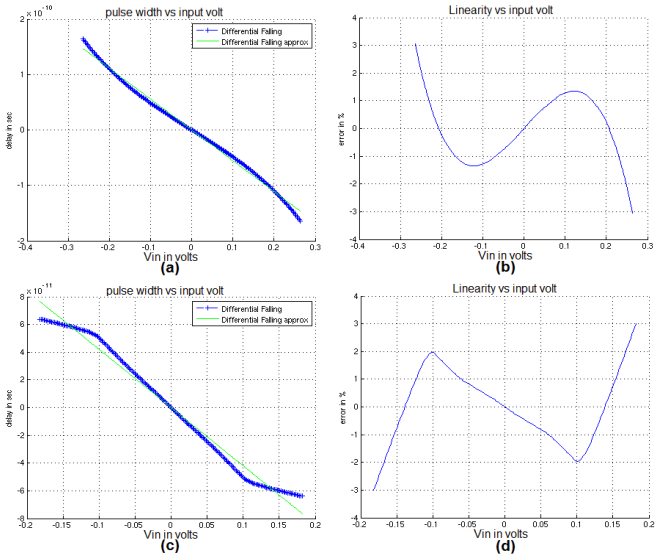

Fig. 5. Differential falling VTC. (a) Linear range at Fs=250MHz. (b) Linearity error check at Fs=250MHz. (c) Linear range at Fs,max=4GHz. (d) Linearity error check at Fs,max=4GHz.

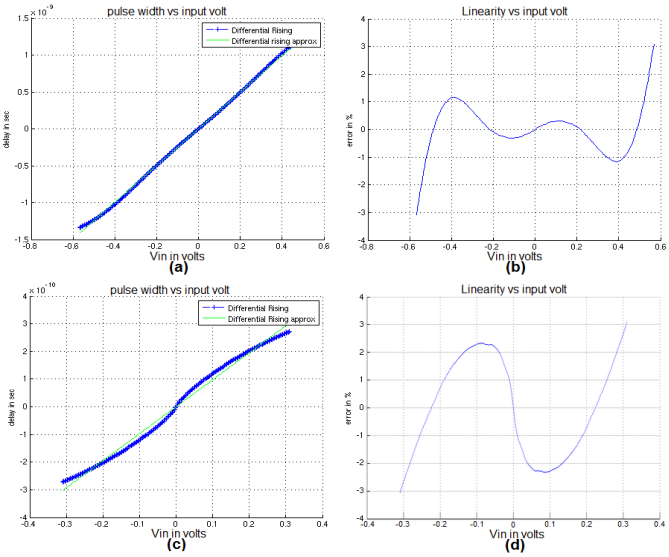

Fig. 6. Differential rising VTC. (a) Linear range at Fs=250MHz. (b) Linearity error check at Fs=250MHz. (c) Linear range at Fs,max=700MHz. (d) Linearity error check at Fs,max=700MHz.

Figure-of-Merit (FOM) [9] can be expressed as in equation (1). Where DR, F_s, and P are the dynamic range, the maximum operated frequency and the power dissipation. The FOM represents the efficiency of using the power to increase the DR and/or the maximum frequency. In case of F_s=250MHz, the FOM for the 1st, 2nd and the proposed design is 3.59×10^{12}, 20.5×10^{12} and 1.57×10^{12}. For a maximum F_s of each design, the FOM equals 2.05×10^{12}, 7.23×10^{12} and 1.49×10^{12}. The proposed design has a quite FOM due to the large power dissipation which is under research to be minimized.

$$FOM = \frac{Fs \times DR^2}{P} \quad (1)$$

Table I compares all the VTC specifications, at a 3% acceptable error, of the 3 designs of this work and the corresponding single-stage designs of [7]. The differential rising-VTC circuit has the highest linear range, due to the small value of the parasitic capacitance of node $V_{F,}$ shown in Fig. 3(a). This produces a low circuit speed. Hence, this differe

TABLE II: Comparison of 65-nm CMOS State-of-the-ART ADCs @ 3% error

Parameter	**This work**	**[7]**	**[8]**	**[10]**	**[11]**	**[12]**	**[13]**	**[14]**
Chip Area (mm^2)	2.7048×10^{-6} (VTC)	4.2872×10^{-6} (VTC)	0.08 (800×10^{-6} VTC)	0.018	0.91	-	0.3	0.11
DR (mV)	1000	550	200	-	-	$1V_{pp}$	-	-
Sensitivity (ps/mV)	9.6	2.13	0.25	-	-	-	-	-
Power Dissipation (μW)	159	61.86	4000	1970	1800	1020	32×10^{4}	6700
$F_{s,max}$ (GHz)	2.5	0.7	7.5	0.8	0.5	1	5	1
FOM	1.57×10^{12}	3.4×10^{12}	0.62pJ/conv	0.116pJ/conv	0.44pJ/conv	0.126pJ/conv	2pJ/conv	0.21pJ/conv

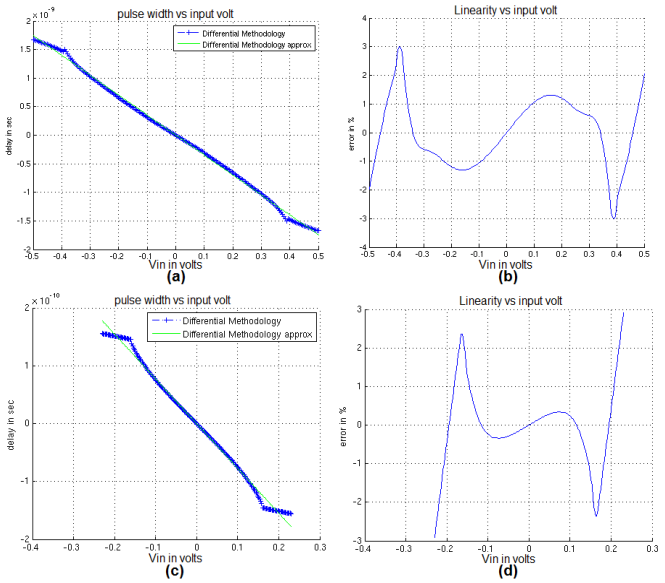

Fig. 7. Differential Proposed Methodology VTC. (a) Linear range at Fs=250MHz. (b) Linearity error check at Fs=250MHz. (c) Linear range at Fs,max=2.5GHz. (d) Linearity error check at Fs,max=2.5GHz.

ntial rising-VTC has a lower Fs,max of 700MHz than other circuits. Table II compares the proposed design with all 65nm CMOS state-of-the-art ADCs which are discussed in [7], [8] and [10]–[14]. From Table II, this work provides the lowest chip area, reasonable sampling speed and FOM, and the highest dynamic range and sensitivity.

IV. Conclusion

In this paper, a novel VTC circuit is proposed which achieves the highest linearity, dynamic analog input range and sensitivity to date. The novelty in this design is emerged from some reasons. First, this work depends on the differential mechanism, in which the even order harmonics are suppressed and the input voltage noise is discarded. Second, we provide an output pulse width which is proportional to the analog input voltage, is the difference between the rising delay and the falling delay of 2 current starved VTCs. Finally, the power of CMOS technology which provides a high-speed low-power and less-area design.

The new VTC circuit provides a 2.5GS/s sampling speed, 9.6ps/mV sensitivity, 1000mV dynamic-range, 2.7048μm^2, 159μW power and 1.49×10^{12} FOM at $F_{s,max}$. This work is a part of time-based ADC with no sample-and-hold (S/H) circuit for analog input frequencies up to 2.5 GHz. If higher input frequencies are expected, the S/H circuit is used.

V. Acknowledgement

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